The CMS pixel readout chip for the Phase 1 Upgrade

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on behalf of the CMS Collaboration

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Outline

• Upgrade Phase I CMS pixel detector
• Upgrade Phase I CMS pixel readout chip
• High rate ROC performance
• ROC radiation hardness
• Layer 1 readout chip status
• Conclusion

Details of ROC modifications see in the talk of Hans-Christian Kästli (PSI)
"Frontend Electronics development for the CMS pixel detector upgrade!", Pixel 2012, Inawashiro, JP
Upgrade Phase I CMS Pixel Detector
Upgrade motivation

New Read-Out Chip needed that could efficiently function at $L > 1 \times 10^{34} \text{cm}^{-2} \text{sec}^{-1}$

<table>
<thead>
<tr>
<th>Detector</th>
<th>Radius (cm)</th>
<th>% Data loss for (cm$^{-2}$s$^{-1}$ @ ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>$1 \times 10^{34}$ @ 25</td>
</tr>
<tr>
<td>Current detector</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BPIX1</td>
<td>4.4</td>
<td>4.0</td>
</tr>
<tr>
<td>BPIX2</td>
<td>7.3</td>
<td>1.5</td>
</tr>
<tr>
<td>BPIX3</td>
<td>10.2</td>
<td>0.7</td>
</tr>
<tr>
<td>FPIX1 and 2</td>
<td></td>
<td>0.7</td>
</tr>
<tr>
<td>Upgrade detector</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BPIX1</td>
<td>3.0</td>
<td>1.19</td>
</tr>
<tr>
<td>BPIX2</td>
<td>6.8</td>
<td>0.23</td>
</tr>
<tr>
<td>BPIX3</td>
<td>10.2</td>
<td>0.09</td>
</tr>
<tr>
<td>BPIX4</td>
<td>16.0</td>
<td>0.04</td>
</tr>
</tbody>
</table>

Already at the end of 2015 luminosity of $L=1.5 \times 10^{34} \text{cm}^{-2} \text{sec}^{-1}$ expected

The detector need to be operational till LS3 (2022) at $L=2 \times 10^{34} \text{cm}^{-2} \text{sec}^{-1}$
Upgrade pixel detector

- **Upgrade Pixel detector**: 4 barrel layers (instead of 3) and 3 forward disks on each side (instead of 2)
- **Installation**: during extended winter shutdown in 2016/17

**Bpix**: 1184 modules, 48M->79M pixels
- L1: r=30mm, 96 modules, 2×TBM09, 4 links
- L2: r=68mm, 224 modules, TBM09, 2 links
- L3: r=109mm, 352 modules, TBM08, 1 link
- L4: r=160mm, 512 modules, TBM08, 1 link

**Fpix**: 672 modules, 18M->45M pixels
- 3 Disks: r=45-161mm, 6×112 modules, TBM08, 1 link
- **Outer ring** rotated by 20° (turbine like)
- **Inner ring** rotated by 20° and tilted by 12° with respect to IP

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Module parameters:

**Full Size**: 66.6 mm × 25/21.6 mm (L2-4/L1)
**Sensor size**: 66.6 mm × 18.8 mm
**ROC size**: 10.55 mm × 8.02 mm
**Weight**: < 3 g
**Si sensor thickness**: 285 μm
**ROC thickness**: 75/175 μm (L1/L2-4)
**Segmentation**: 16 x 52 x 80 = 66560 pixels
**Power**: 2.0 W
Upgrade Phase I Pixel Readout Chip
Upgrade Phase I ROC

• Based on present analog chip

• Limitations of present chip at Phase I
  1. Buffer sizes for level 1 trigger latency
     ➢ Action: increase buffer sizes increased (next slide)
  2. Readout related dead time at higher data volumes
     ➢ Action: additional readout buffer stage added
  3. Higher readout bandwidth needed for higher module number but the same number of fibers
     ➢ Action: digital instead of analog readout with following modifications:
       ✓ on chip ADC
       ✓ new fast digital readout links
       ✓ PLL to provide higher frequencies
       ✓ modification to control logic

• Lower signal threshold required for extend longevity of detector
Layout of the Phase I ROC

(1) **Pixel array**: 52 columns and 80 rows arranged in groups of 2 columns (26 double columns)

(2) **26 Double Column Interfaces**

(3) **Control Interface Block**: readout logic, DACs, I2C interface, voltage regulators, reference and pads
<table>
<thead>
<tr>
<th>Feature</th>
<th>PSI46V2</th>
<th>PSI46DIG</th>
</tr>
</thead>
<tbody>
<tr>
<td>ROC size</td>
<td>7.9 mm x 9.8 mm</td>
<td>7.9 mm x 10.2 mm</td>
</tr>
<tr>
<td>Pixel size</td>
<td>100 μm x 150 μm</td>
<td>100 μm x 150 μm</td>
</tr>
<tr>
<td>Smallest radius</td>
<td>4.3 cm</td>
<td>2.9 cm</td>
</tr>
<tr>
<td>Settable DACs / registers</td>
<td>26 / 2</td>
<td>19 / 2</td>
</tr>
<tr>
<td>Power Up condition</td>
<td>not defined</td>
<td>default values</td>
</tr>
<tr>
<td>pixel charge readout</td>
<td>analog</td>
<td>digitized, 8bit</td>
</tr>
<tr>
<td>Readout speed</td>
<td>40 MHz</td>
<td>160 Mbit/s</td>
</tr>
<tr>
<td>Time stamp Buffer size</td>
<td>12</td>
<td>24</td>
</tr>
<tr>
<td>Data Buffer size</td>
<td>32</td>
<td>80</td>
</tr>
<tr>
<td>Output Buffer FIFO</td>
<td>no</td>
<td>yes</td>
</tr>
<tr>
<td>Double column Speed</td>
<td>20 MHz</td>
<td>20 MHz (40 MHz)</td>
</tr>
<tr>
<td>Metal layers</td>
<td>5</td>
<td>6</td>
</tr>
<tr>
<td>Leakage current compensation</td>
<td>yes</td>
<td>no</td>
</tr>
<tr>
<td>in-time threshold</td>
<td>3500 e</td>
<td>&lt; 2000 e</td>
</tr>
<tr>
<td>PLL</td>
<td>no</td>
<td>yes</td>
</tr>
<tr>
<td>Data loss at max Operating flux</td>
<td>~3.8% at 120 MHz/cm²</td>
<td>1.6% at 150 MHz/cm² (≈3% at 580 MHz/cm²)</td>
</tr>
</tbody>
</table>
High rate X-rays tests
High rate X-rays: measurements vs simulation

- Definition: efficiency = (#readout calibrate signals) / (#injected calibrate signals)
- Periodic calibrate signal injection and trigger at rate of 30kHz
- X-ray inefficiency mostly due to limited time stamp buffer size
- Low WBC (CMS level 1 trigger latency) bypass this limitation
- Remaining inefficiency due to pixel busy and column drain

![Graph showing X-ray (single pixel cluster) efficiency vs rate (psi46dig-v2.1)](image)

- Measurement WBC 50
- Measurement WBC 75
- Measurement WBC 100
- Measurement WBC 125
- Measurement WBC 150
- Measurement WBC 175
- Measurement WBC 200
- Measurement WBC 225
- Simulation WBC 50
- Simulation WBC 75
- Simulation WBC 100
- Simulation WBC 125
- Simulation WBC 150
- Simulation WBC 175
- Simulation WBC 200
- Simulation WBC 225
High rate particles: simulation

- **Main difference with respect to X-ray**
  - more hits per time stamp: 2.3 (particles) vs 1 (X-ray)
  - module readout simulated, not single ROC
  - random (non periodic) trigger used, hence more data loss mechanisms contribute

- **WBC=156 (CMS level 1 trigger latency)**, random trigger at 100kHz rate

- **Expected hit rate at R=6.8cm (Bpix Layer 2) – 120MHz/cm²**

![Efficiency vs rate (simulation, upgrade ROC layer 2-4) graph]

- **Single pixel inefficiency [%]**
- **Particle pixel hit rate [MHz/cm²]**
- **Expected layer 2 rate**
Irradiation studies

Acknowledgment:
The research leading to these results has received funding from the European Commission under the FP7 Research Infrastructures project AIDA, grant agreement no. 262025
Expected irradiation dose

Absorbed dose

for $L=500 \text{ fb}^{-1}$

at $R=2.9\text{ cm (}z=0\text{)}$

expected dose $1.2 \text{ MGy}$
CCE in silicon

12ke− after 2/3 years (200/250fb⁻¹), low threshold required
Timewalk and threshold

• **Timewalk** ($T_{TM}$): time difference between moments at which largest and lowest signals cross ROC threshold
  - analog ROC: $T_{TM} > 25$ ns
  - digital ROC: $T_{TM} < 16$ ns

• **Minimum threshold:**
  - analog ROC: $3200e^-$
  - digital ROC: $<1800e^-$ (also due to reduced x-talk in new ROC layout)

• **Low threshold** increases detector longevity
Irradiation at KIT: samples and dose

- Irradiation done
  - with proton beam, proton energy 23 MeV
  - at two doses: 60Mrad ($2 \times 10^{14} \text{p/cm}^2$) and 120Mrad ($4 \times 10^{14} \text{p/cm}^2$)

- 6 samples irradiated at each dose
  - 4 samples powered and 2 - not during irradiation
Analog and digital current

- Dynamic range of $V_{ana}$ DAC before and after irradiation is fine
- Minor increase of $I_{ana}$ after irradiation
- For several samples irradiated to 120MRad observed current saturation above $V_{ana}=170$

- Small dependence of $I_{dig}$ vs $V_{dig}$ DAC, as expected
- Remains the same after irradiation
Trimming: Vcal threshold and trim bits

- Before and after irradiation ROC trimmed to (internal calibrate signal) \( V_{\text{cal}} = 40 \)
- Trimming works well before and after irradiation
- Small increase (30%) of threshold spread within ROC observed
- After irradiation mean of trim bit distributions shifts slightly around 0 (both positive and negative)

NB: PSI46digV2 – previous version of the final chip, shown for comparison
Noise

- Average noise
  - before irradiation – 144 ± 5e⁻
  - after 60 Mrad – 106 ± 6e⁻
  - after 120 Mrad – 114 ± 8e⁻
- Used conversion factor 50e⁻/Vcal
- Conversion factor after irradiation is not known
- Noise spread among pixels in ROC stays almost the same
Pixel efficiency with high rate Xrays

**Efficiency at 120MHz/cm²**
- measured with Xrays
- higher than 98.5% and
- stays the same for non irradiated and irradiated samples up to 120MRad

**NB**
*Not the best possible measurements: for Dose=0 VICoLoR DAC was not optimized*
Layer I ROC
Main mechanisms of data losses addressed in the design:
1. pixel busy
2. CoLOR overflow
3. readout reset

Leading inefficiency mechanism: at 580 MHz/cm² is larger than 30%
Bpix Layer 1 ROC status

• Double column logic needed modifications for higher data rates
• Hence Dynamic Cluster Column Drain architecture implemented
  – dynamic cluster (2×2 pixels) finding in double column
  – transfer speed increased from 20MHz to 40MHz
  – data throughput in double column improved by factor of 3.5
  – pixel dead time (pixel busy) reduced to 1.3%
  – column busy (leading) inefficiency completely gone
• Dead time free data buffer management (reset RO)
  – buffer logic improved mechanism to protect valid hits from overwriting
  – related data loss reduced by at least factor of 5
Data loss mechanisms in Upgrade ROC for layer 1

**Pixel busy:** 1.3%
- Pixel insensitive until hit transferred to data buffer (column drain mechanism)

**Double column busy:** 0.2%
- Column drain finds hit pixels and transfers hits from pixel to data buffer. Maximum 7 pending column drains requests accepted

**Data Buffer full:** 0.0%
- Size: 80 (32)

**Timestamp Buffer full:** 0.3%
- Size: 24 (12)

**Readout and double column reset:** 0.7% for 100kHz L1 trigger rate

**Luminosity:** $2 \times 10^{34} \text{cm}^{-2}\text{sec}^{-1}$
- Pixel fluence: 585 MHz/cm$^2$

**Total data loss in layer 1 at run start:** 2.5%

**Readout Buffer size:** 80 (0)

**Digital Readout**
- 160 Mbit/s
- 320 Mbit/s

**Data loss mechanisms diagram**
- PUC: Pixel Column Interface
- TBM: Timing and Booking Module
- RB: Readout Buffer
- 26 x / ROC

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Bpix Layer 1 ROC status

• Chip size almost the same as for Layer 2-4 ROC (PSI46digV2.1)
• Pads and data format the same as for PSI46digV2.1
• Power consumption the same or lower than for PSI46digV2.1
• Submission at the end of 2014
Conclusion

• After three iterations (2012-2014) and thorough investigations in labs, beam tests and irradiation ROC for Bpix Layer 2-4 and Fpix works as expected

• Signal threshold could be set as low as 1800e⁻ (compare with present ROC of 3200e⁻)

• Hit efficiency (measured with X-rays and simulated for X-rays and particles) is higher than 98% at expected hit rate (120MHz/cm²) for Bpix Layer 2 even after irradiation of 120MRad

• Production submission is done in July 2014 (48 wafers, the rest will be produced at the end of 2014)

• Design of Bpix Layer 1 ROC is almost done and submission for production is planned at the end 2014
Acknowledgment

In this presentation work of many people from the CMS Pixel Upgrade Phase I community is used. I would like to thank all of them. Special thank to

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Jan Hoss (ETHZ)
Marco Rossini (ETHZ)
Tilman Rohe (PSI)
Silvan Streuli (PSI)
Jackson Young (Uni of Kansas)
Backup slides
Trimming: trim bits

Reproducibility: mean=0.1; RMS=0.6

- After irradiation mean of trim bit distributions shifts around 0 (both positive and negative)
- This may mean increase of trim bits non linearity (to be checked)
- Degradation of pixel threshold uniformity after irradiation to be checked
Timewalk

0 and 60 MRad
Max timewalk below 50 CalDel units (<25ns)

0 and 120 MRad
Max timewalk below 50 CalDel units (<25ns)