The CMS pixel readout chip for the Phase 1 Upgrade

D. Hits, A. Starodumov

ETH Zurich, Switzerland

on behalf of the CMS Collaboration

Pixel 2014 Workshop

1-5 Sep 2014, Niagara Falls (Canada)

Outline

- Upgrade Phase I CMS pixel detector
- Upgrade Phase I CMS pixel readout chip
- High rate ROC performance
- ROC radiation hardness
- Layer 1 readout chip status
- Conclusion

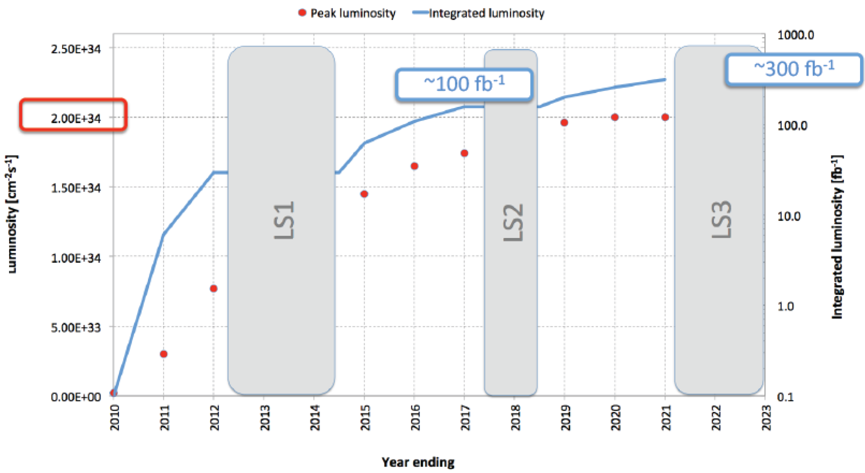
Details of ROC modifications see in the talk of Hans-Christian Kästli (PSI)
"Frontend Electronics development for the CMS pixel detector upgrade!", ***Pixel 2012, Inawashiro, JP***

Upgrade Phase I CMS Pixel Detector

Upgrade motivation

New Read-Out Chip needed that could efficiently function at $L > 1\times10^{34}$ cm^{-2} sec^{-1}

Detector	Radius (cm)	% Data loss for ($cm^{-2}s^{-1}$ @ ns) 1×10^{34} @ 25	2×10^{34} @ 25	2×10^{34} @ 50
Current detector				
BPIX1	4.4	4.0	16.0	50.0
BPIX2	7.3	1.5	5.8	18.2
BPIX3	10.2	0.7	3.0	9.3
FPIX1 and 2		0.7	3.0	9.3
Upgrade detector				
BPIX1	3.0	1.19	2.38	4.76
BPIX2	6.8	0.23	0.46	0.93
BPIX3	10.2	0.09	0.18	0.36
BPIX4	16.0	0.04	0.08	0.17



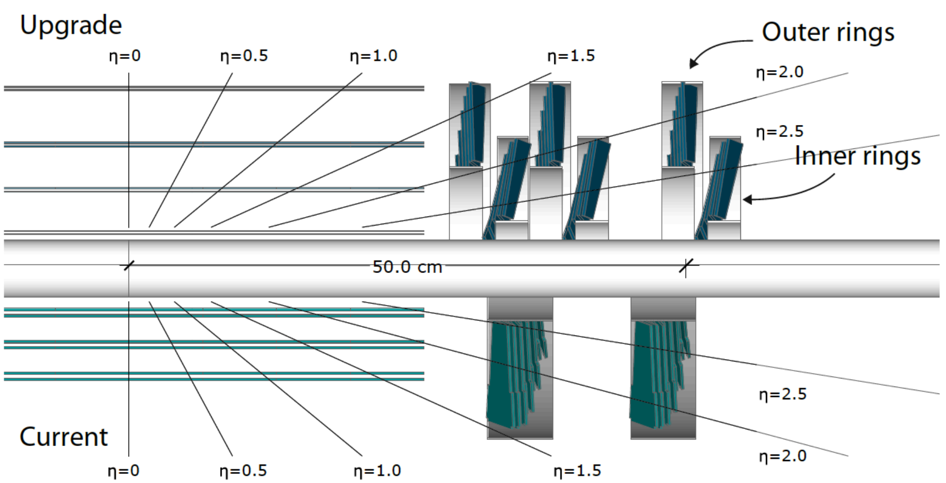
Already at the end of 2015 luminosity of $L=1.5\times10^{34}$ cm^{-2}sec^{-1} expected

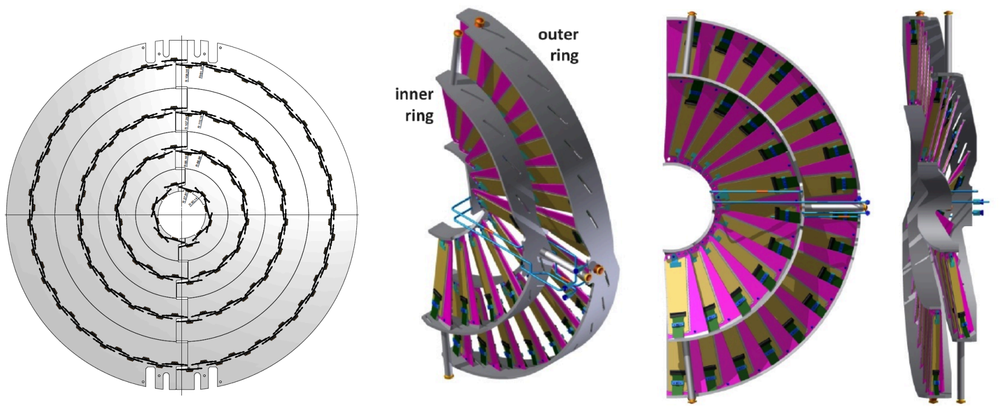
The detector need to be operational till LS3 (2022) at $L=2\times10^{34}$ cm^{-2}sec^{-1}

Upgrade pixel detector

- Upgrade Pixel detector: 4 barrel layers (instead of 3) and 3 forward disks on each side (instead of 2)
- Installation: during extended winter shutdown in 2016/17

Bpix: 1184 modules, 48M->79M pixels
L1 r= 30mm, 96 modules, 2×TBM09, 4 links
L2 r= 68mm, 224 modules, TBM09, 2 links
L3 r=109mm, 352 modules, TBM08, 1 link
L4 r=160mm, 512 modules, TBM08, 1 link
Fpix: 672 modules, 18M->45M pixels
3 Disks r=45-161mm, 6×112 modules, TBM08, 1 link
Outer ring rotated by 20° (turbine like)
Inner ring rotated by 20° and tilted by 12° with respect to IP

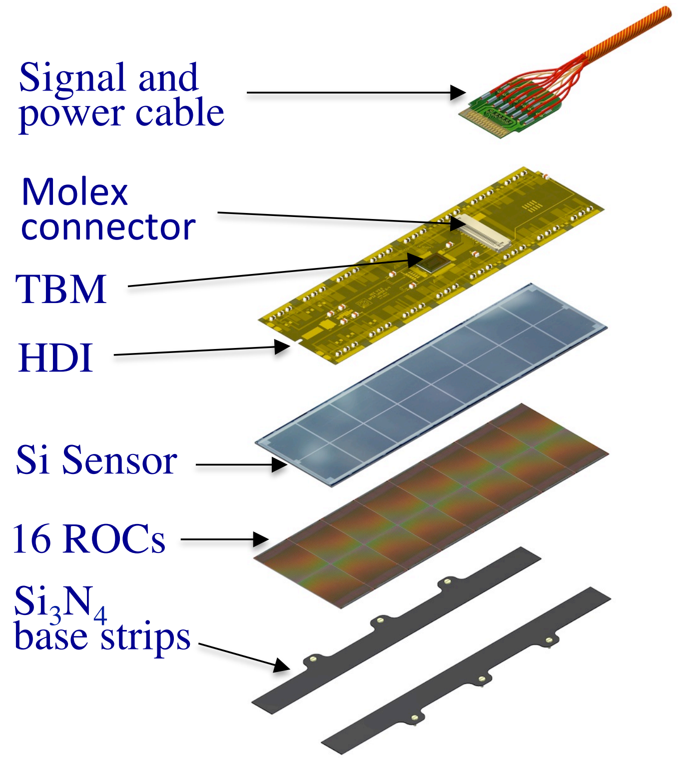




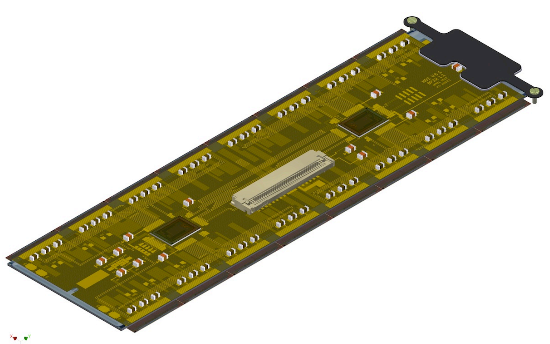
Pixel module

Module parameters:

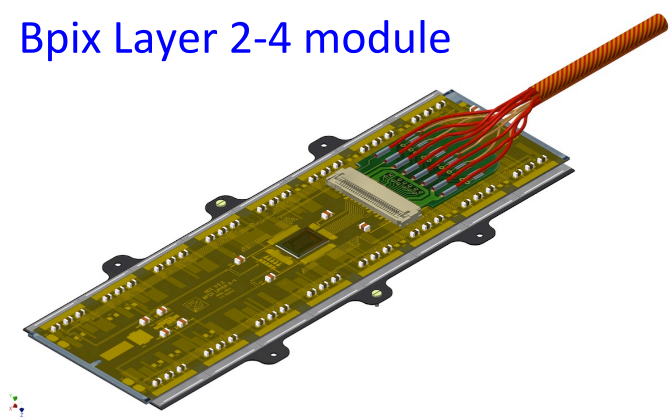
Full Size: 66.6 mm × 25/21.6 mm (L2-4/L1)
Sensor size: 66.6 mm × 18.8 mm
ROC size: 10.55 mm × 8.02mm
Weight: < 3 g
Si sensor thickness: 285 µm
ROC thickness: 75/175 µm (L1/L2-4)
Segmentation: 16 x 52 x 80 = 66560 pixels
Power: 2.0 W



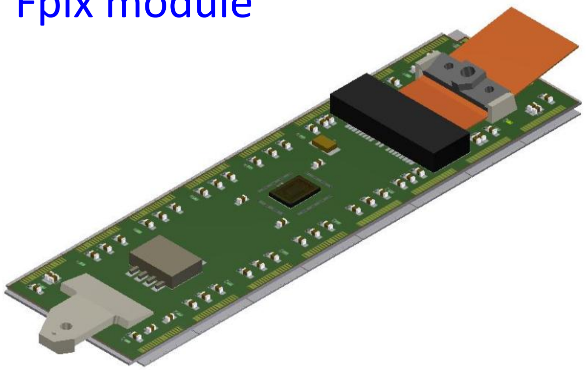
Bpix Layer 1 module



Bpix Layer 2-4 module



Fpix module



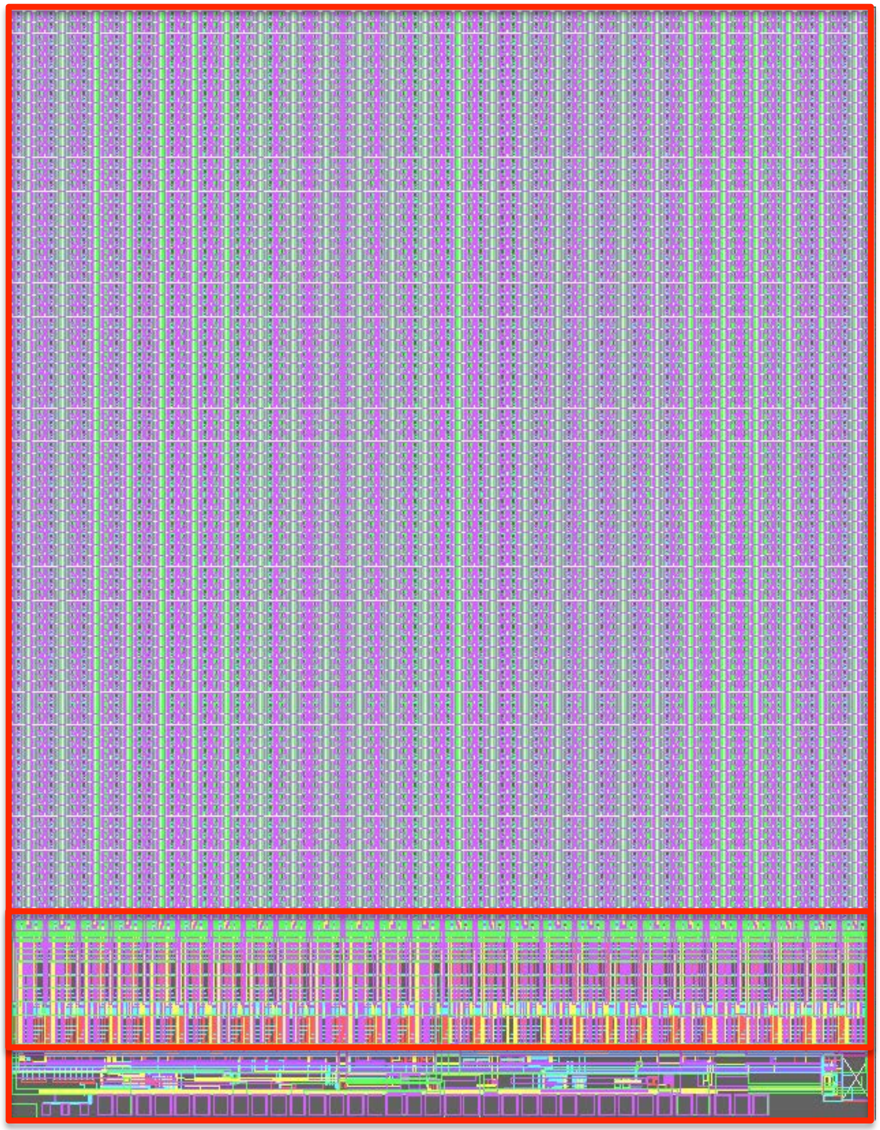
Upgrade Phase I Pixel Readout Chip

Upgrade Phase I ROC

- Based on present analog chip
- Limitations of present chip at Phase I
  1. Buffer sizes for level 1 trigger latency
     - ➢ Action: increase buffer sizes increased (next slide)
  2. Readout related dead time at higher data volumes
     - ➢ Action: additional readout buffer stage added
  3. Higher readout bandwidth needed for higher module number but the same number of fibers
     - ➢ Action: digital instead of analog readout with following modifications:
       - ✓ on chip ADC
       - ✓ new fast digital readout links
       - ✓ PLL to provide higher frequencies
       - ✓ modification to control logic
- Lower signal threshold required for extend longevity of detector

Layout of the Phase I ROC

(1)



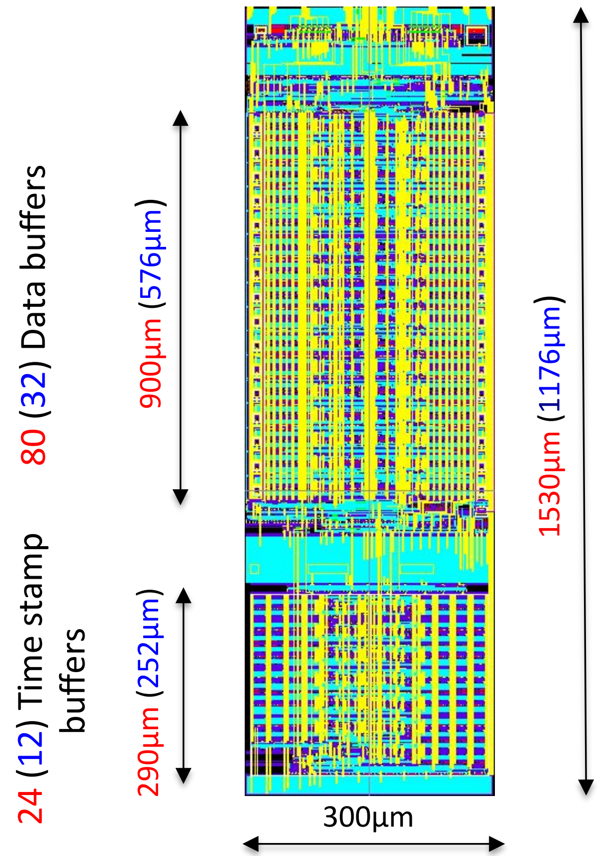
(2)

(3)

(1) Pixel array: 52 columns and 80 rows arranged in groups of 2 columns (26 double columns)

(2) 26 Double Column Interfaces

New ROC
Present ROC



(3) <u>Control Interface Block</u>: readout logic, DACs, I2C interface, voltage regulators, reference and pads

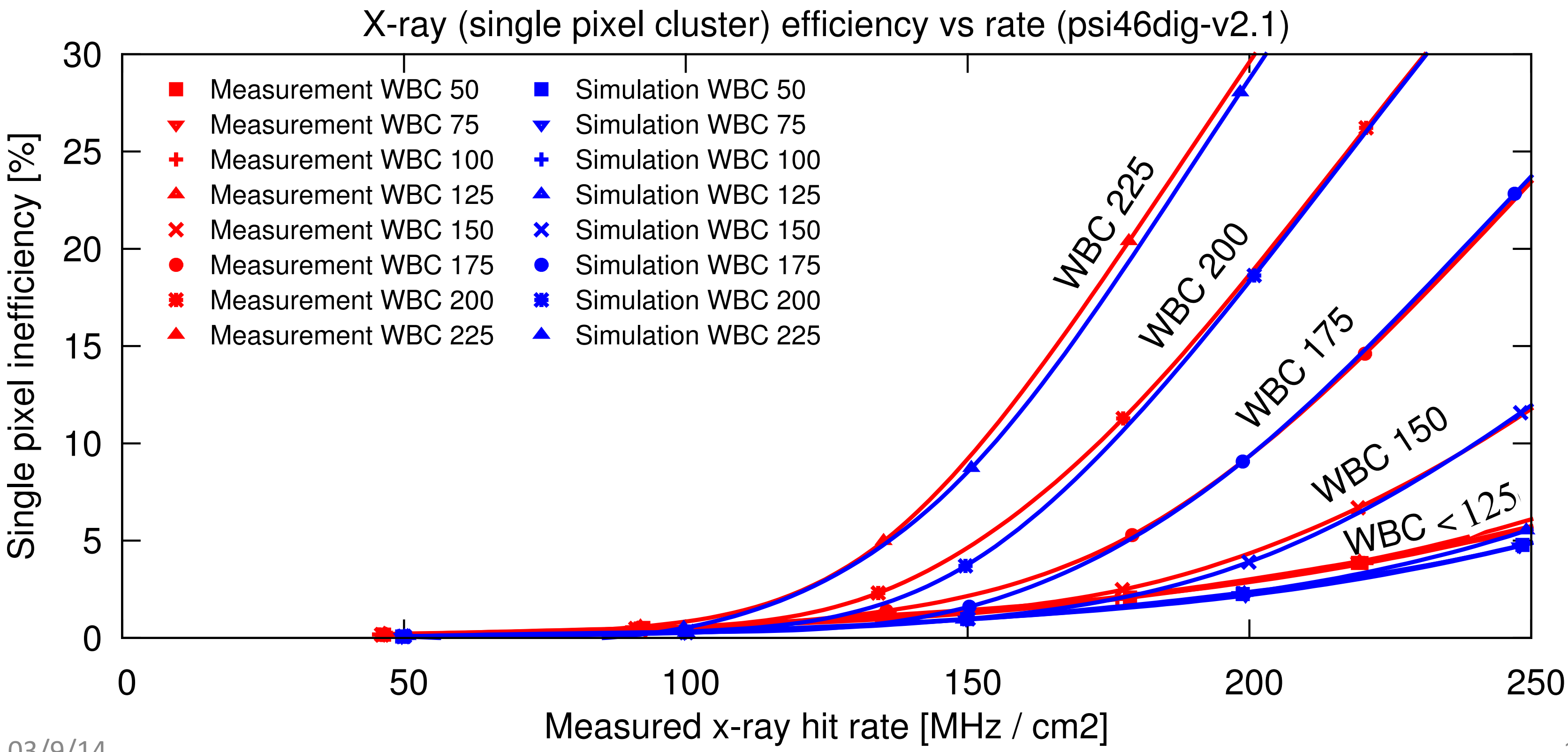
Analog vs digital ROC

	PSI46V2	PSI46DIG
ROC size	7.9 mm x 9.8 mm	7.9 mm x 10.2 mm
Pixel size	100 μm x 150 μm	100 μm x 150 μm
Smallest radius	4.3cm	2.9cm
Settable DACs / registers	26 / 2	19 / 2
Power Up condition	not defined	default values
pixel charge readout	analog	digitized, 8bit
Readout speed	40 MHz	160 Mbit/s
Time stamp Buffer size	12	24
Data Buffer size	32	80
Output Buffer FIFO	no	yes
Double column Speed	20 MHz	20 MHz (40 MHz)
Metal layers	5	6
Leakage current compensation	yes	no
in-time threshold	3500 e	$<$ 2000 e
PLL	no	yes
Data loss at max Operating flux	$\sim$3.8% at 120 MHz/cm^2	1.6% at 150 MHz/cm^2 ($\sim$3% at 580 MHz/cm^2)

High rate X-rays tests

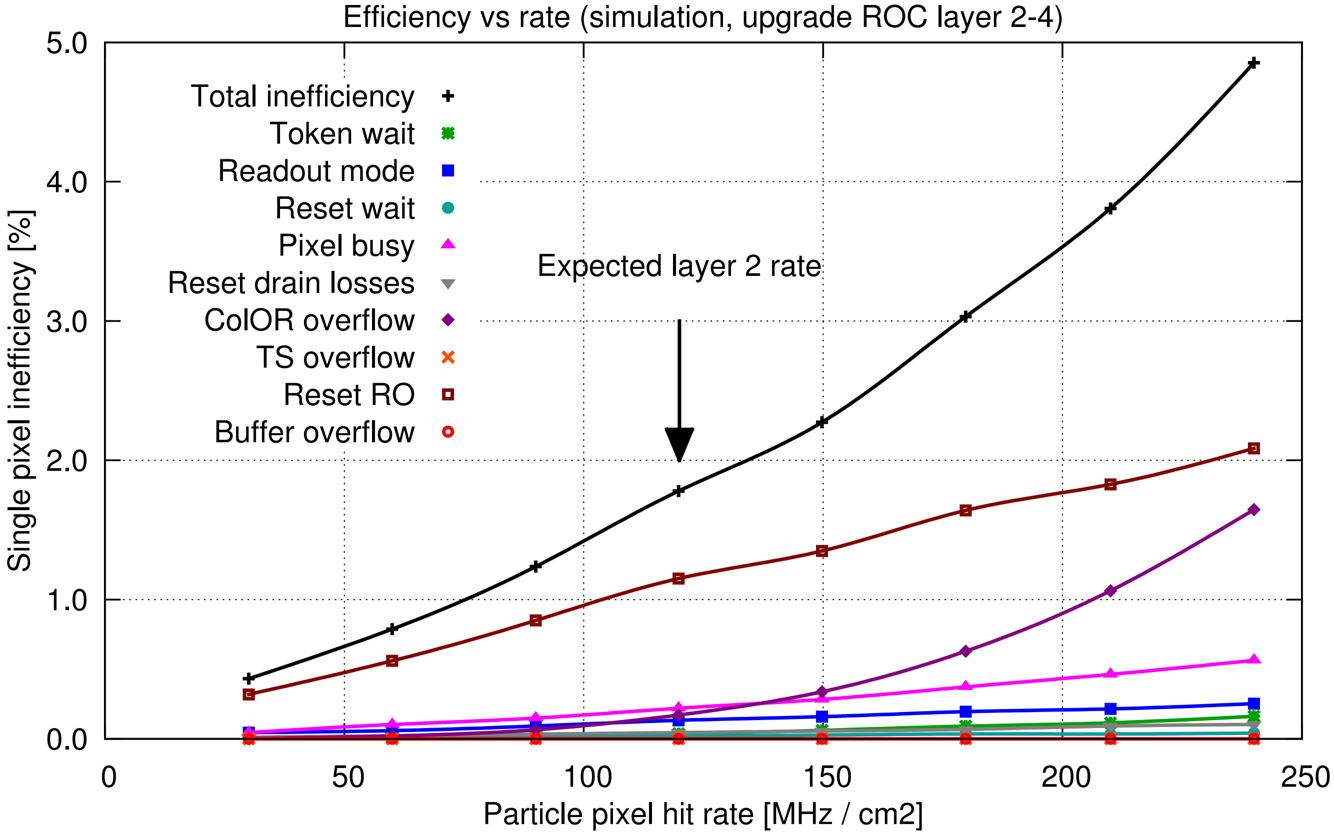
High rate X-rays: measurements vs simulation

- Definition: efficiency = (#readout calibrate signals) / (#injected calibrate signals)
- Periodic calibrate signal injection and trigger at rate of 30kHz
- X-ray inefficiency mostly due to limited time stamp buffer size
- Low WBC (CMS level 1 trigger latency) bypass this limitation
- Remaining inefficiency due to pixel busy and column drain



High rate particles: simulation

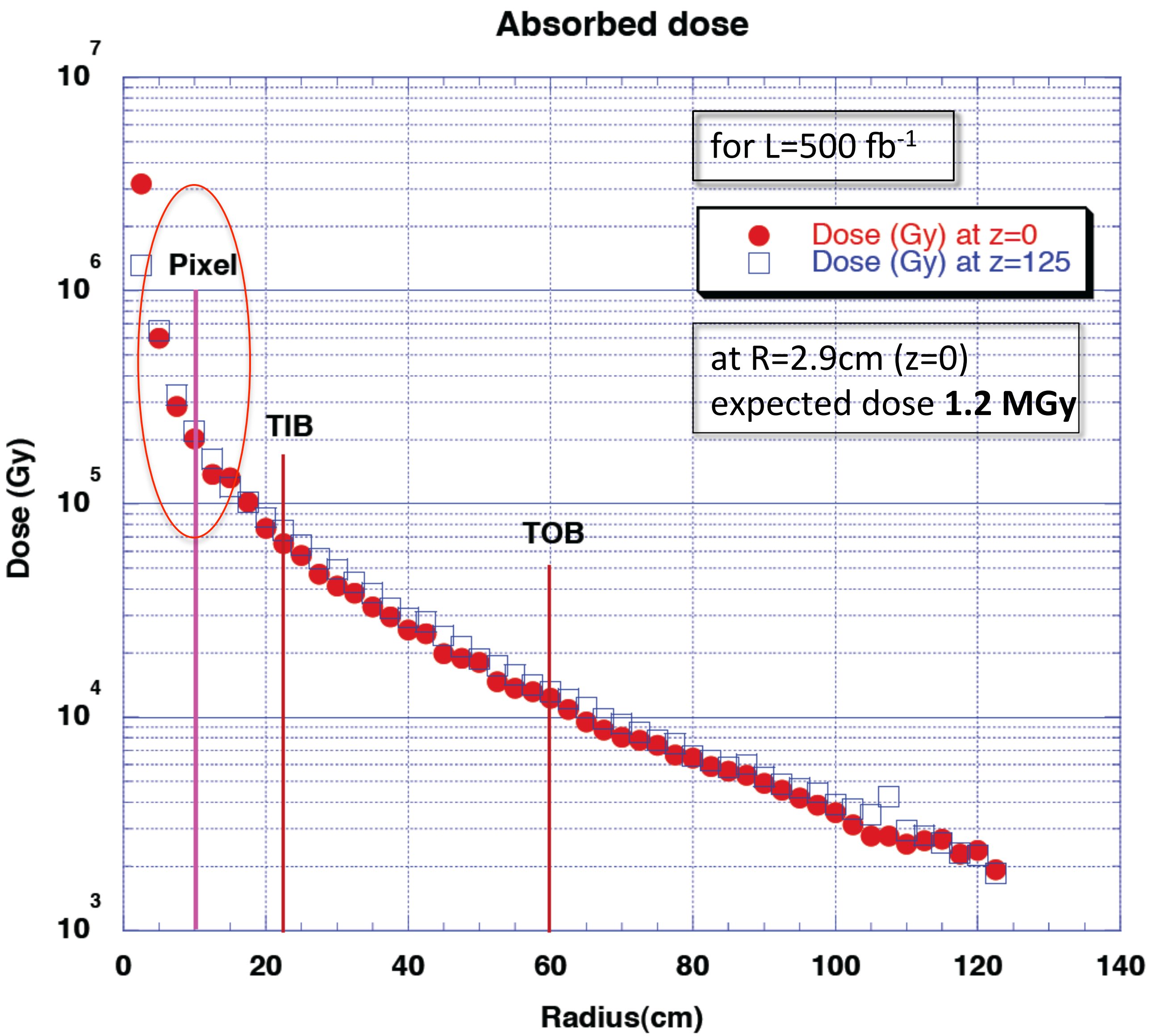
- Main difference with respect to X-ray
  - more hits per time stamp: 2.3 (particles) vs 1 (X-ray)
  - module readout simulated, not single ROC
  - random (non periodic) trigger used, hence more data loss mechanisms contribute
- WBC=156 (CMS level 1 trigger latency), random trigger at 100kHz rate
- Expected hit rate at R=6.8cm (Bpix Layer 2) – 120MHz/cm^2



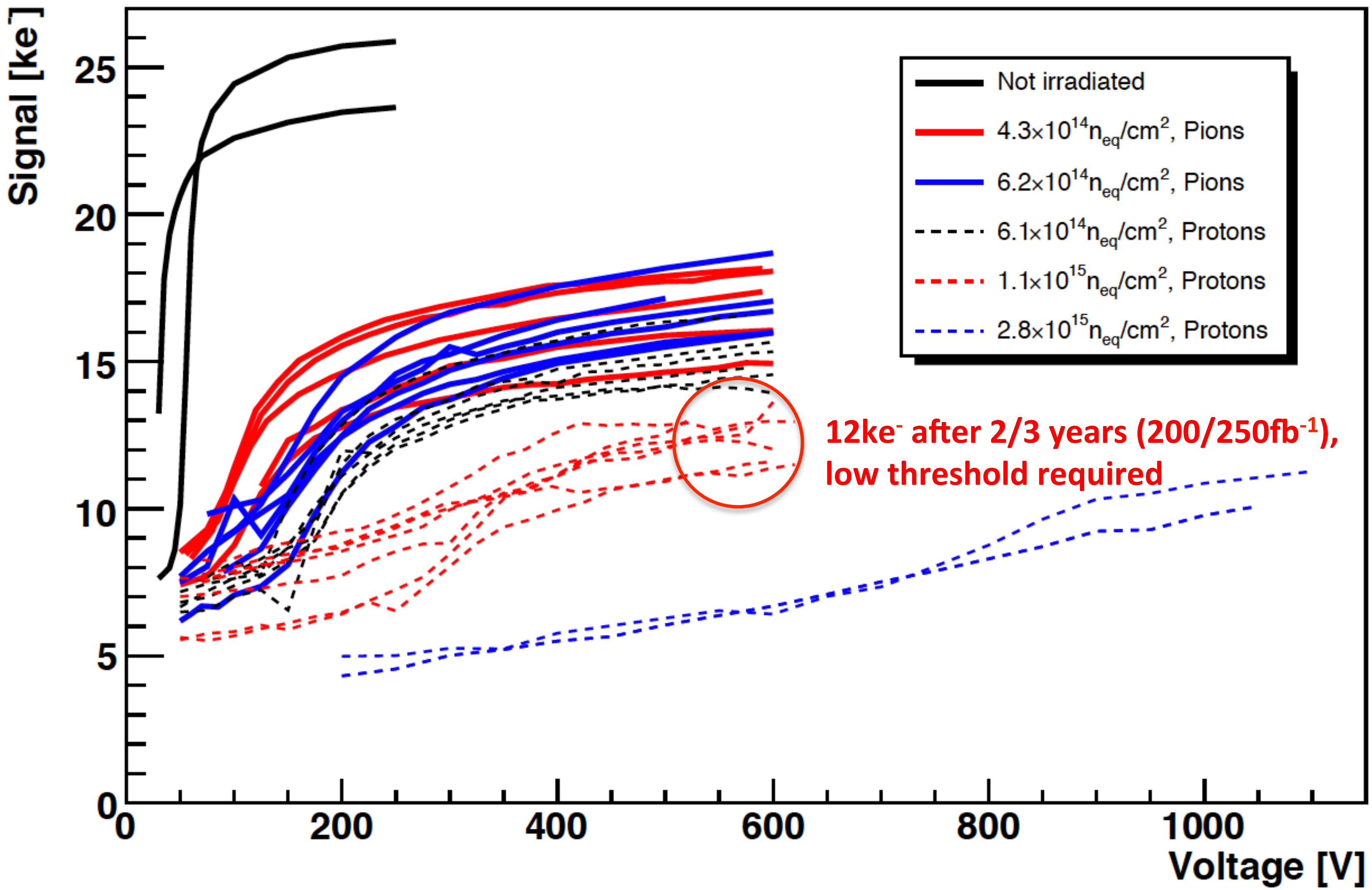
Irradiation studies

Acknowledgment:
The research leading to these results has received funding from the European Commission under the FP7 Research Infrastructures project AIDA, grant agreement no. 262025

Expected irradiation dose

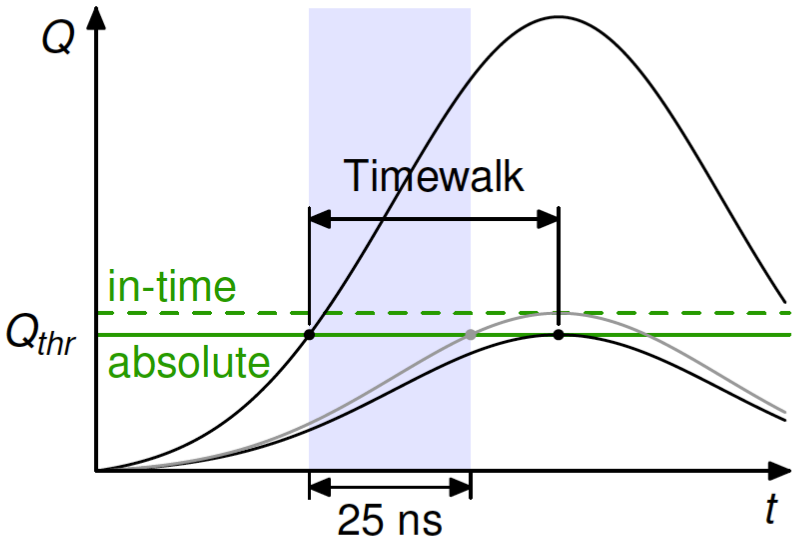


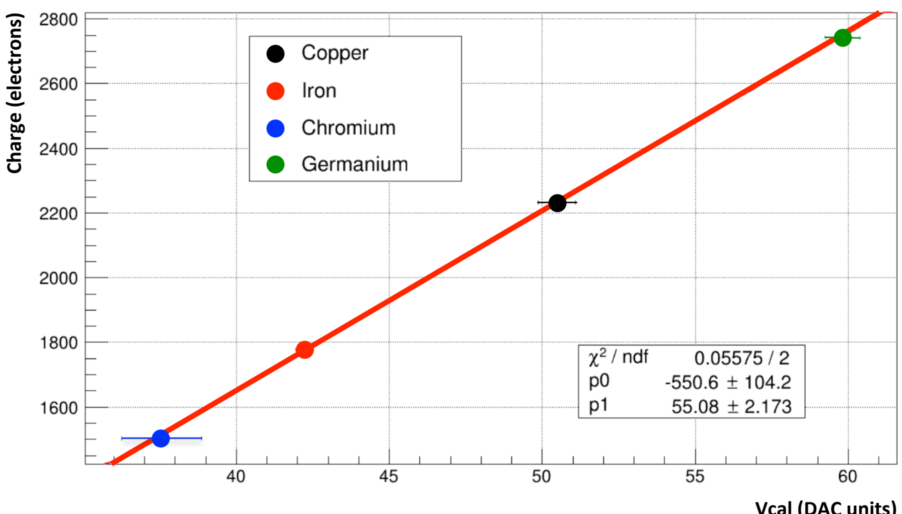
CCE in silicon

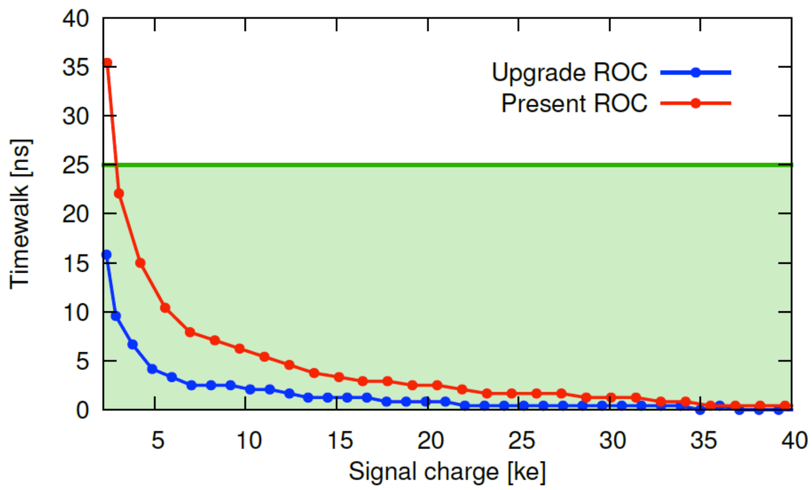


Timewalk and threshold

- Timewalk(T_{TM}): time difference between moments at which largest and lowest signals cross ROC threshold
  - analog ROC: T_{TM}>25ns
  - digital ROC: T_{TM}<16ns
- Minimum threshold:
  - analog ROC: 3200e$^-$
  - digital ROC: <1800e$^-$ (also due to reduced x-talk in new ROC layout)
- Low threshold increases detector longevity



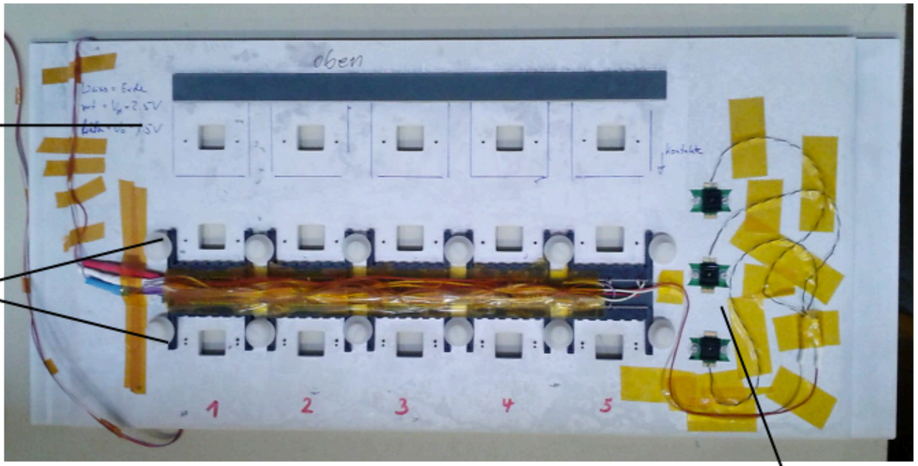




Irradiation at KIT: samples and dose

- Irradiation done
  - with proton beam, proton energy 23 MeV
  - at two doses: 60Mrad (2×10^{14}p/cm^2) and 120Mrad (4×10^{14}p/cm^2)
- 6 samples irradiated at each dose
  - 4 samples powered and 2 - not during irradiation

Irradiation setup

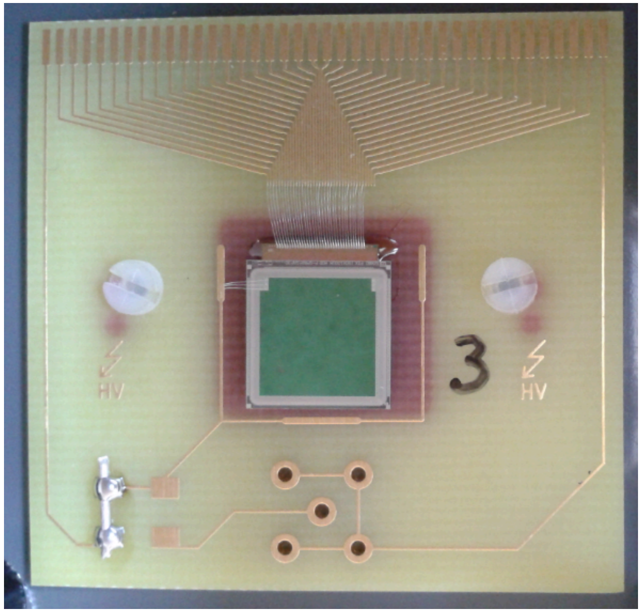


no power

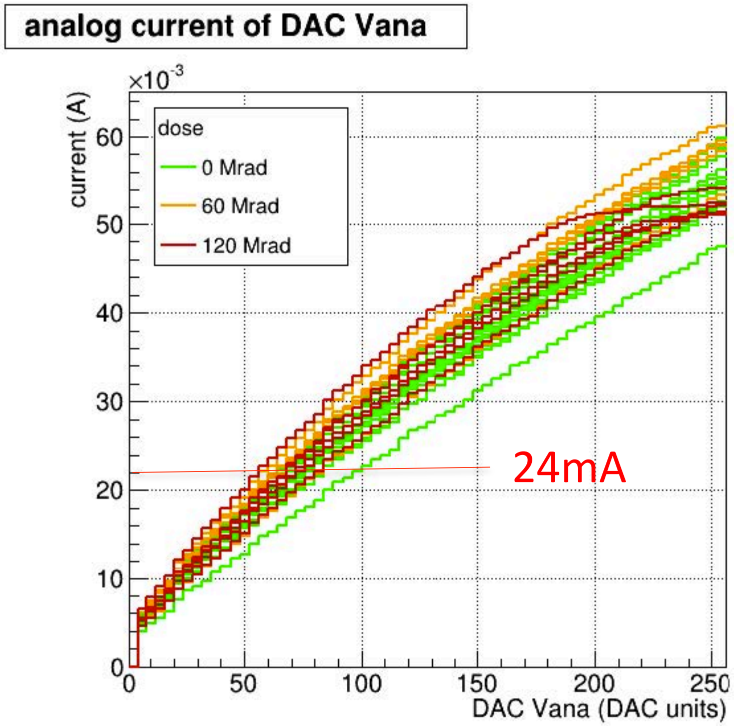
Power during irradiation

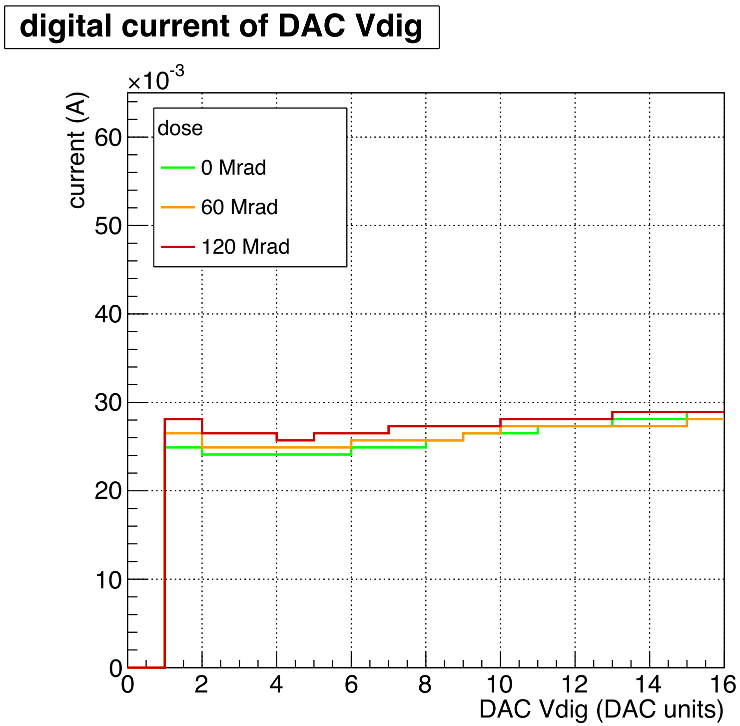
3 test structures

Irradiated sample



Analog and digital current

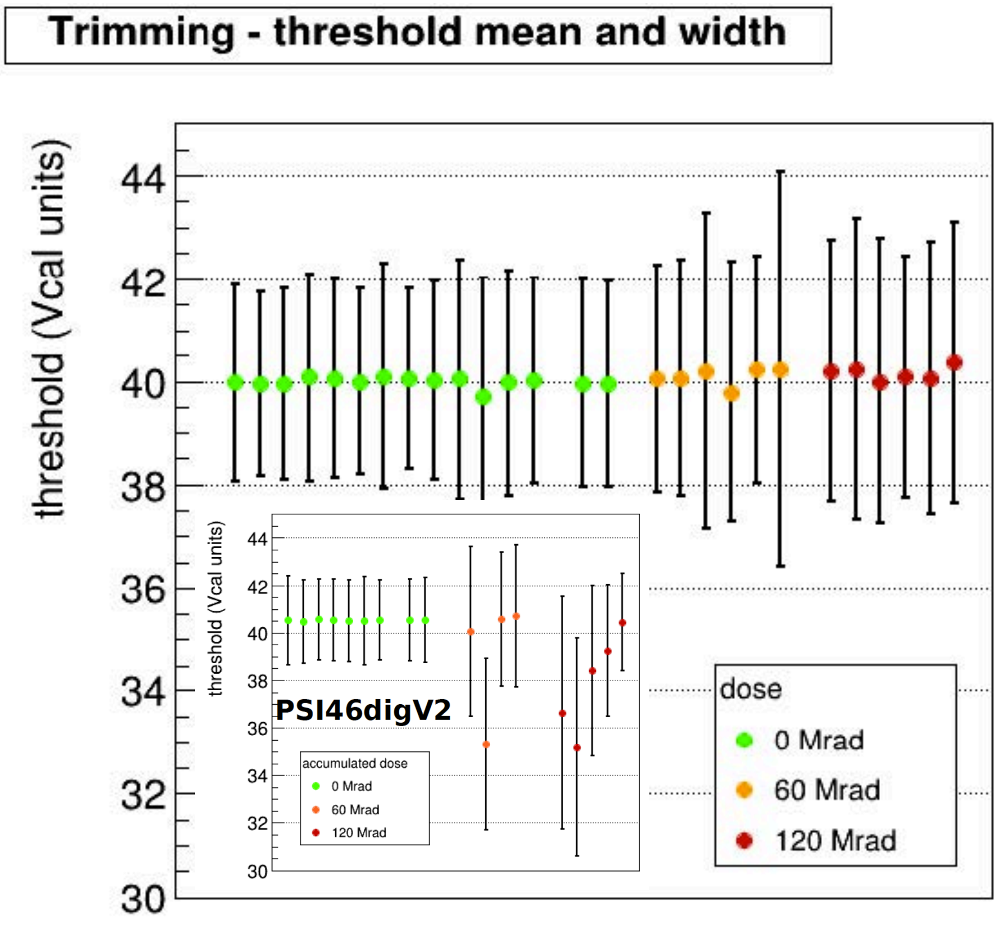




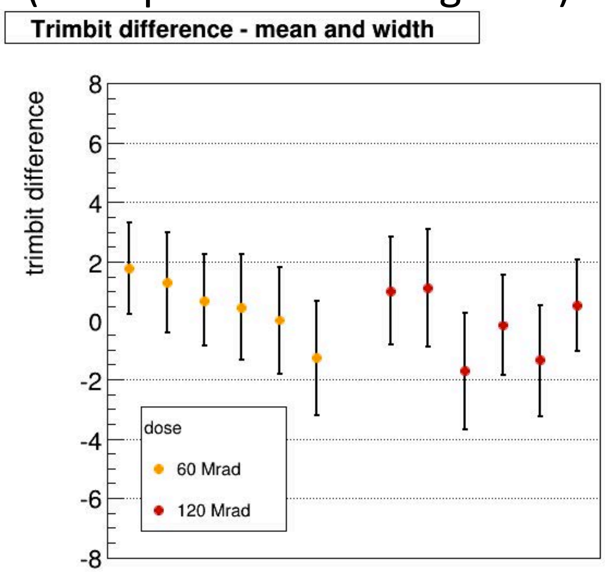
- Dynamic range of **Vana** DAC before and after irradiation is fine
- Minor increase of **Iana** after irradiation
- For several samples irradiated to 120MRad observed current saturation above **Vana**=170

- Small dependence of **Idig** vs **Vdig** DAC, as expected
- Remains the same after irradiation

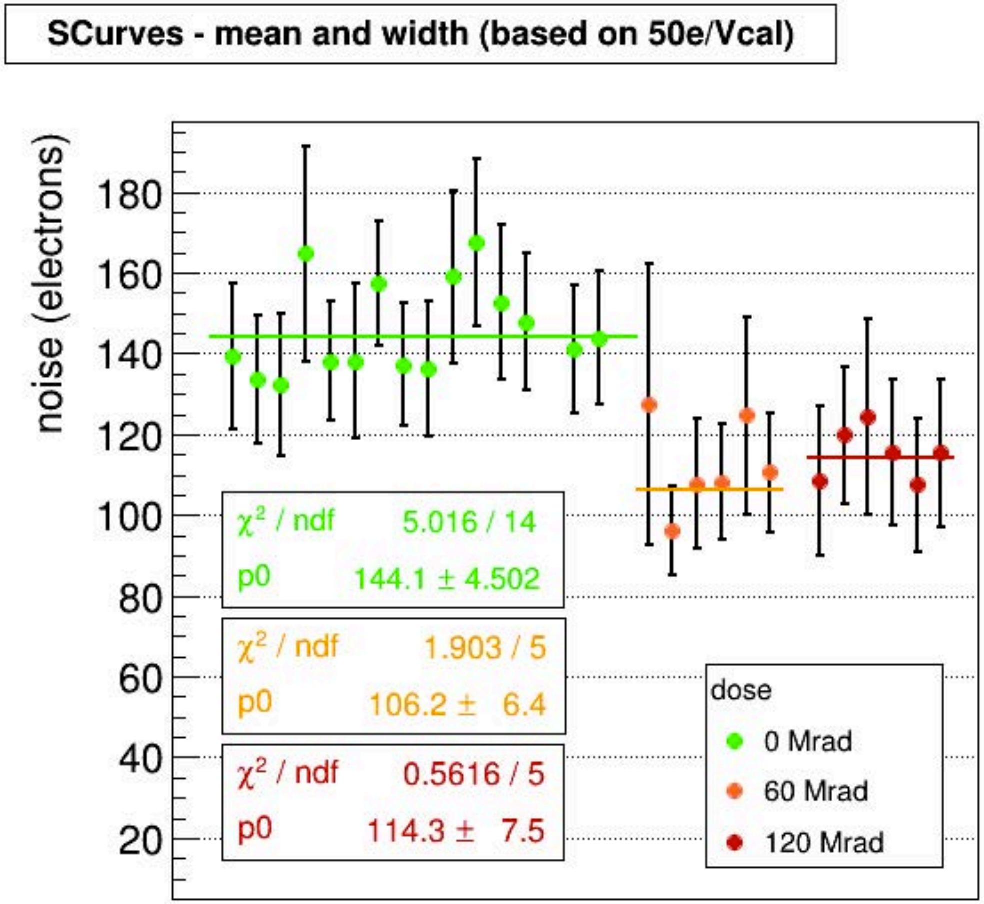
Trimming: Vcal threshold and trim bits



NB: **PSI46digV2** – previous version of the final chip, shown for comparison

- Before and after irradiation ROC trimmed to (internal calibrate signal) **Vcal**=40
- Trimming works well before and after irradiation
- Small increase (30%) of threshold spread within ROC observed
- After irradiation mean of trim bit distributions shifts slightly around 0 (both positive and negative)
- 

Noise



- Average noise
  - before irradiation – 144 ± 5e$^-$
  - after 60 Mrad – 106 ± 6e$^-$
  - after 120 Mrad – 114 ± 8e$^-$
- Used conversion factor 50e$^-$/**Vcal**
- Conversion factor after irradiation is not known
- Noise spread among pixels in ROC stays almost the same

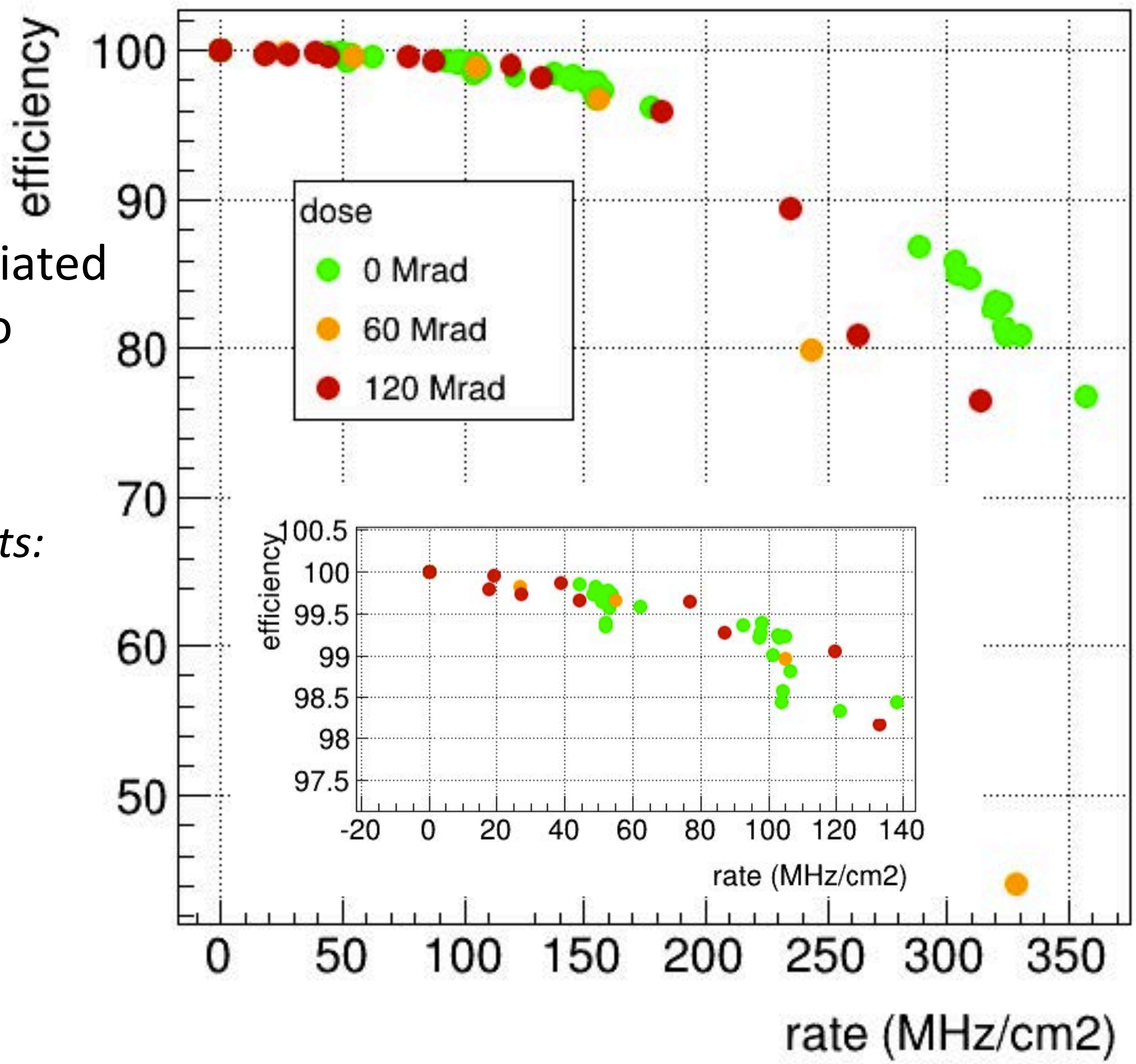
Pixel efficiency with high rate Xrays

Efficiency at 120MHz/cm^2

- measured with Xrays
- higher than 98.5% and
- stays the same for non irradiated and irradiated samples up to 120MRad

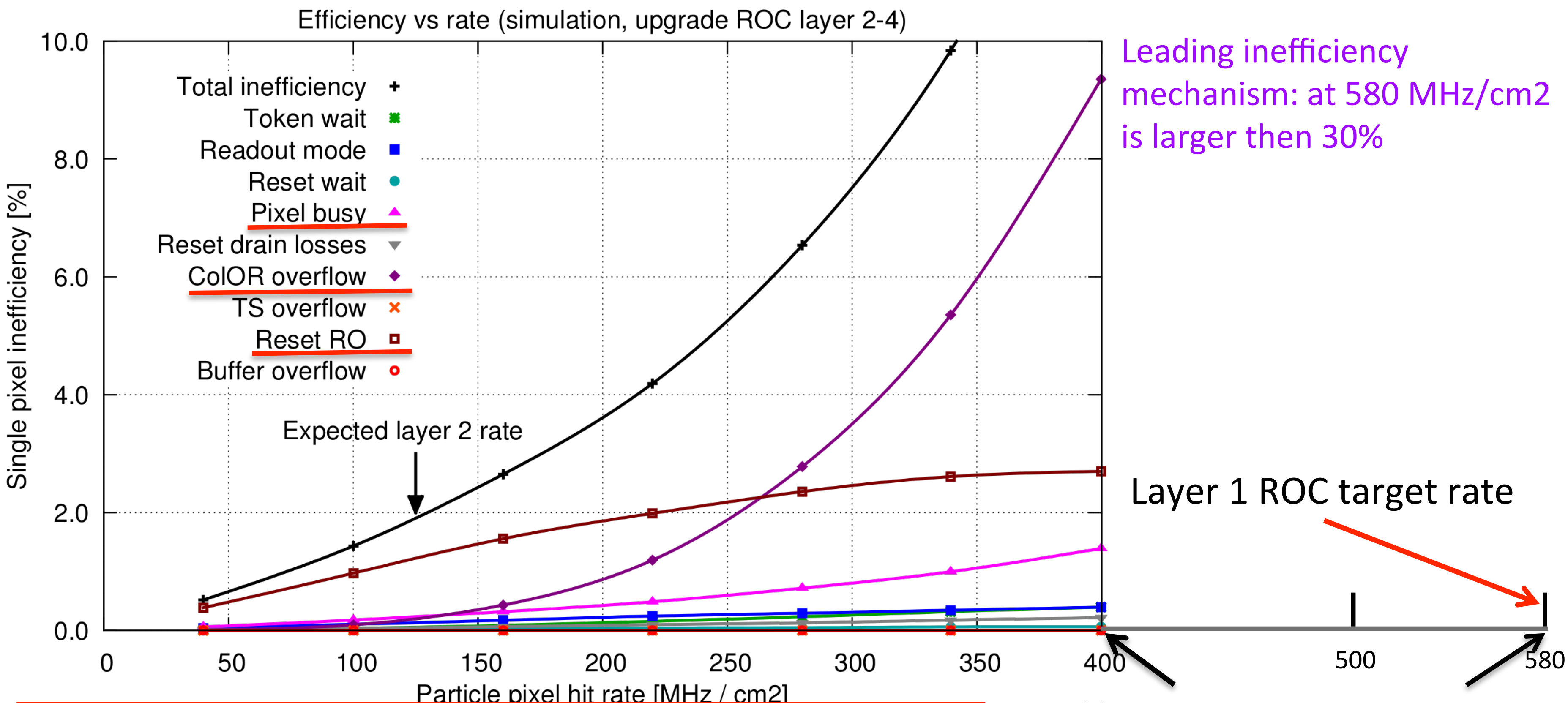
NB

Not the best possible measurements: for Dose=0 VIColOr DAC was not optimized



Layer I ROC

Bpix Layer 1 ROC



$r^{-1.3}$ low as measured at P5

$r^{-1.8}$ low as simulated by PYTHIA

Main mechanisms of data losses addressed in the design:

1. pixel busy
2. ColOR overflow
3. readout reset

Bpix Layer 1 ROC status

- Double column logic needed modifications for higher data rates
- Hence Dynamic Cluster Column Drain architecture implemented
  - dynamic cluster (2×2 pixels) finding in double column
  - transfer speed increased from 20MHz to 40MHz
  - data throughput in double column improved by factor of 3.5
  - pixel dead time (pixel busy) reduced to 1.3%
  - column busy (leading) inefficiency completely gone
- Dead time free data buffer management (reset RO)
  - buffer logic improved mechanism to protect valid hits from overwriting
  - related data loss reduced by at least factor of 5

Data loss mechanisms in Upgrade ROC for layer 1

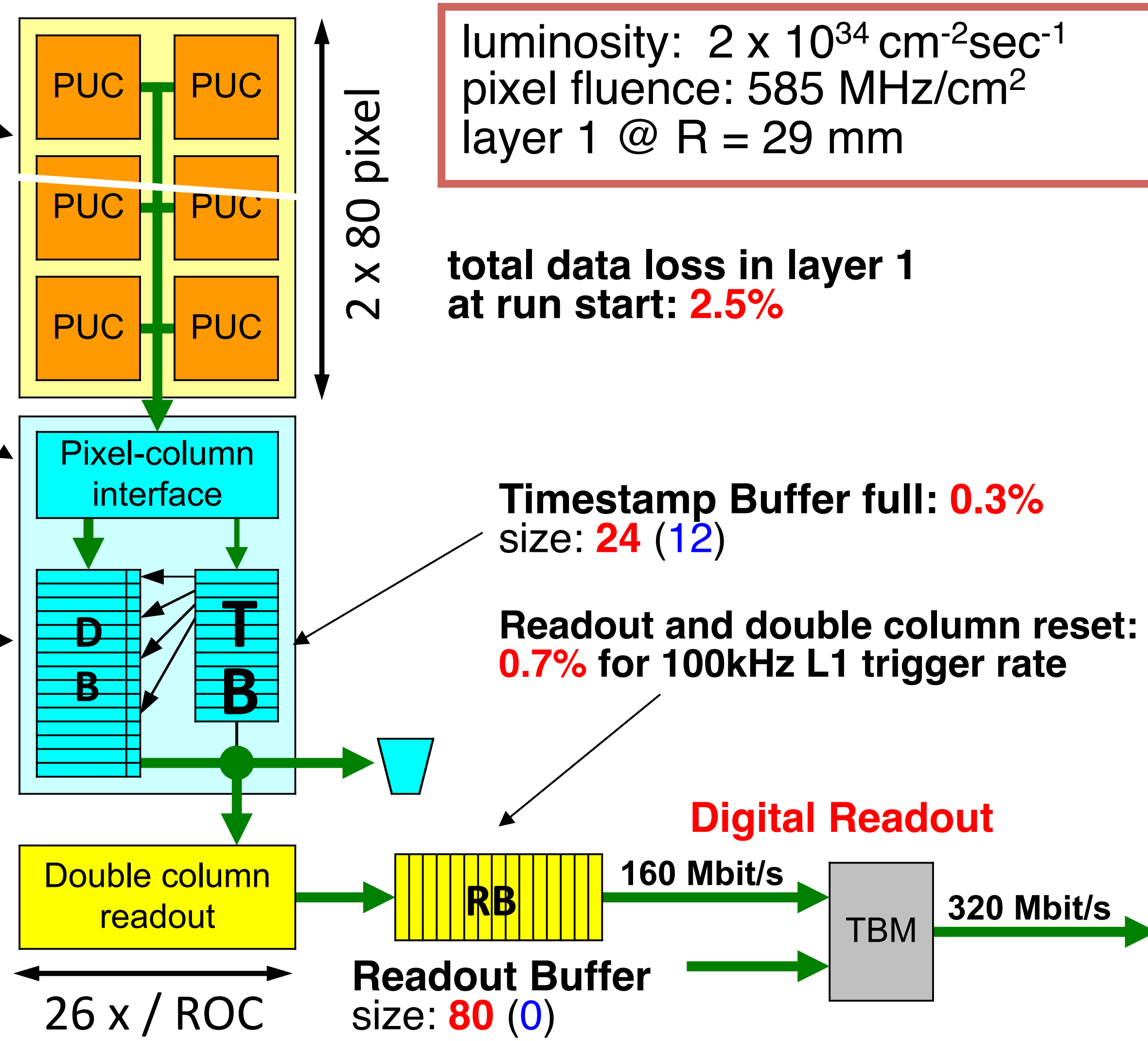
luminosity: 2 x 10^{34} $cm^{-2}sec^{-1}$
pixel fluence: 585 MHz/cm^2
layer 1 @ R = 29 mm

total data loss in layer 1 at run start: 2.5%

Pixel busy: 1.3%
pixel insensitive until hit transferred to data buffer (column drain mechanism)

Double column busy: 0.2%
Column drain finds hit pixels and transfers hits from pixel to data buffer. Maximum 7 pending column drains requests accepted

Data Buffer full: 0.0%
size: **80** (32)



Bpix Layer 1 ROC status

- Chip size almost the same as for Layer 2-4 ROC (PSI46digV2.1)
- Pads and data format the same as for PSI46digV2.1
- Power consumption the same or lower than for PSI46digV2.1
- **Submission at the end of 2014**

Conclusion

- After three iterations (2012-2014) and thorough investigations in labs, beam tests and irradiation ROC for Bpix Layer 2-4 and Fpix works as expected
- Signal threshold could be set as low as 1800e^- (compare with present ROC of 3200e^-)
- Hit efficiency (measured with X-rays and simulated for X-rays and particles) is higher than 98% at expected hit rate (120MHz/cm^2) for Bpix Layer 2 even after irradiation of 120MRad
- Production submission is done in July 2014 (48 wafers, the rest will be produced at the end of 2014)
- Design of Bpix Layer 1 ROC is almost done and submission for production is planned at the end 2014

Acknowledgment

In this presentation work of many people from the CMS Pixel Upgrade Phase I community is used. I would like to thank all of them. Special thank to

Hans-Chritian Kästly (PSI)

Beat Meier (PSI)

Jan Hoss (ETHZ)

Marco Rossini (ETHZ)

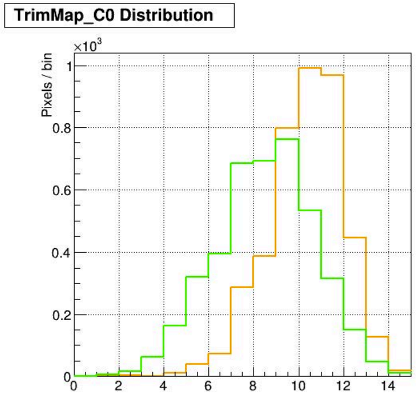
Tilman Rohe (PSI)

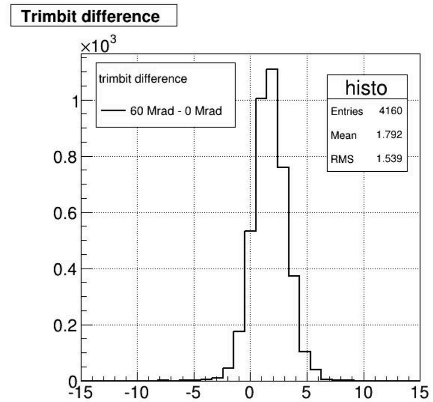
Silvan Streuli (PSI)

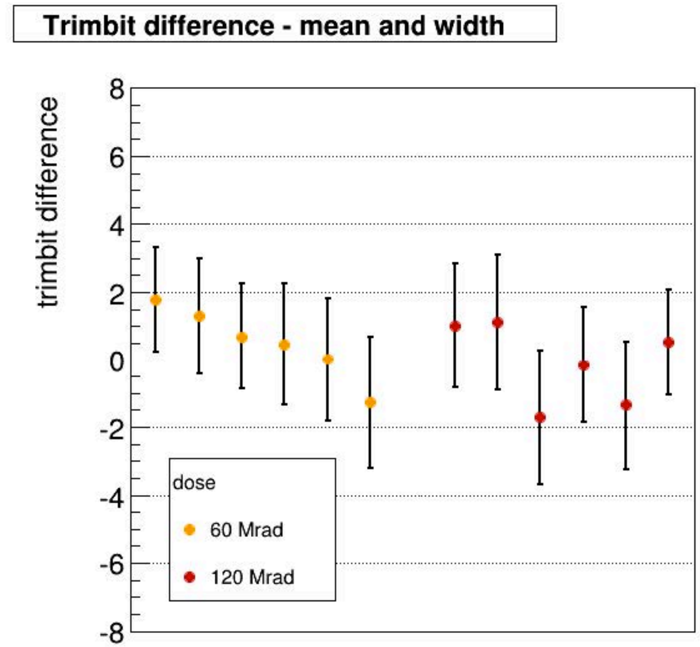
Jackson Young (Uni of Kansas)

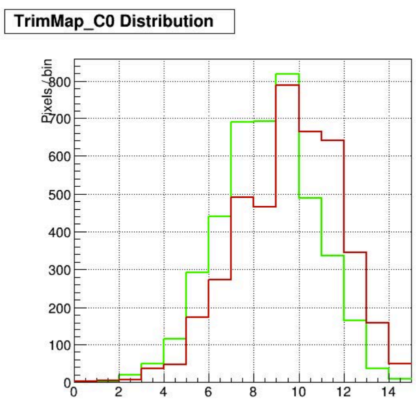
Backup slides

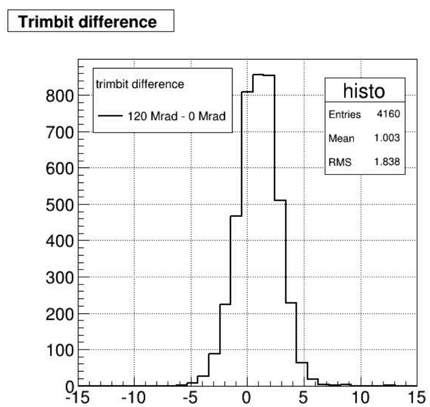
Trimming: trim bits







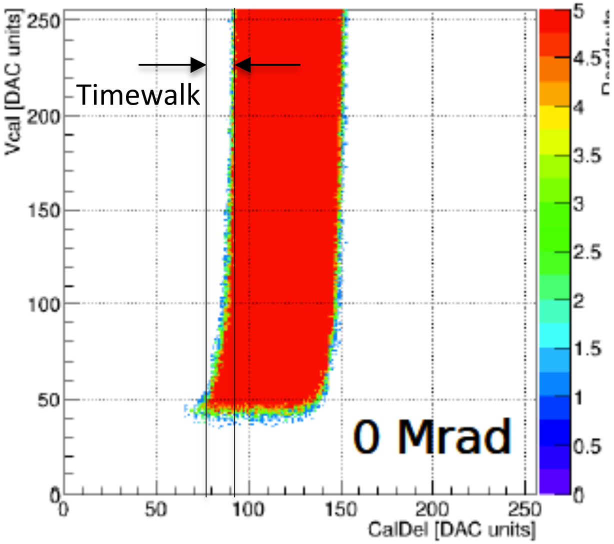


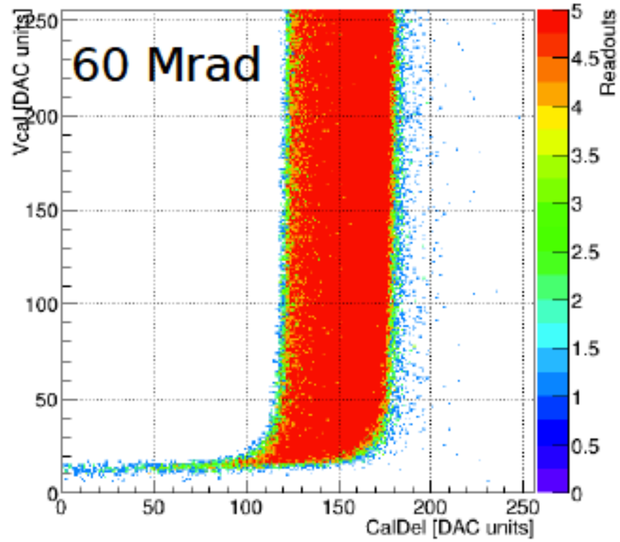


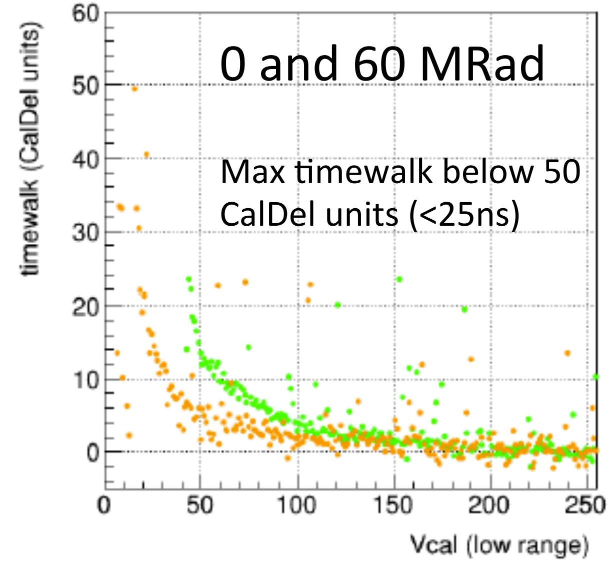
Reproducibility: mean=0.1; RMS=0.6

- After irradiation mean of trim bit distributions shifts around 0 (both positive and negative)
- This may mean increase of trim bits non linearity (to be checked)
- Degradation of pixel threshold uniformity after irradiation to be checked

Timewalk







VcalCalDel_c5r5_C0

VcalCalDel_c5r5_C0

timewalk