Qualification of the CMS pixel readout chip for the phase 1 upgrade

Marco Rossini
on behalf of the CMS collaboration

Institute for Particle Physics, ETH Zürich

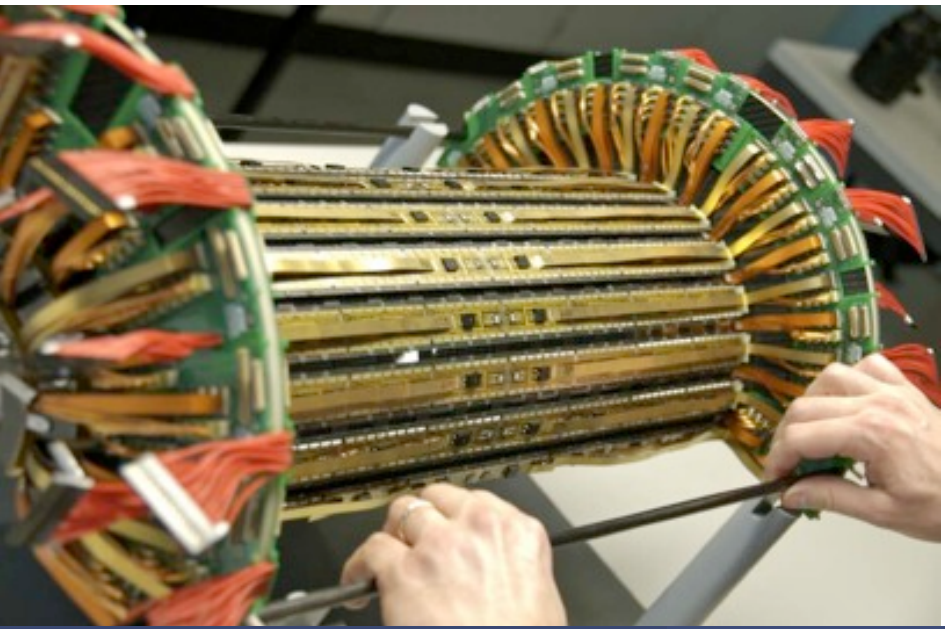
4. September 2013

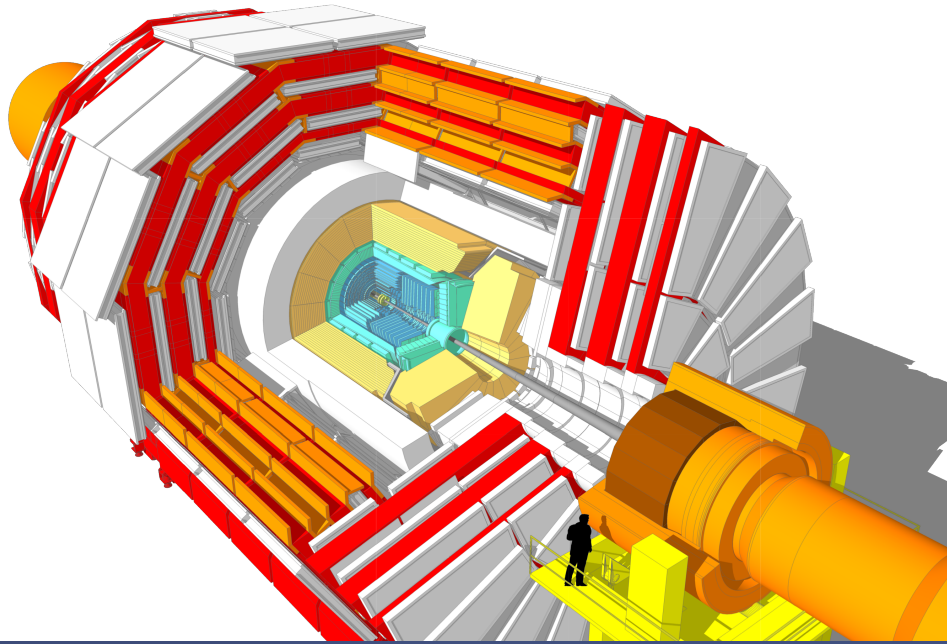
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

The CMS pixel detector

The pixel detector is installed at the core of CMS

- 3 pixel hits for $\eta < 2.1$, 3 barrel layers (BPIX), 2 endcaps (FPIX)
- 66 M channels, 98 % still working
- Power consumption of 3.5 kW
- BPIX $r = 4.4, 7.3, 10.2$ cm, FPIX $z = 34.5, 46.5$ cm
- 100×150 μm pixels, achieved resolution $r\phi$: 12.8 μm, z : 24 μm

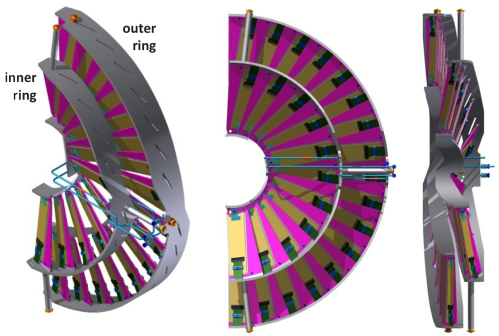




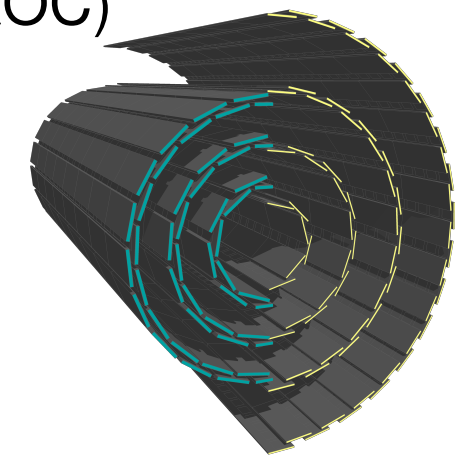
The pixel detector upgrade

Changes to the detector in the phase 1 upgrade include:

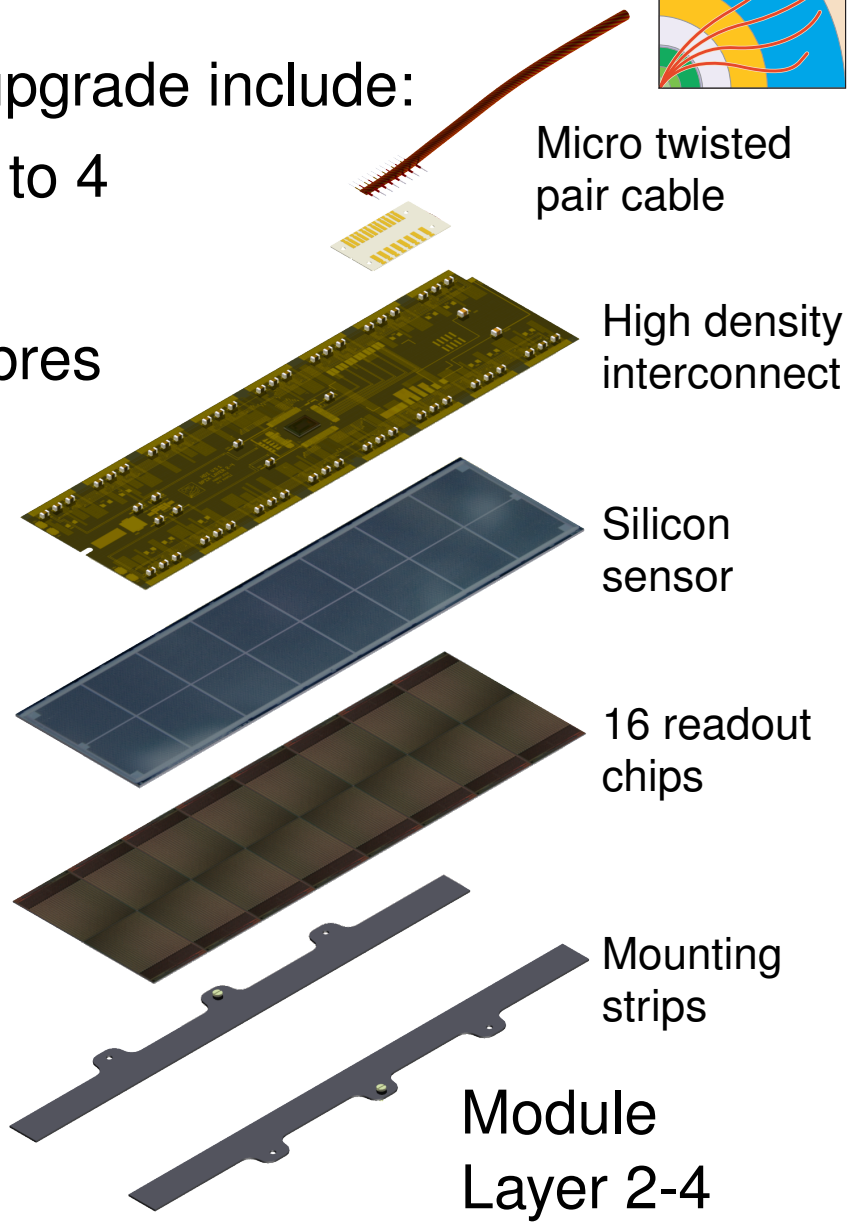
- Increase number of pixel hits from 3 to 4
- Innermost layer at $r = 2.95$ cm
- Re-use power cables and readout fibres
- Ensure operation at $\mathcal{L} = 2 \cdot 10^{34}$
- Upgrade of the front end electronics (readout chip/ROC)



New endcap disk design



Addition of one barrel layer

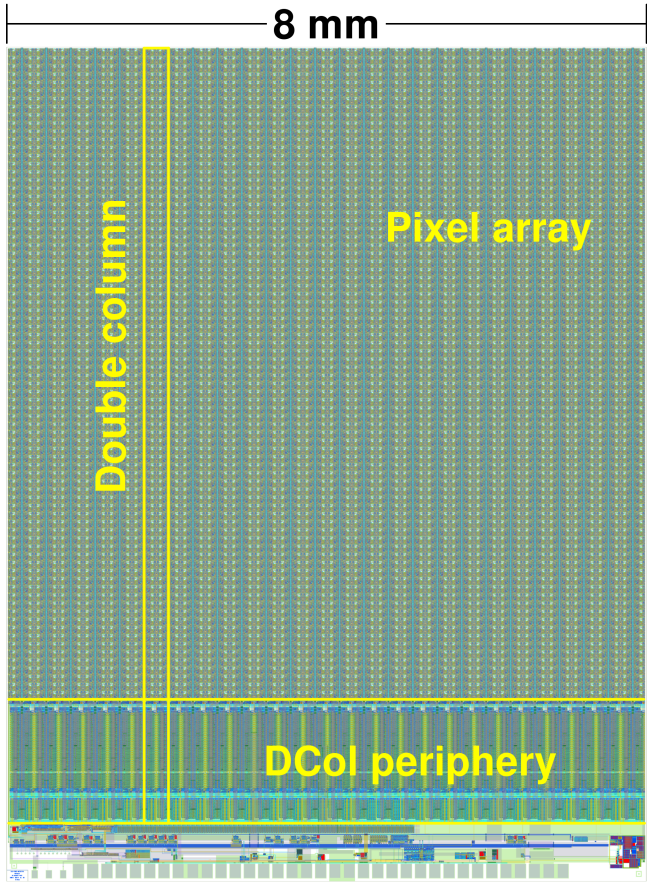


Module Layer 2-4

The present pixel readout chip

The current architecture has the following properties:

- 4160 pixels, bump-bonded to silicon sensor
- Zero suppressed signal charge readout
- Pairs of columns operate independently
- Each double column has a drain mechanism and buffers
- 40 MHz operation, trigger latency 3.9 μs
- Discarding of data that is not validated by the trigger
- Trigger verified hits readout via token passage
- Power consumption: 140 mW



Motivation for the upgrade of the front end electronics

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- Ensure efficient readout at 4-5 times the present hit rate
- Enable readout of increased number of modules with fibres from present 3 layer detector
- Improve lifetime of irradiated layers through higher charge sensitivity

Changes in the ROC design

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Maintaining efficiency at high rates:

- buffer cell size reduction to increase buffer capacity
- addition of a readout buffer to reduce dead time

Increase bandwidth:

- Change to 160 MHz digital readout with PLL
- Use low power 8 bit ADC for signal charge readout

Improve charge sensitivity:

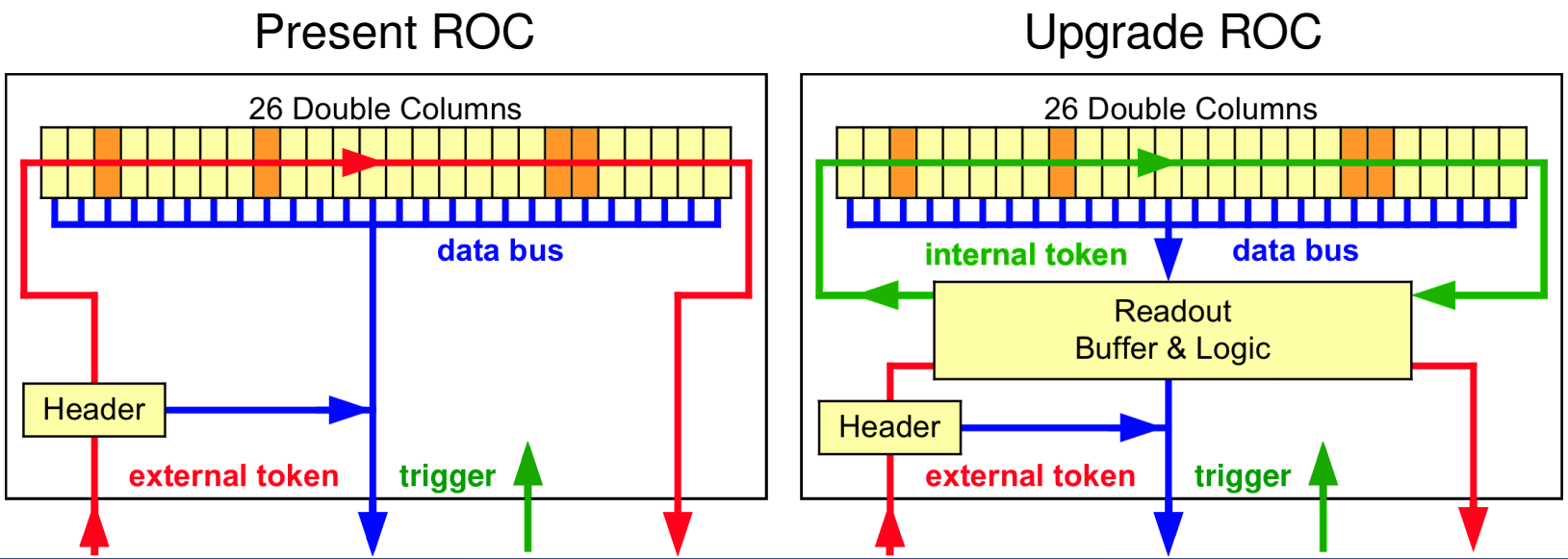
- threshold comparator redesign to reduce the timewalk
- layout changes to increase uniformity and reduce cross talk

Other changes:

- Startup circuit to initializes the ROC registers
- Readback of programmed chip parameters

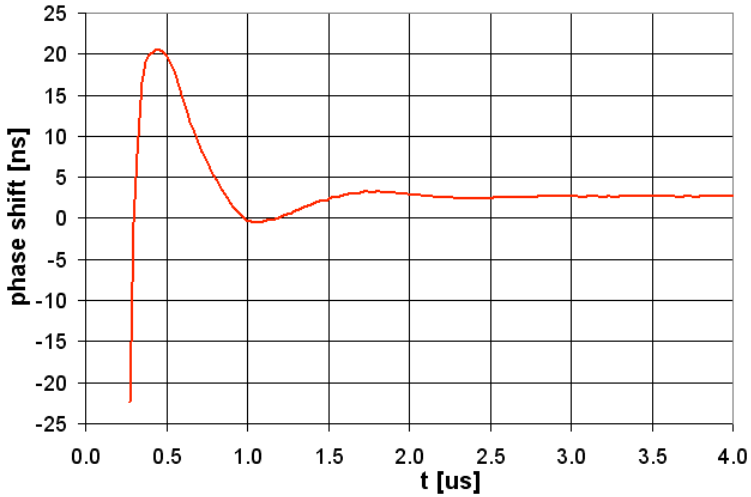
Adapting internal storage for 4-5 times higher data rates

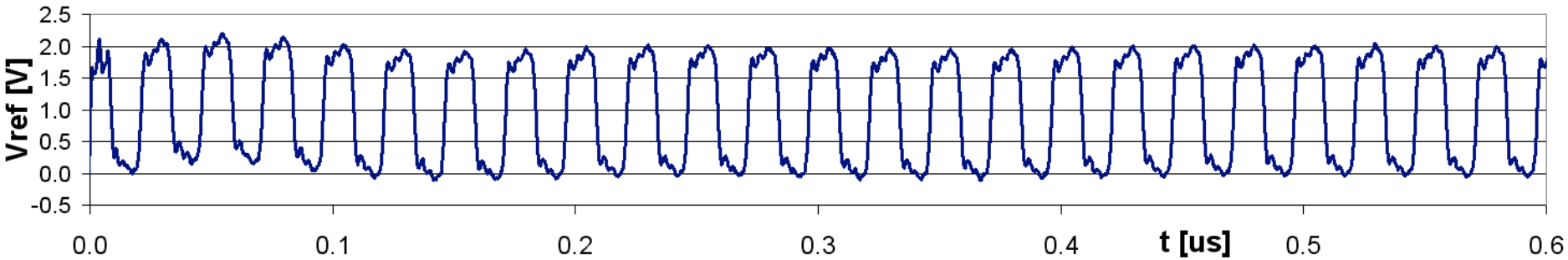
- Increased timestamp buffer size from 12 to 24
- Increased data buffer size from 32 to 80
- Buffer size determined through Pythia and GEANT based simulations
- Added readout buffer with 64 cells to deal with trigger validated DC waiting for readout token

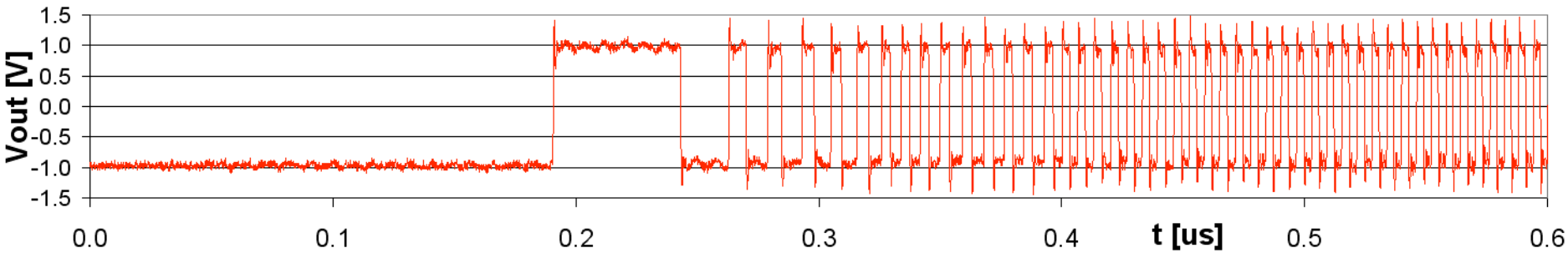


PLL performance

- Converts 40 MHz to 160 MHz
- Locks onto frequencies from 10 to 75 MHz
- Output clock jitter < 3 ps
- Operating temperature -20 to $20\,^{\circ}$C

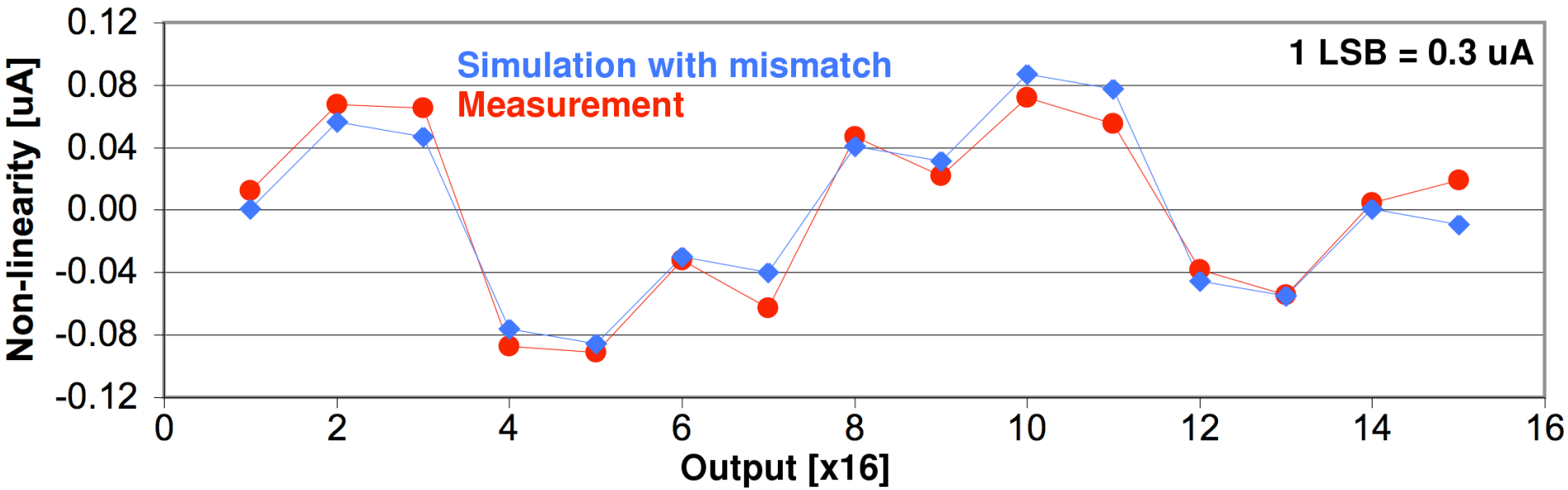






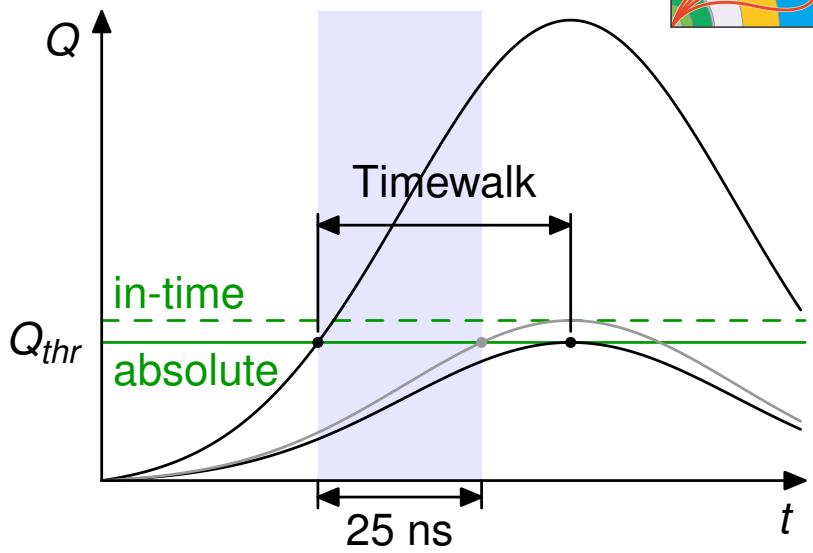
Pulse height ADC performance

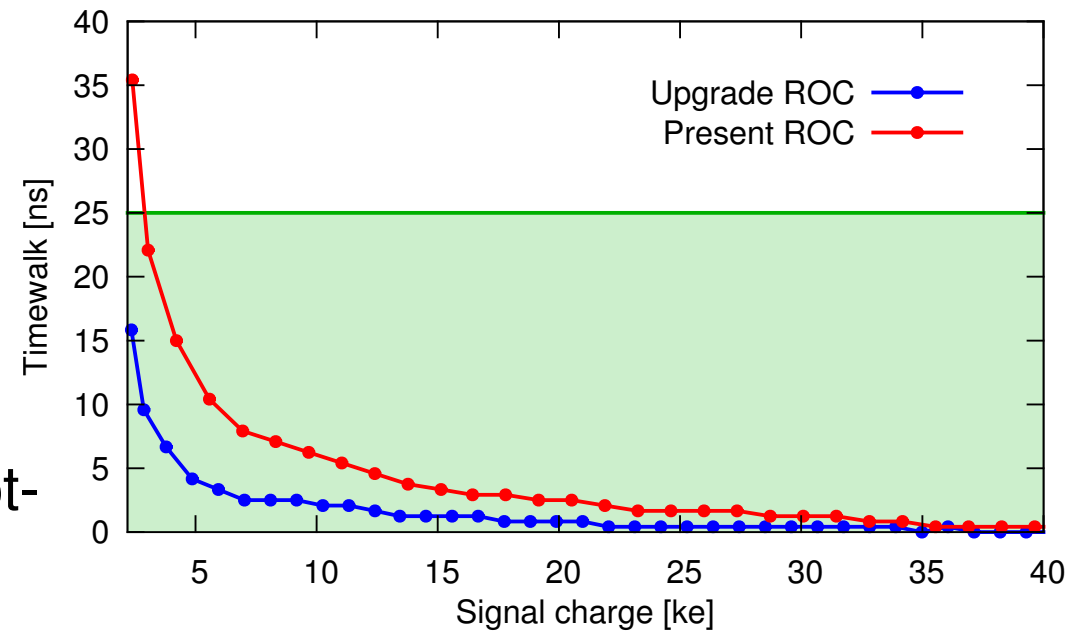
- Successive approximation 8 bit ADC with S&H
- Clock frequency 80 MHz
- Conversion time 8 clock cycles
- Current consumption ?? mA
- Non-linearity smaller than 0.5 LSB
- Explained by DAC ref. current mismatch



Comparator redesign: Timewalk improvement

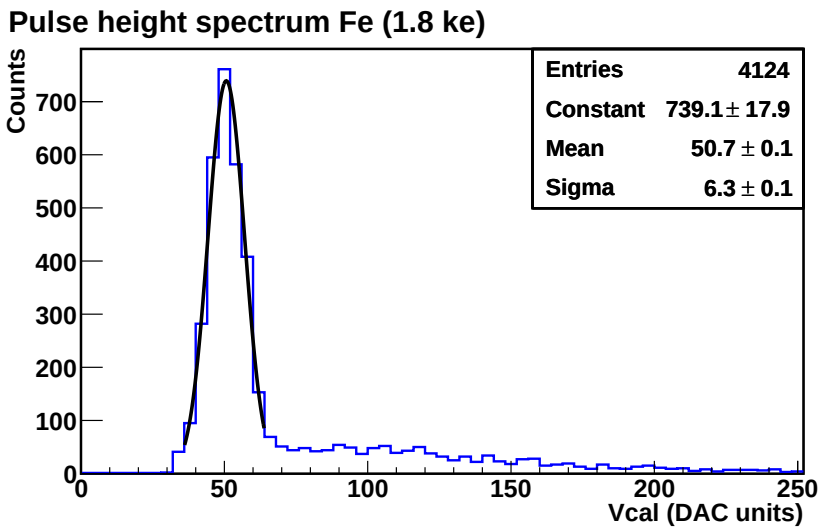
- Smallest signal in acceptance time defines the in-time threshold
- New comparator reduces timewalk to < 25 ns (acceptance time)
- Effectively lowers the threshold by ≈ 700 e$^-$ w.r.t. current design
- CMS (in-time) threshold ≈ 3200 e$^-$
- Threshold of upgrade ROC ≈ 1800 e$^-$
- Increases maximum acceptable sensor irradiation

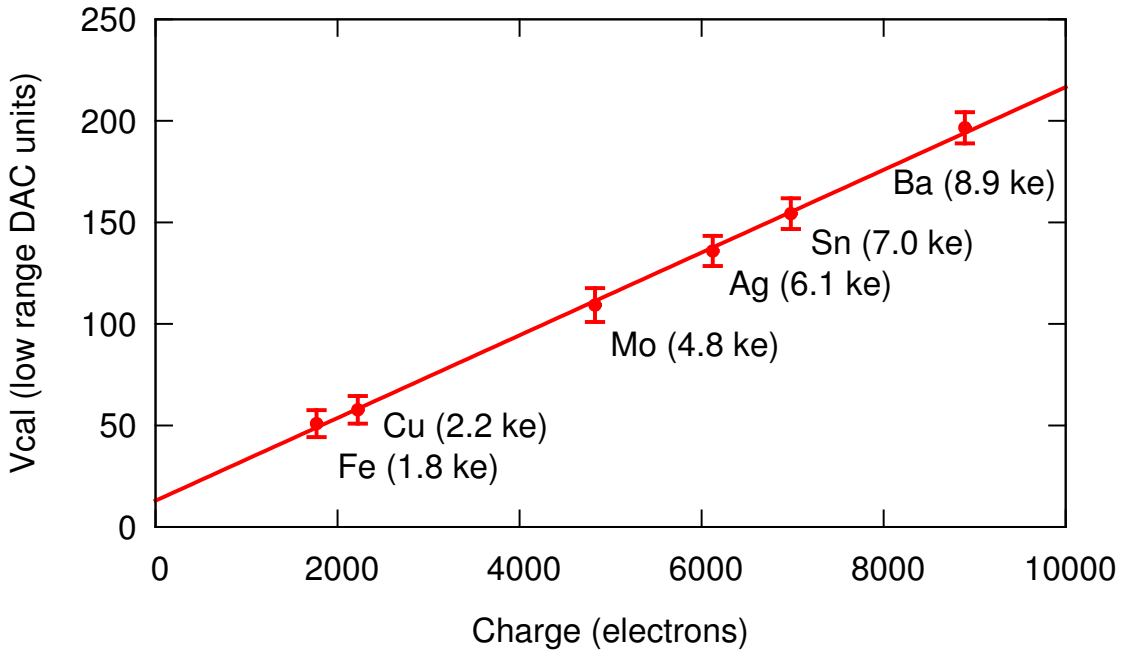




Calibration and confirmation of low threshold

- Use well defined x-ray fluorescence lines for calibration
- Measured spectrum peak compared to internal test pulse
- Iron (Fe) spectrum confirms threshold $< 1800\ e^-$
- Calibration: parameters of linear relation
- Slope: $51.3 \pm 2.8\ e^-/\text{Vcal}$, offset: $-940 \pm 50\ e^-$





Full qualification results

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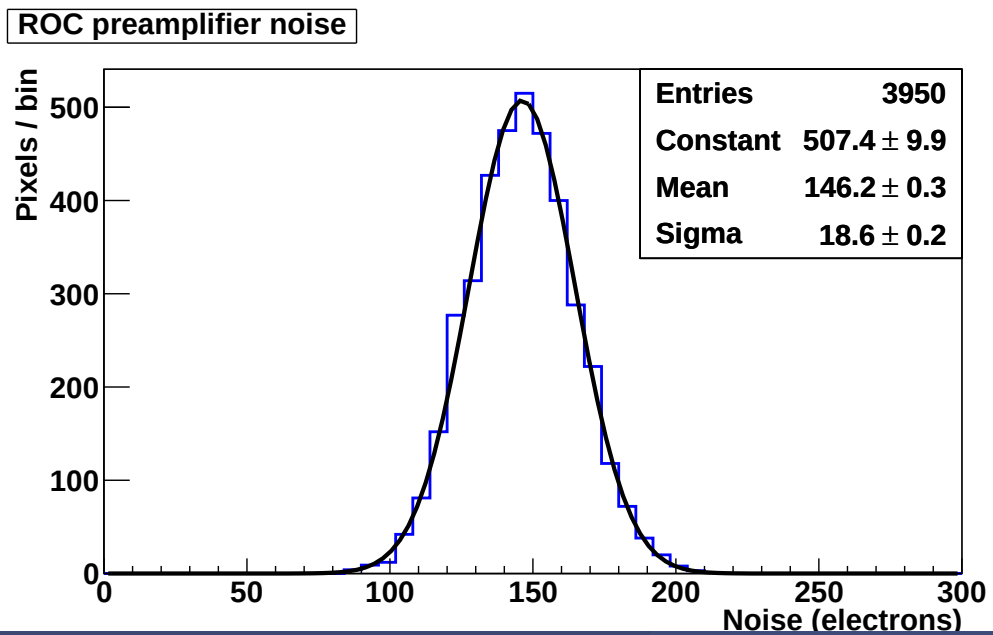
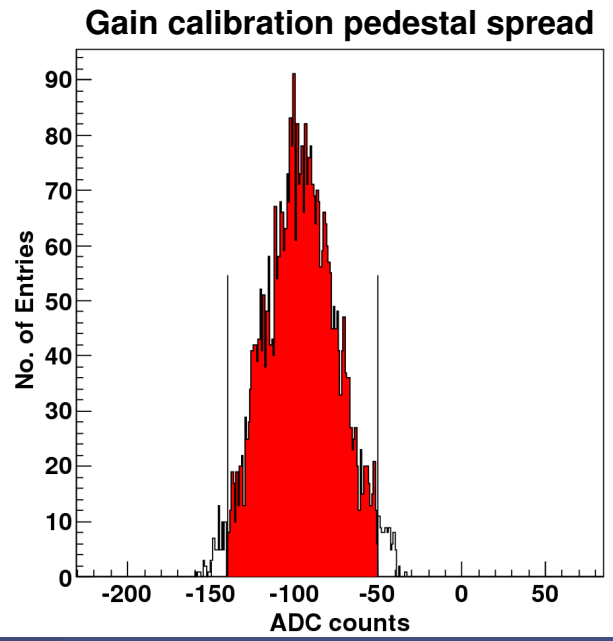
from an analysis of 14 ROCs

	Qualification for present ROC
▸ Pixel defects: ≈ 0.3 %	< 1.0 %
▸ Preamplifier noise: $\approx 150 \pm 20$ e$^-$	< 500 e$^-$
▸ Gain calibration:	
▸ Gain: ≈ 0.06 %	< 0.10 %
▸ Pedestal: ≈ 1300 e$^-$	< 2500 e$^-$





Summary

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- The CMS pixel detector readout chip will changed for the Phase 1 Upgrade
- Motivation for the change include
  - Increasing the number of pixel hits from 3 to 4
  - Increase readout bandwidth to allow for more channels using the same fibres
  - Maintain efficiency at new rate conditions
  - Increase the layer lifetime by lowering the threshold
- Evolutionary changes to achieve these goals have been made
- ROC prototype works very well and with expected performance
- Plans for the future:
  - Pilot system installed with present detector in long shutdown 1
  - ROC mass production in 2014
  - Phase 1 four pixel hit upgrade in extended winter shutdown 2016/17

Thank you for your attention!

Backup

ADC non-linearity