# BPIX Module Testing Status - Week 7

19th February 2007

# Production overview

**Production Status:** 448 modules produced (403 / 45)

- 280/61 graded as A/B → 85% || 35/6 → 91%
- 62 graded as C → 15% || 4 → 9%

**Module Testing Report of Week 7:**

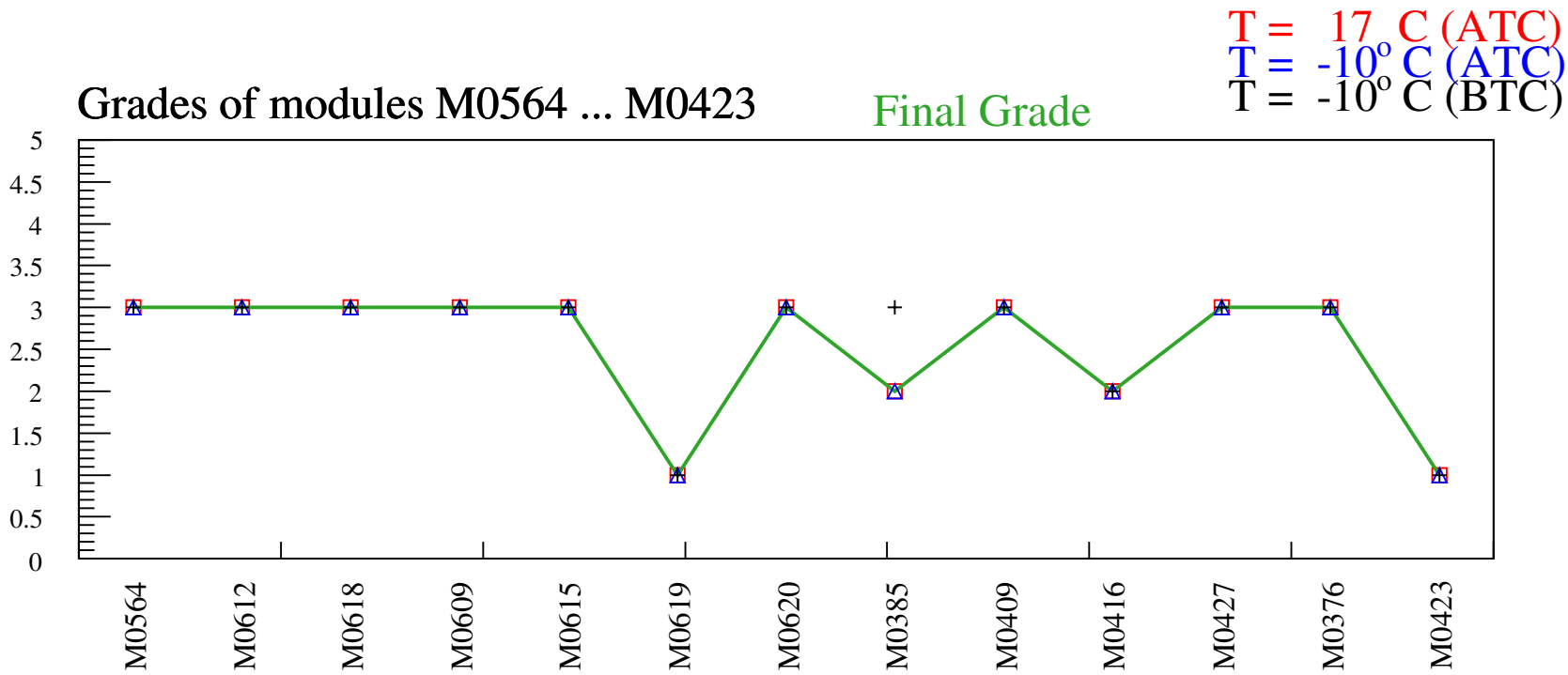
- 7/6 modules fully tested and therm. cycled (0 retested)

| | *Modules* | | | *Half-Modules* | | |
|---|---|---|---|---|---|---|
| **Grade** | **A** | **B** | **C** | **A** | **B** | **C** |
| T = $-10^o$ C, BTC* | 6 | 0 | 1 | 4 | 1 | 1 |
| T = $-10^o$ C, ATC | 6 | 0 | 1 | 3 | 2 | 1 |
| T = $+17^o$ C, ATC | 6 | 0 | 1 | 3 | 2 | 1 |
| **Final Grade** | 6 | 0 | 1 | 3 | 2 | 1 |

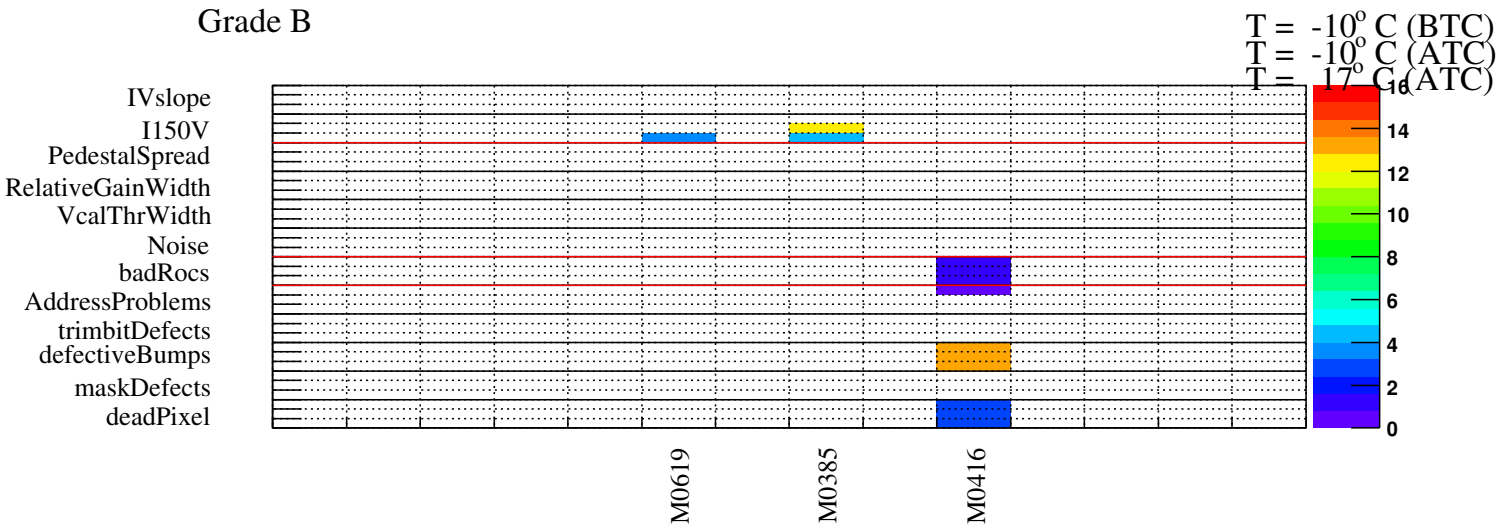
- no retests with new DAC settings

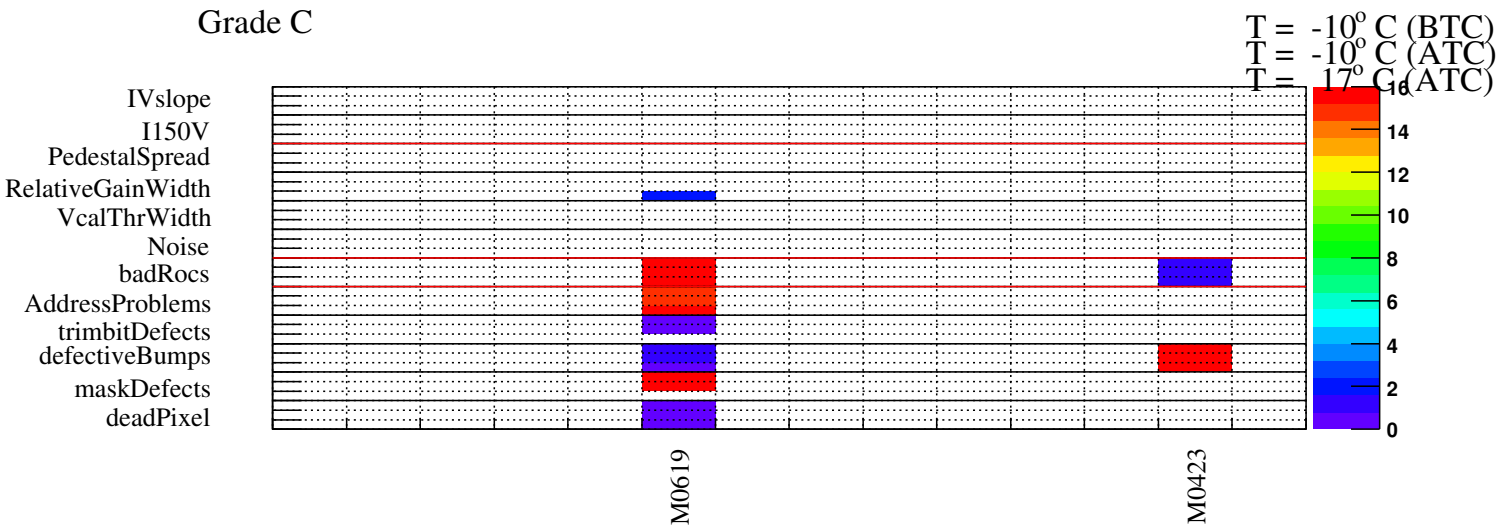
*without IV-criteria

# Production summary



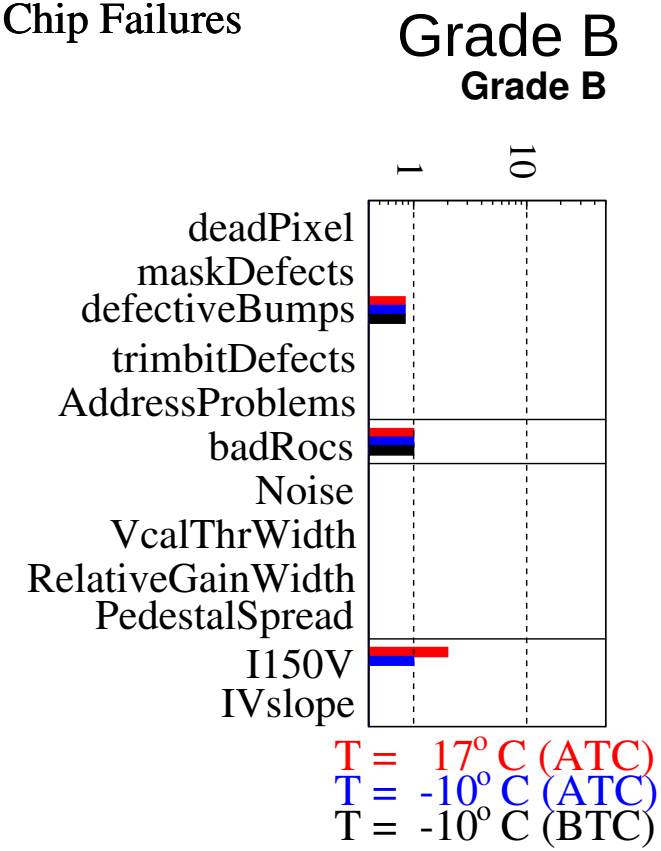
# Module Failures Overview

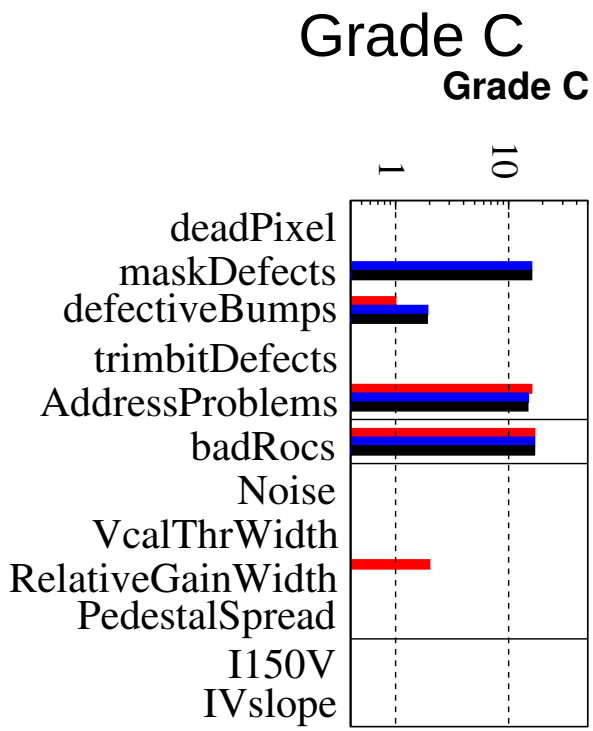


# Production quality

Chip Failures




← Pixel defects

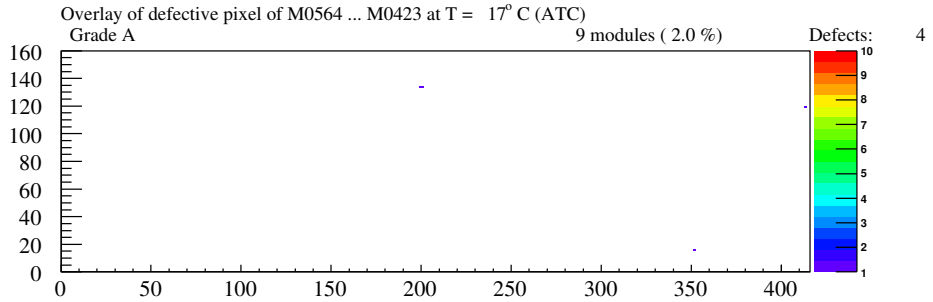
← Chip performance

← Module IV

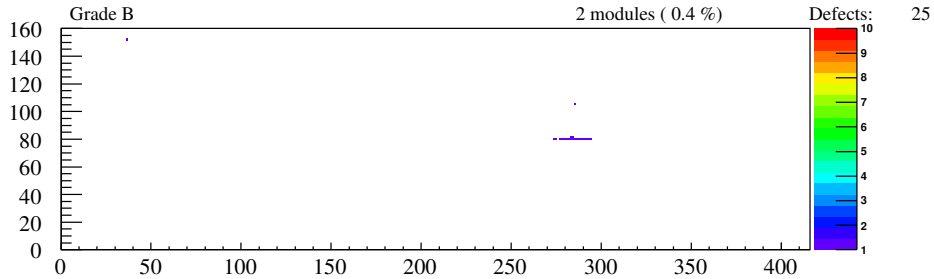
# Defective pixel $T = 17^{o}C$ (ATC)

## Overlay of all fully tested modules at T = $+17^{o}$ C (ATC)

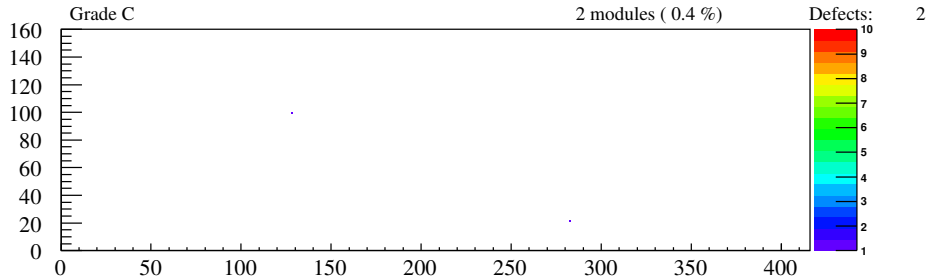
Grade A
(9 modules)




Grade B
(2 modules)



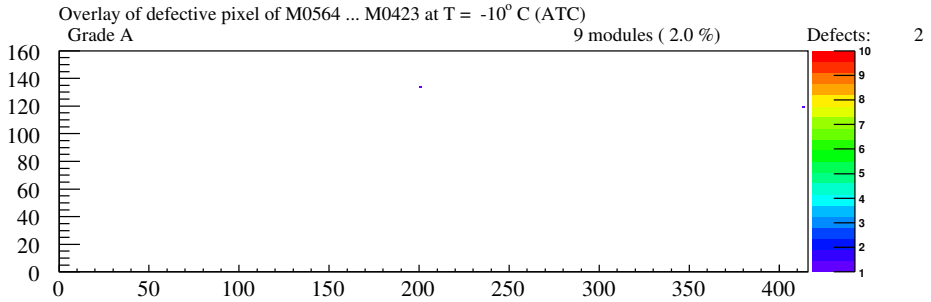

Grade C
(2 modules)



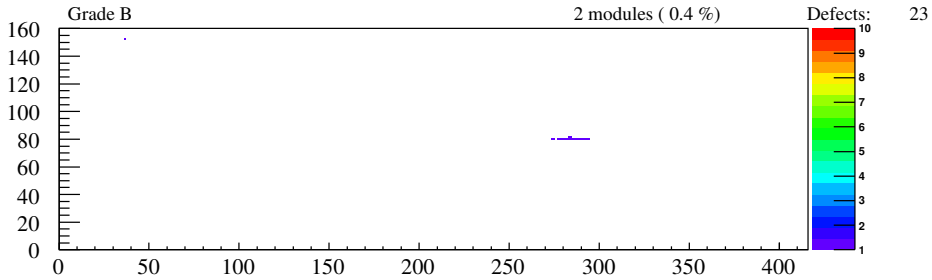
# Defective pixel $T = -10^oC$ (ATC)

## Overlay of all fully tested modules at T = $-10^o$ C (ATC)

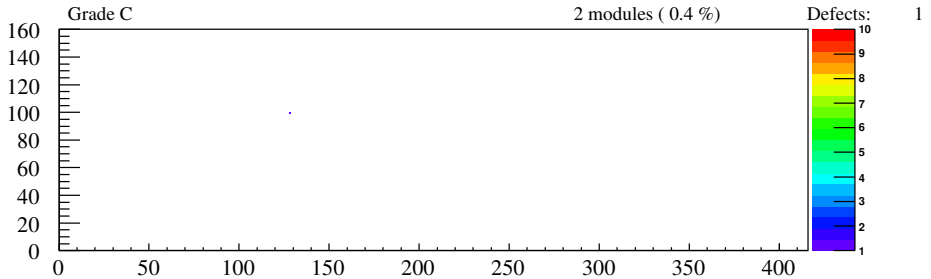
Grade A
(9 modules)




Grade B
(2 modules)



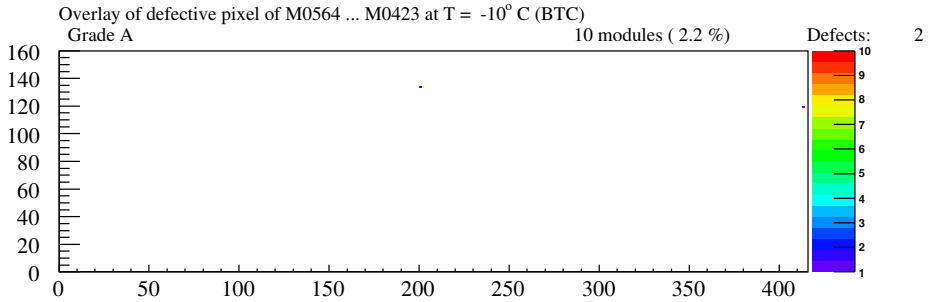

Grade C
(2 modules)



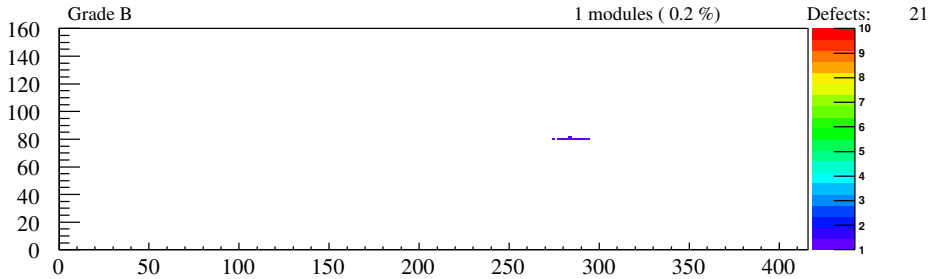
# Defective pixel $T = -10^{o}C$ (BTC)

## Overlay of all fully tested modules at T = $-10^{o}$ C (BTC)

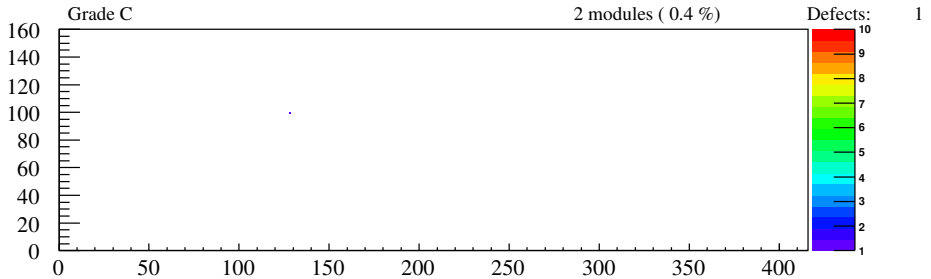
Grade A
(10 modules)




Grade B
(1 modules)



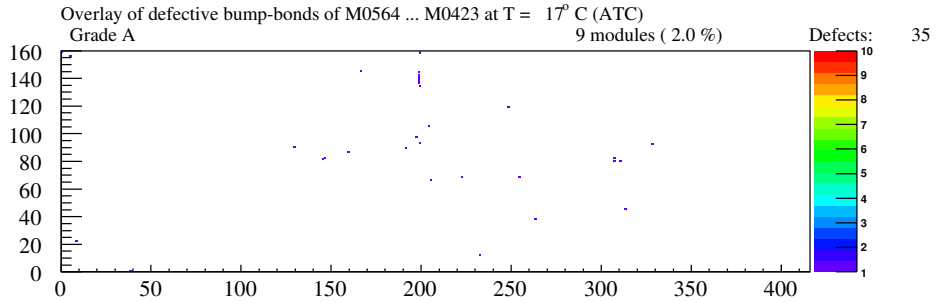

Grade C
(2 modules)



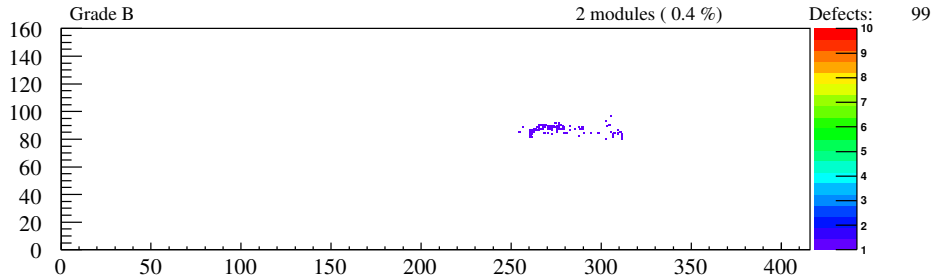
# Defective bump-bonds $T = 17^oC$ (ATC)

Overlay of all fully tested modules at T = $+17^o$ C (ATC)

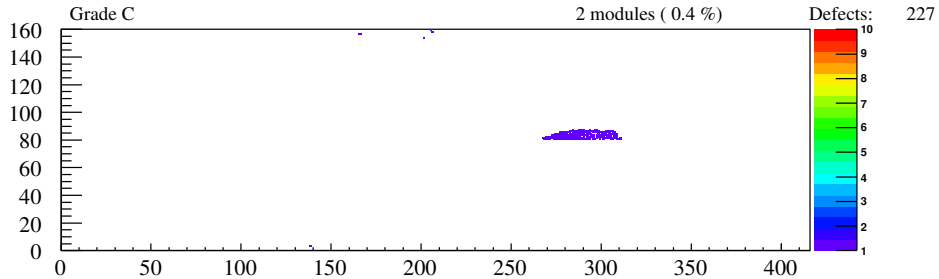
Grade A
(9 modules)




Grade B
(2 modules)



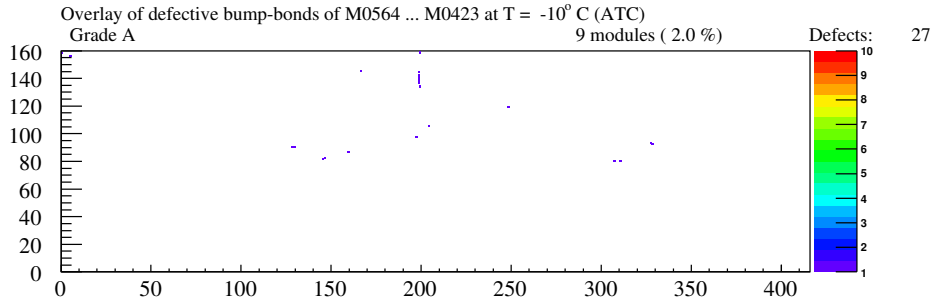

Grade C
(2 modules)



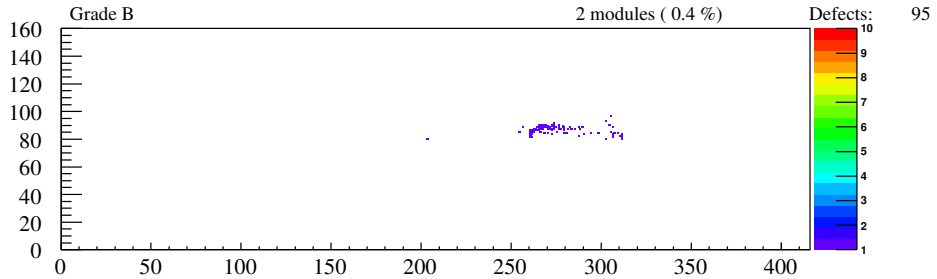
# Defective bump-bonds $T = -10^{o}C$ (ATC)

Overlay of all fully tested modules at T = $-10^{o}$ C (ATC)

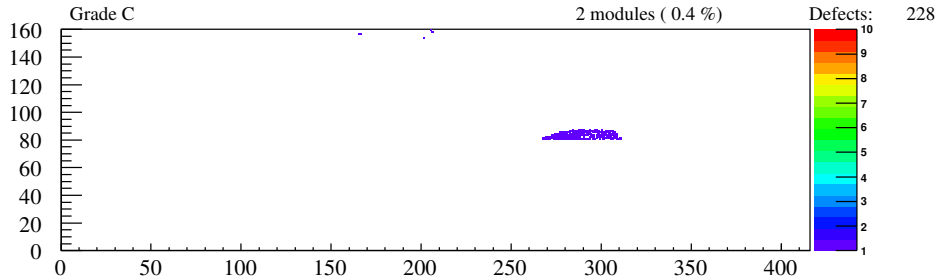
Grade A
(9 modules)




Grade B
(2 modules)



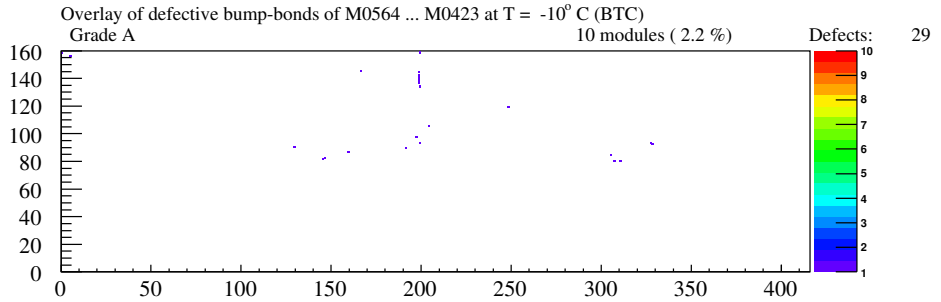

Grade C
(2 modules)



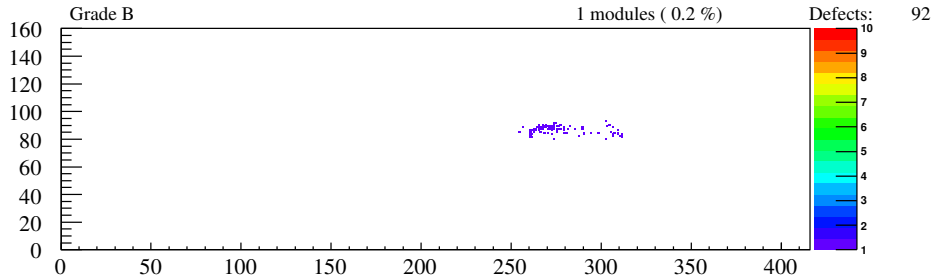
# Defective bump-bonds $T = -10^{o}C$ (BTC)

## Overlay of all fully tested modules at T = $-10^{o}$ C (BTC)

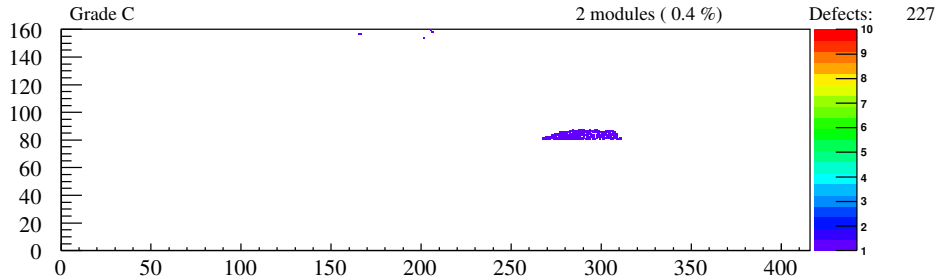
Grade A
(10 modules)




Grade B
(1 modules)

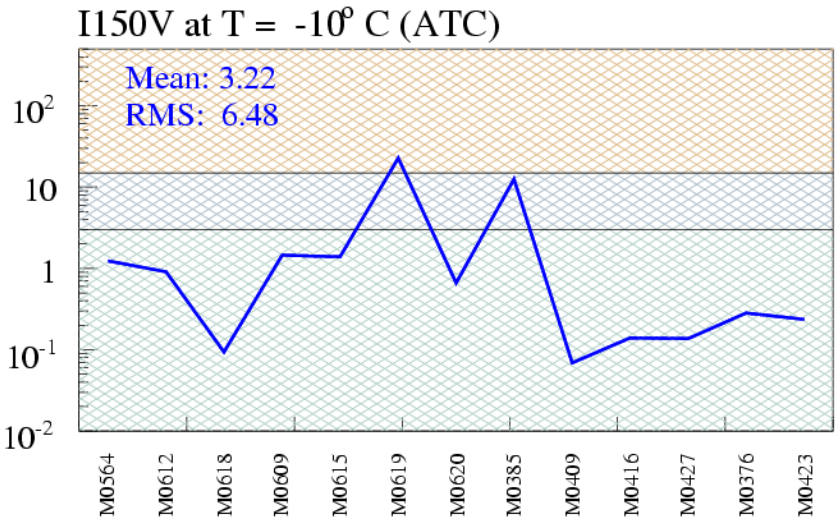



Grade C
(2 modules)

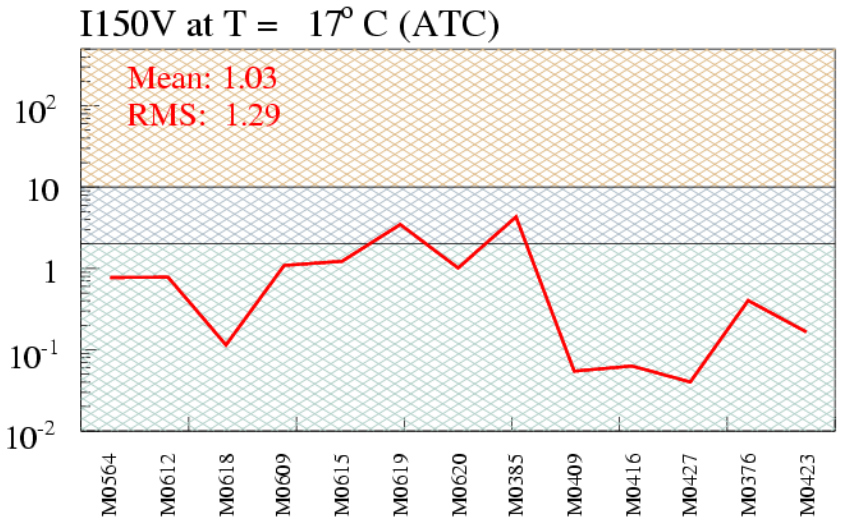


# Current at 150 V

Current at 150 V (in $\mu$A) at $T = 17^oC$ and $T = -10^oC$



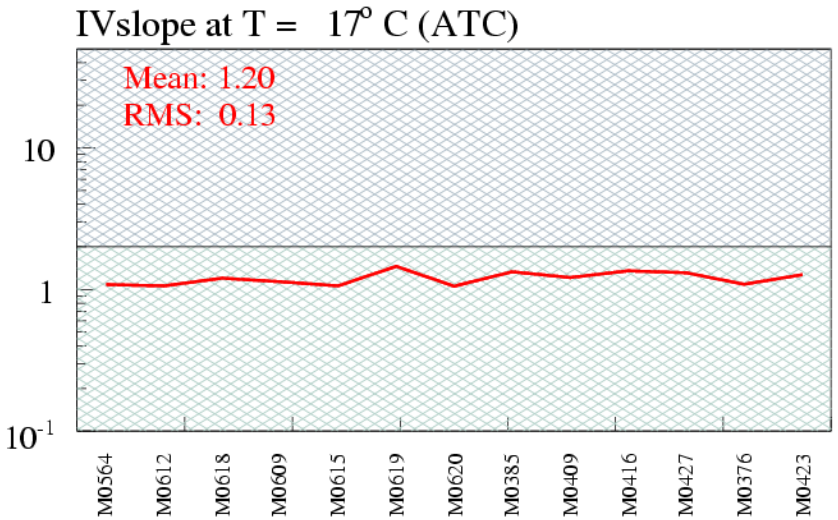

recalculated

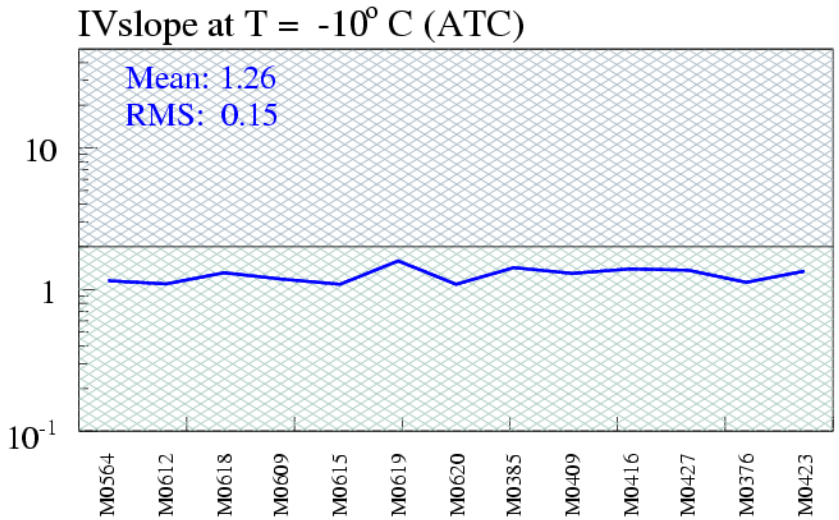



measured

# Slope of IV-Curve

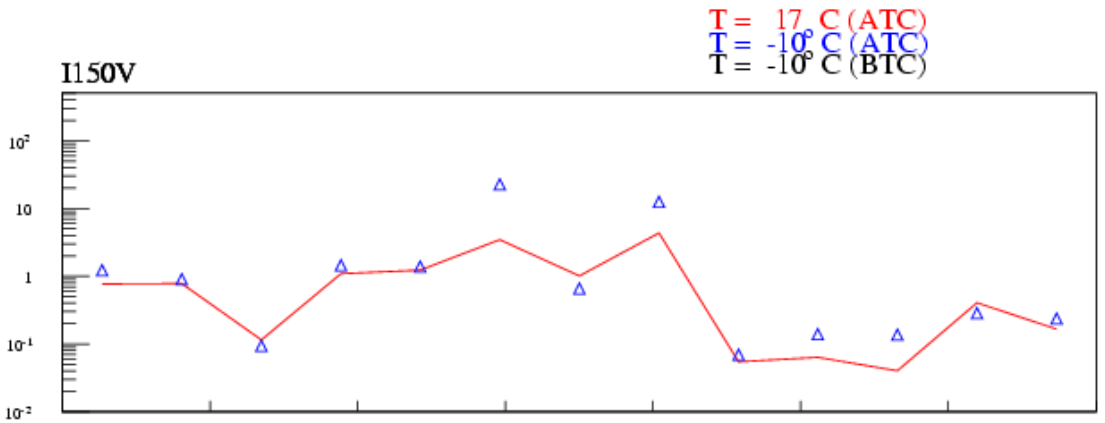
Slope of IV-Curveat $T = 17^oC$ and $T = -10^oC$

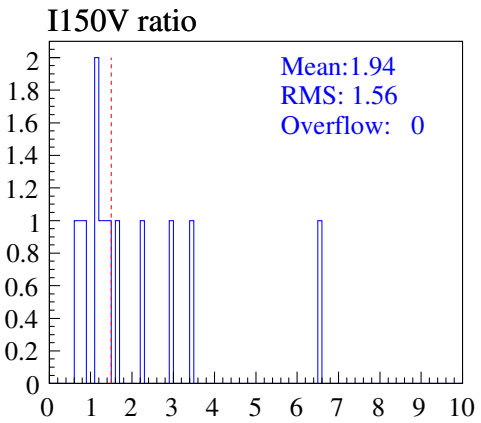


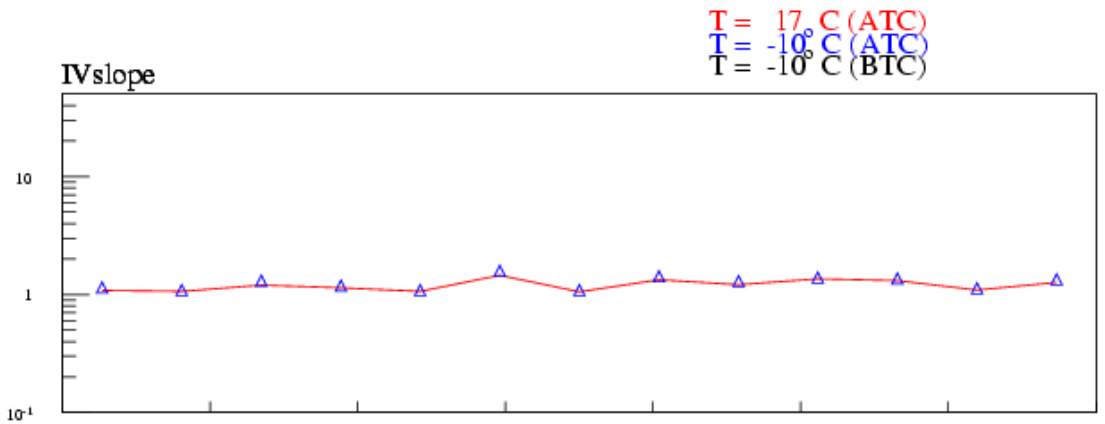



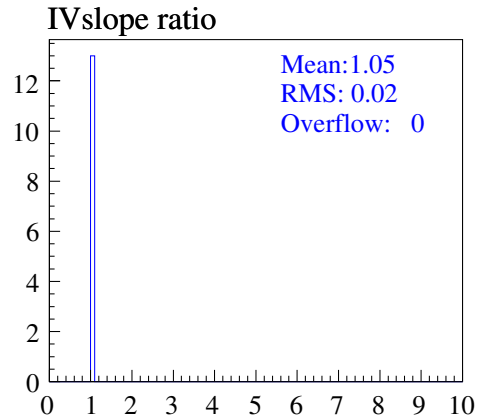
# Current recalculation to $T = 17^oC$

## Cross check of recalculated values with measured values



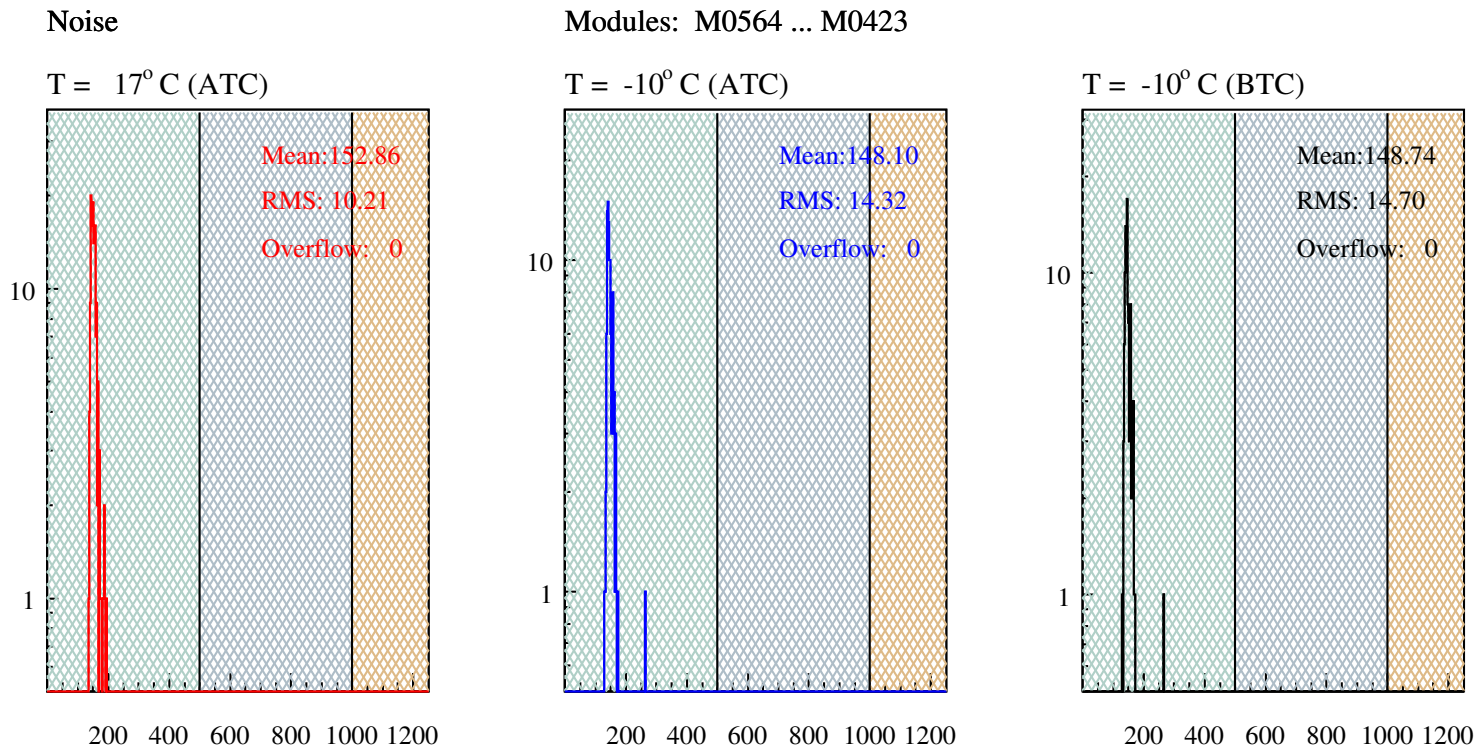



# Noise

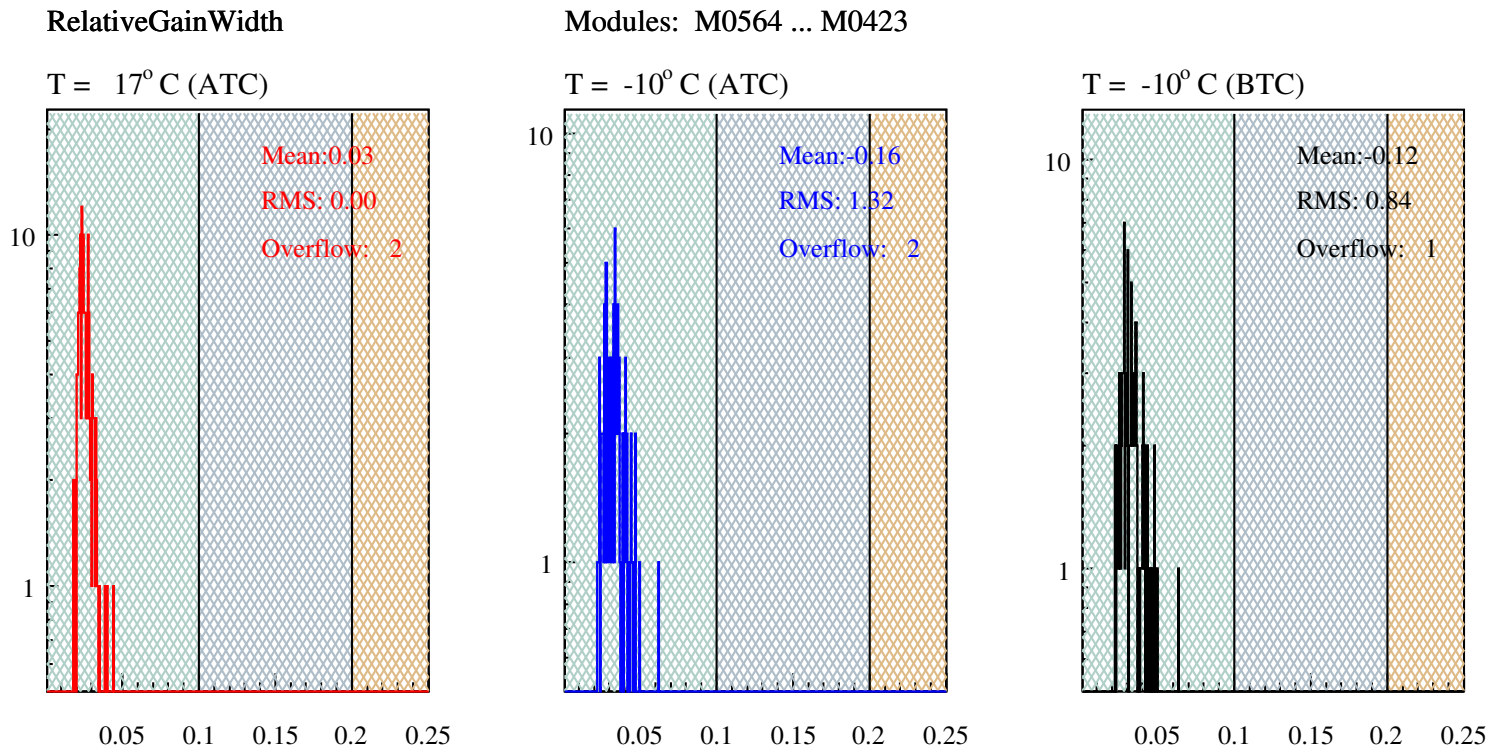
## **MeanNoise** of chips




Noise in $e^-$

# Relative Gain Width

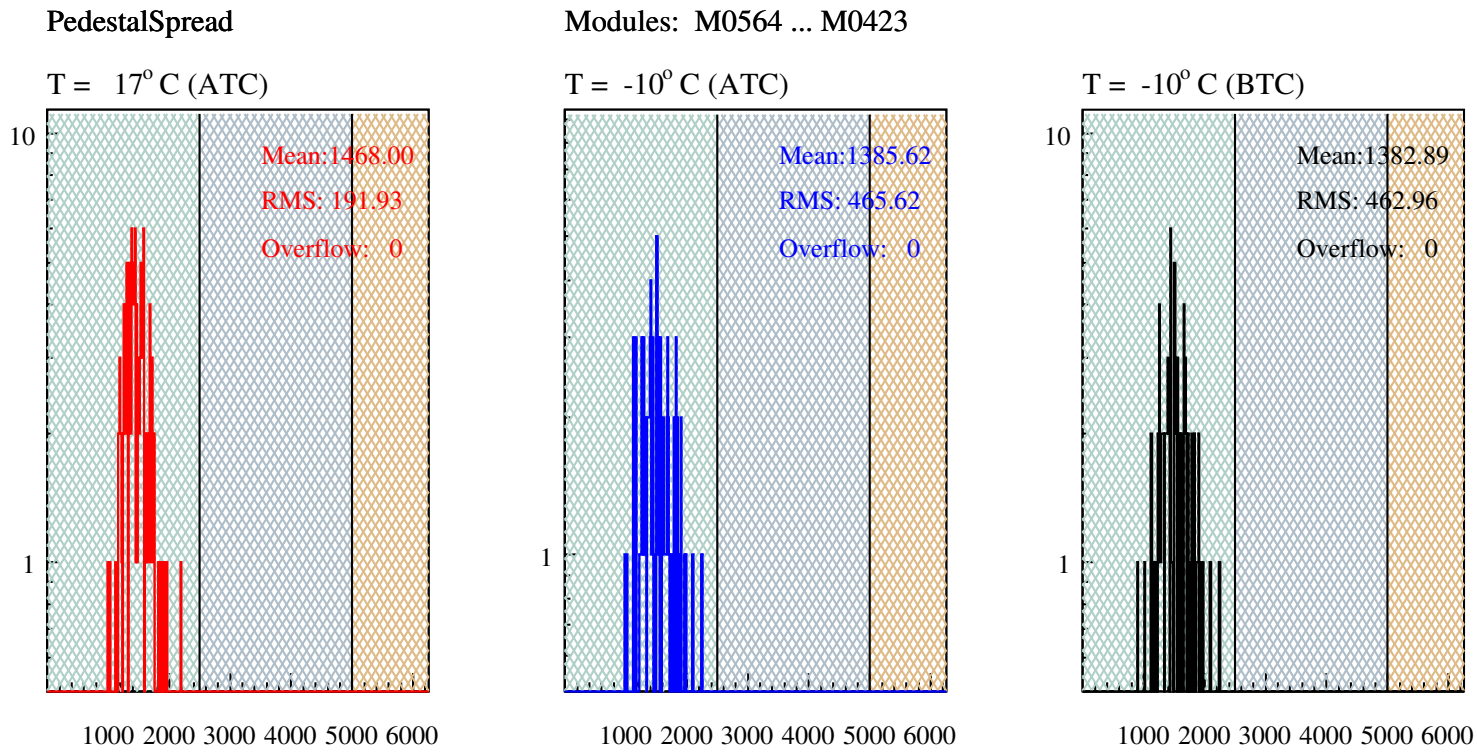
## **RelativeGainWidth** of chips




Rel. Gain Width in %

# Pedestal Spread

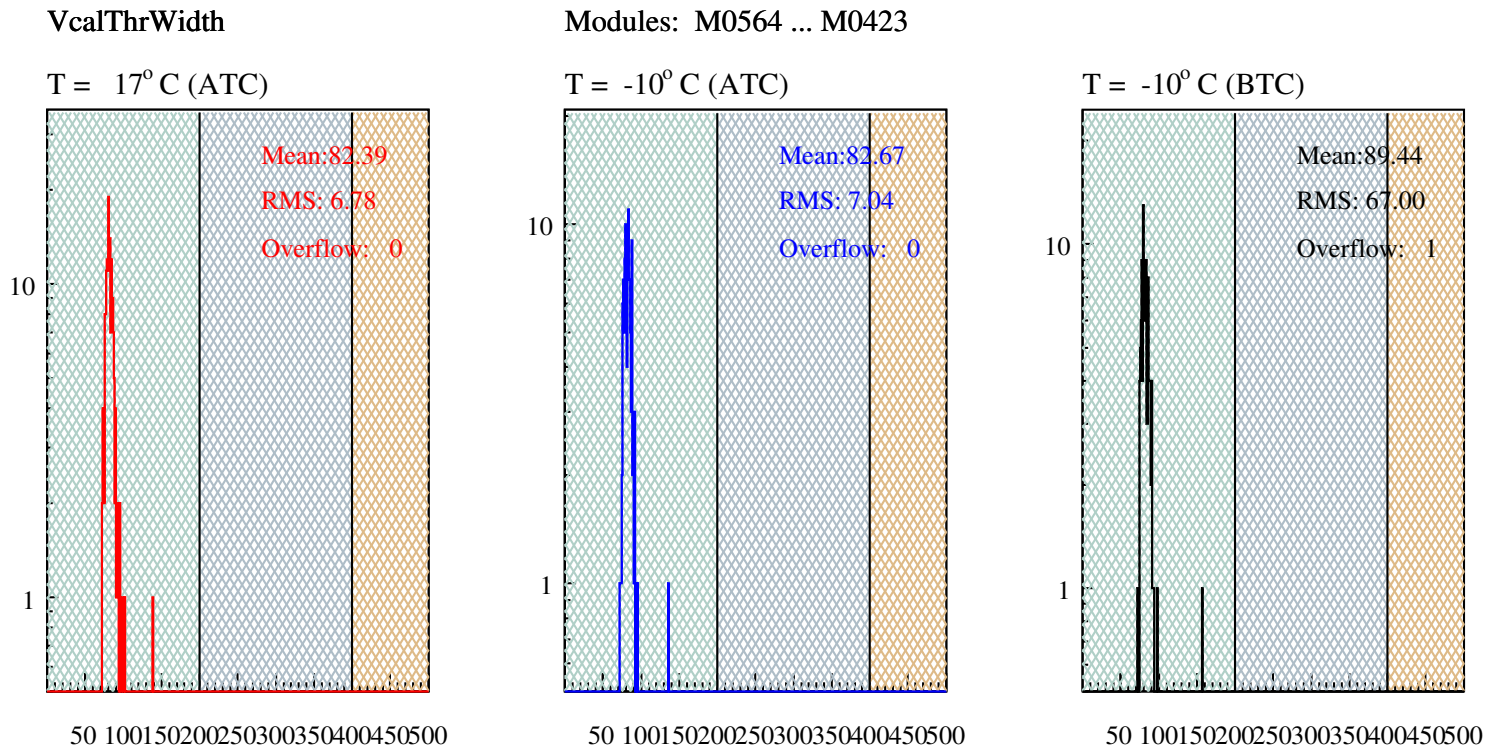
## **PedestalSpread** of chips




Pedestal Spread in $e^-$

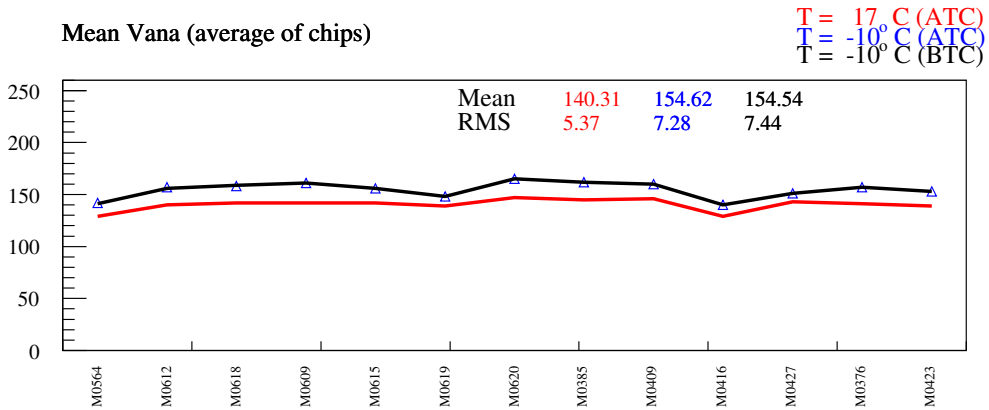
# Vcal Threshold Width

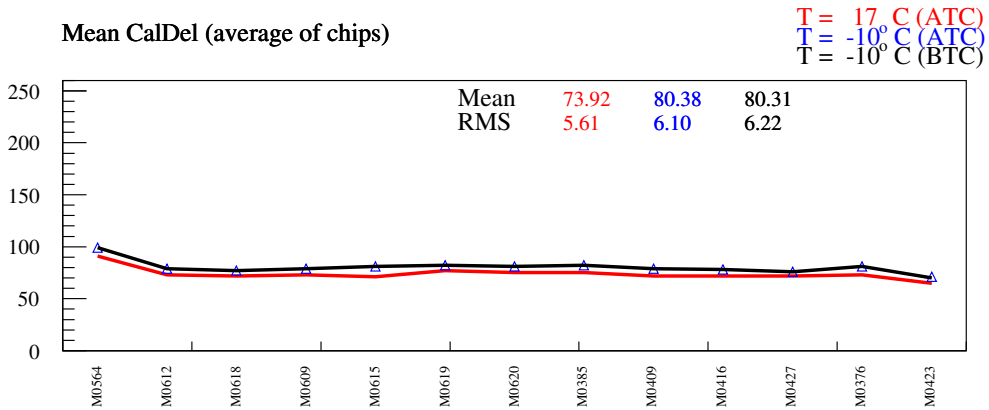
## **VcalThresholdWidth** of chips



# Operational parameters I

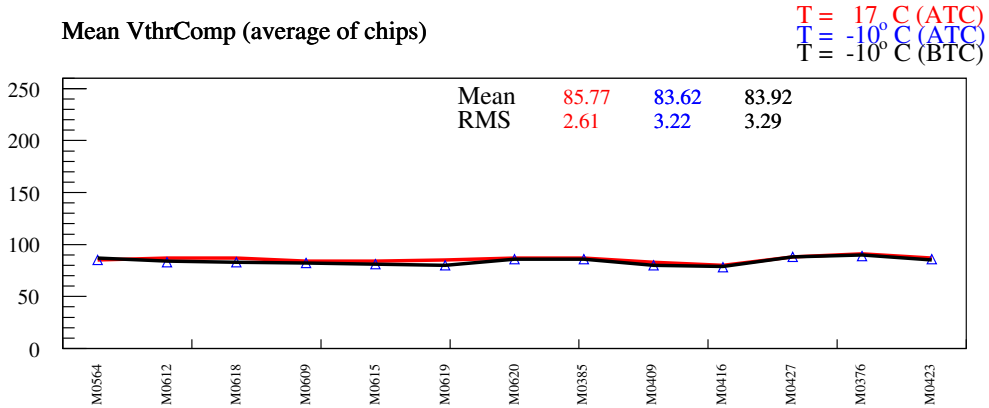
## Mean DACs I

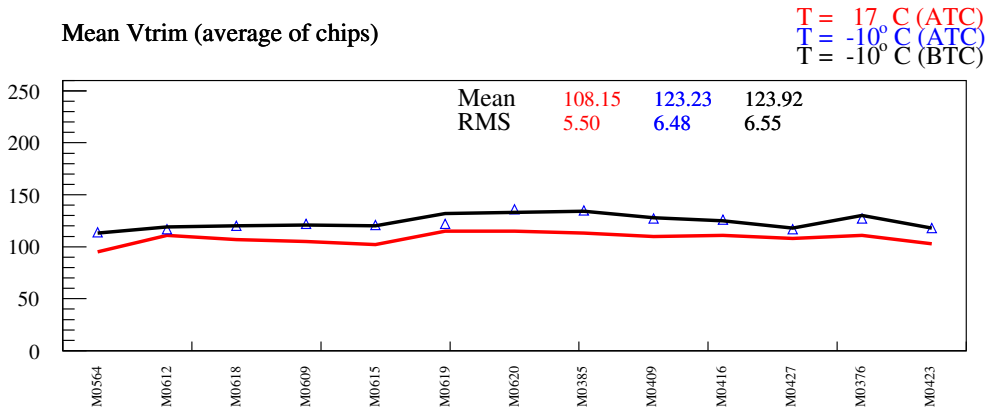


# Operational parameters II

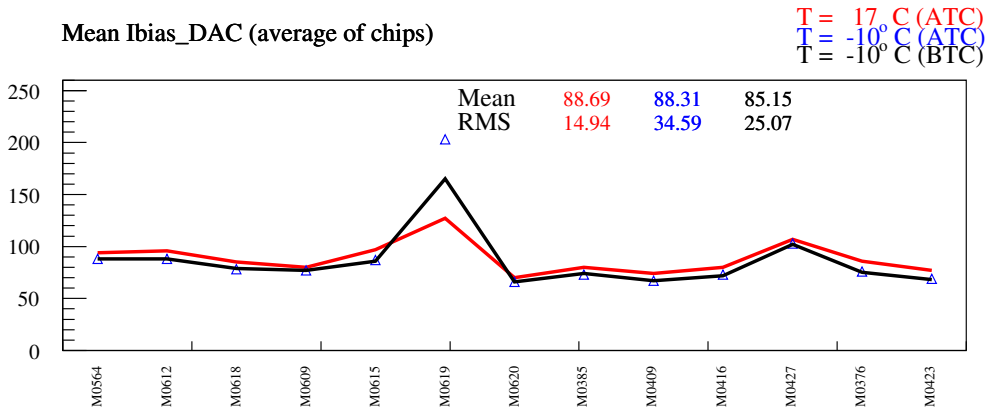
## Mean DACs II

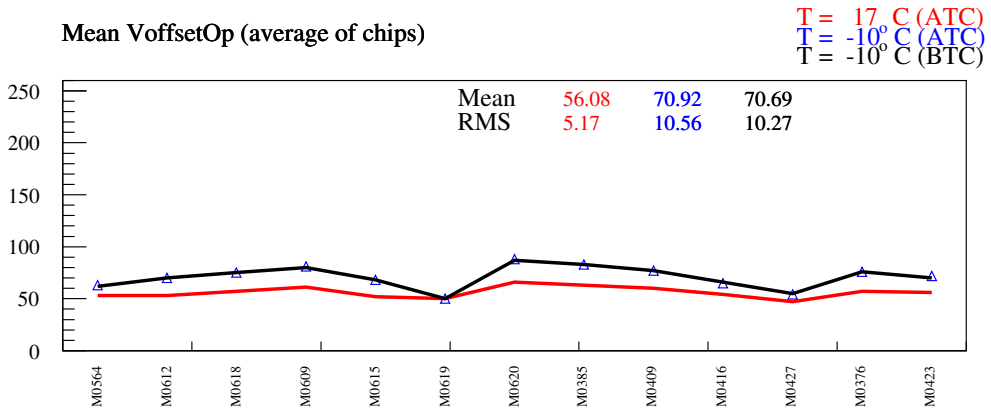


# Operational parameters III

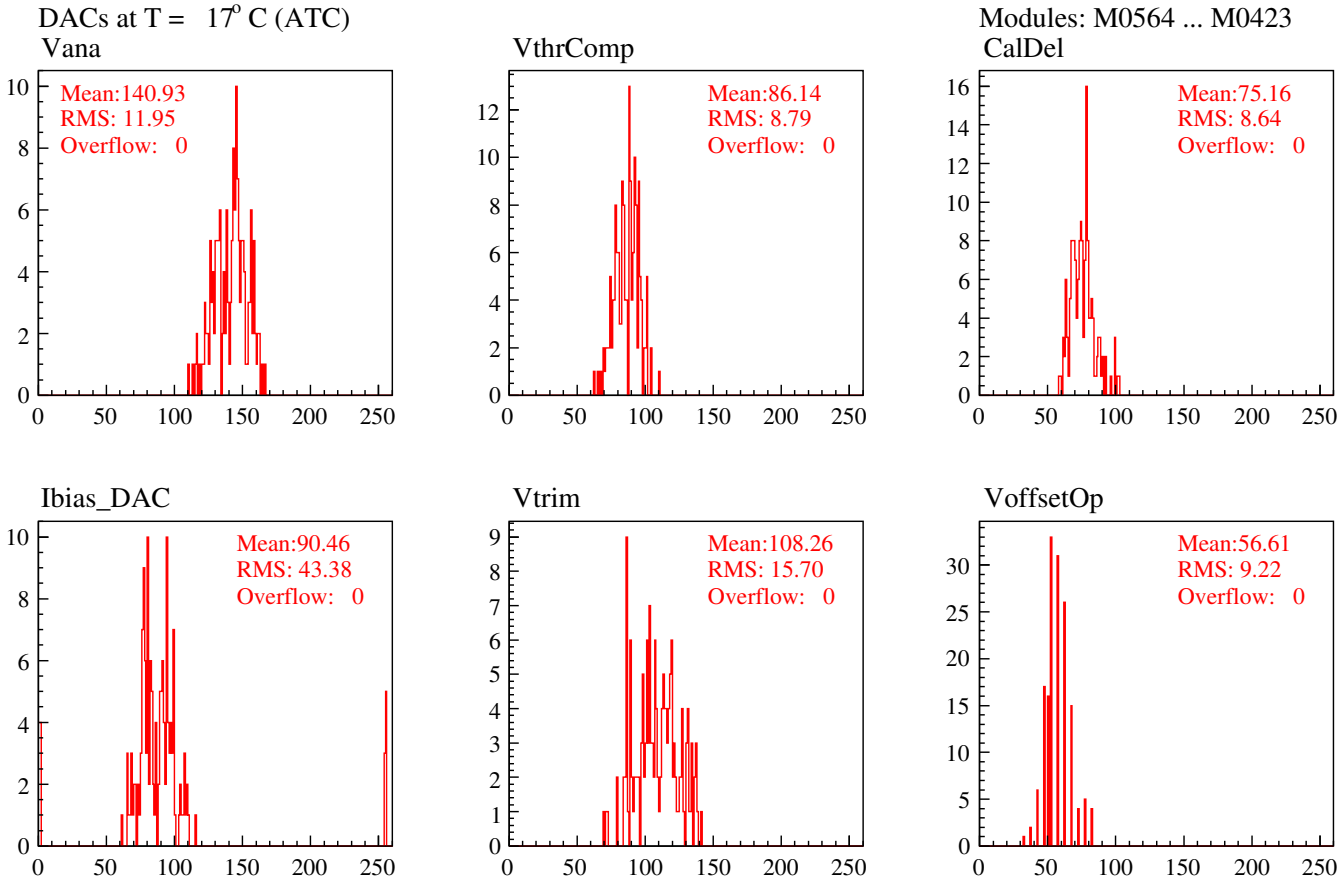
## Mean DACs III



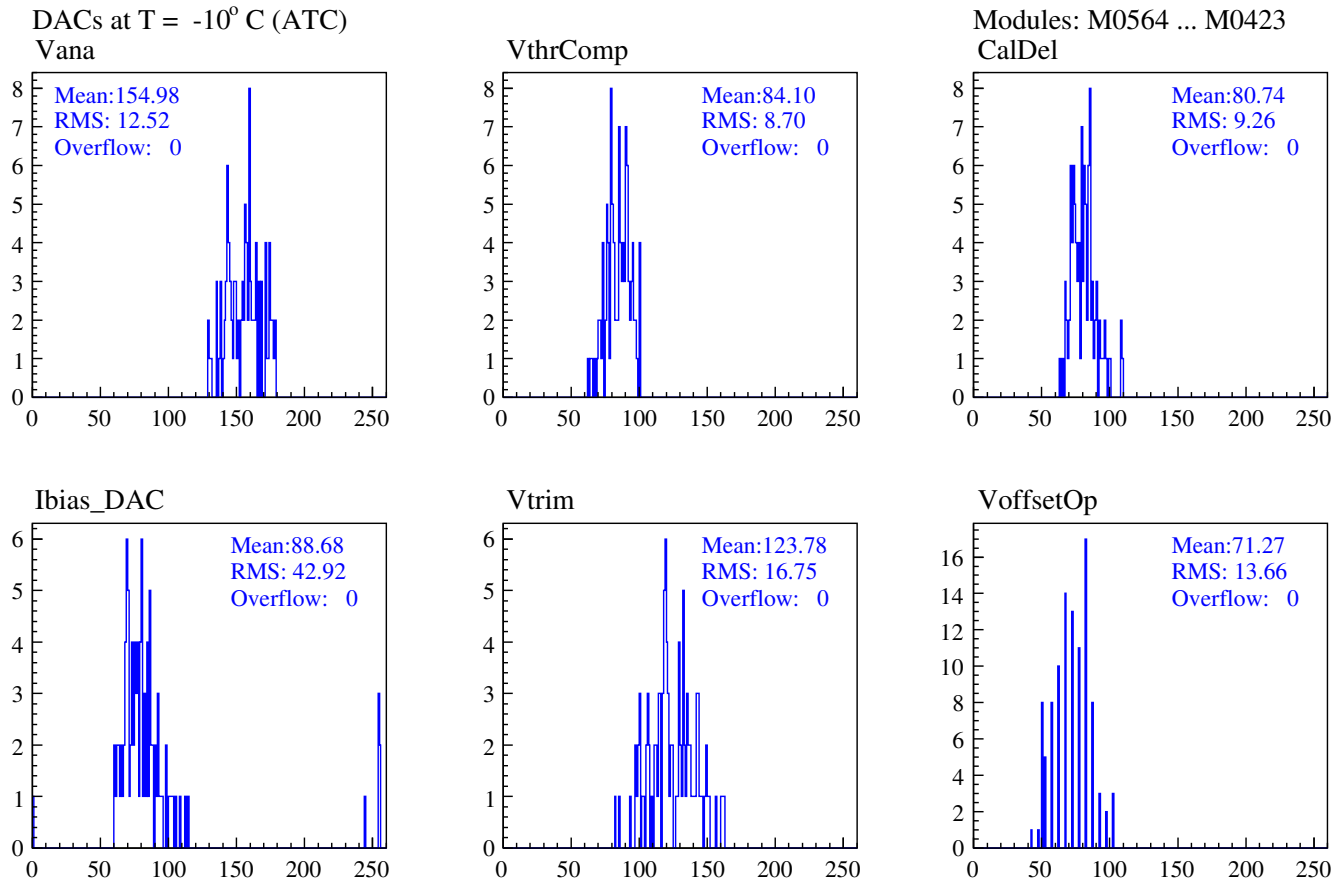
# Operational parameters at $T = +17^{o}C$ (ATC)

## DAC distribution (of chips)



# Operational parameters at $T = -10^{o}C$ (ATC)

## DAC distribution (of chips)



# Operational parameters at $T = +17^{o}C$ (BTC)

## DAC distribution (of chips)