

BPIX Module Testing Status - Week 5

5th February 2007

Production overview

Production Status: 432 modules produced (392 / 40)

- 304/64 graded as A/B → 85%
- 64 graded as C → 15%

Module Testing Report of Week 5:

- 14/10 modules fully tested and therm. cycled (0 retested)

	Modules			Half-Modules		
Grade	A	B	C	A	B	C
T = -10° C, BTC*	14	0	0	9	0	1
T = -10° C, ATC	10	3	1	8	1	1
T = $+17^{\circ}$ C, ATC	11	3	0	9	0	1
Final Grade	10	3	1	8	1	1

- no retests with new DAC settings

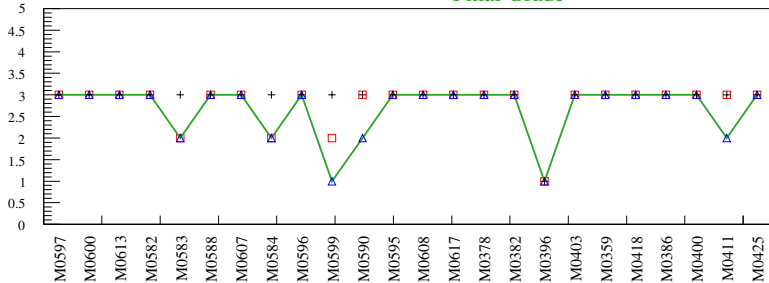
*without IV-criteria

Production summary

Grades of modules M0597 ... M0425

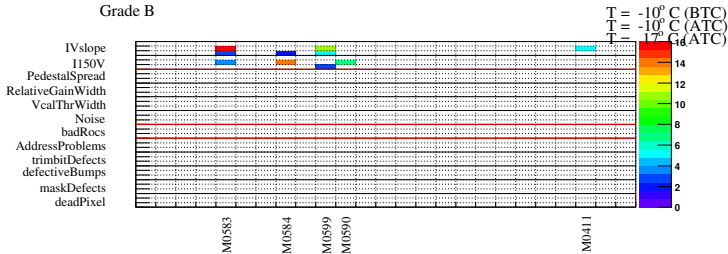
Final Grade

T = 17°C (ATC)
T = -10°C (ATC)
T = -10°C (BTC)

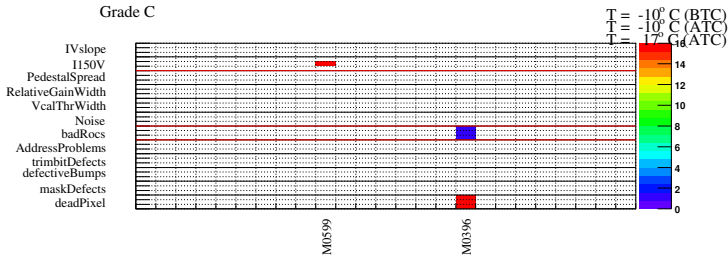


Module Failures Overview

Grade B



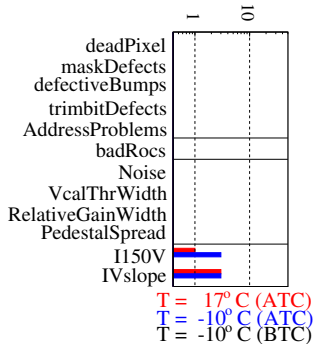
Grade C



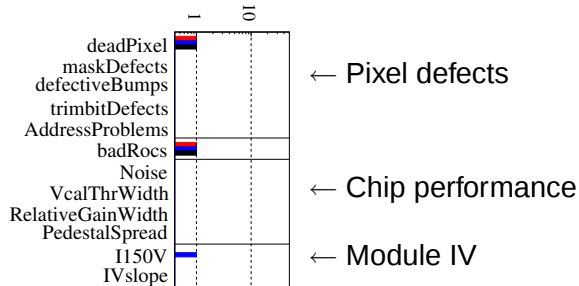
Production quality

Chip Failures

Grade B
Grade B



Grade C
Grade C



← Pixel defects

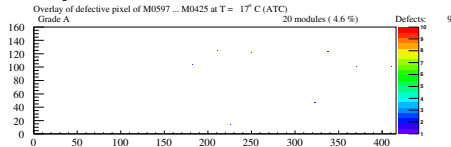
← Chip performance

← Module IV

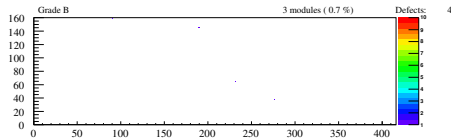
Defective pixel $T = 17^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = +17^{\circ}\text{C}$ (ATC)

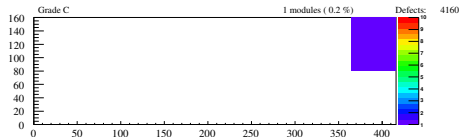
Grade A
(20 modules)



Grade B
(3 modules)



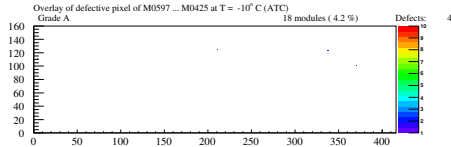
Grade C
(1 modules)



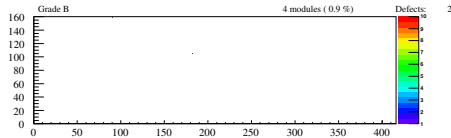
Defective pixel $T = -10^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (ATC)

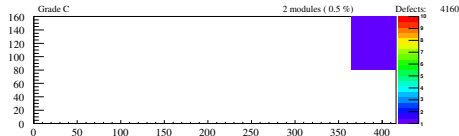
Grade A
(18 modules)



Grade B
(4 modules)



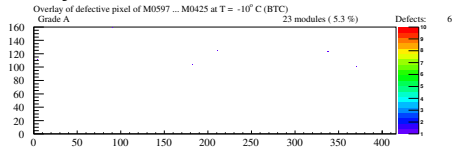
Grade C
(2 modules)



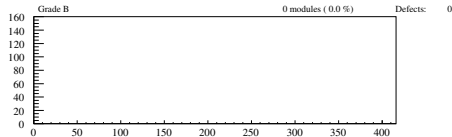
Defective pixel $T = -10^{\circ}\text{C}$ (BTC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (BTC)

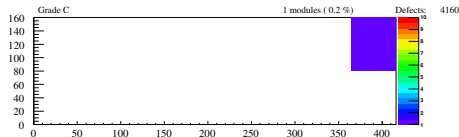
Grade A
(23 modules)



Grade B
(0 modules)



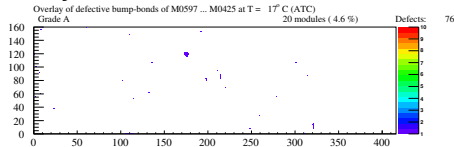
Grade C
(1 modules)



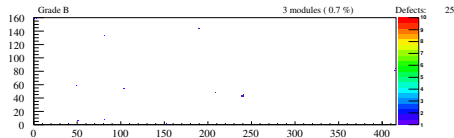
Defective bump-bonds $T = 17^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = +17^{\circ}\text{C}$ (ATC)

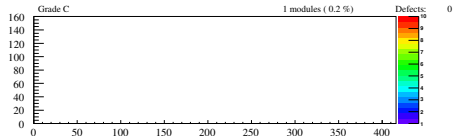
Grade A
(20 modules)



Grade B
(3 modules)



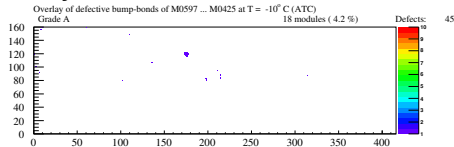
Grade C
(1 modules)



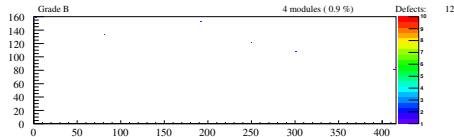
Defective bump-bonds $T = -10^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (ATC)

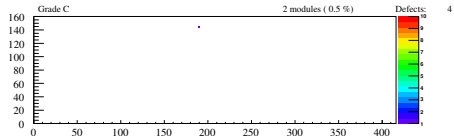
Grade A
(18 modules)



Grade B
(4 modules)



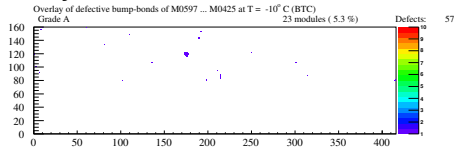
Grade C
(2 modules)



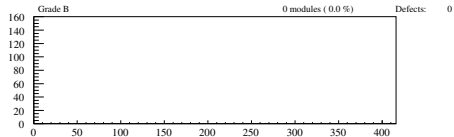
Defective bump-bonds $T = -10^{\circ}\text{C}$ (BTC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (BTC)

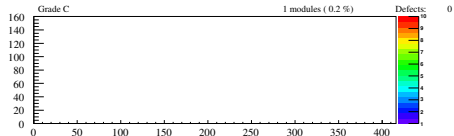
Grade A
(23 modules)



Grade B
(0 modules)



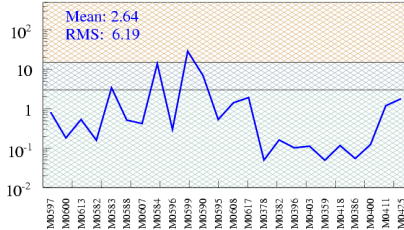
Grade C
(1 modules)



Current at 150 V

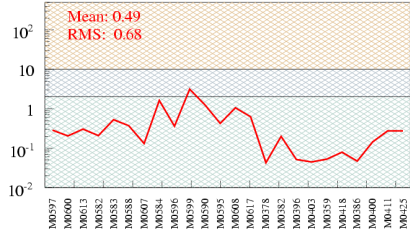
Current at 150 V (in μA) at $T = 17^\circ\text{C}$ and $T = -10^\circ\text{C}$

I150V at T = -10°C (ATC)



recalculated

I150V at T = 17°C (ATC)

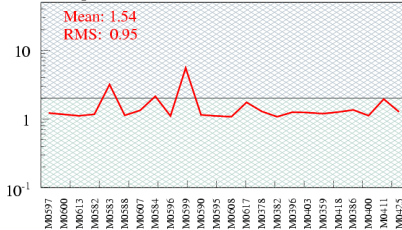


measured

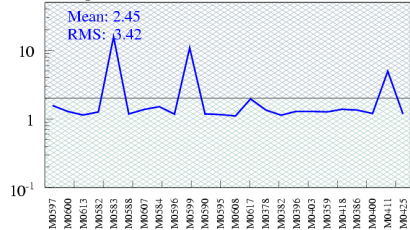
Slope of IV-Curve

Slope of IV-Curve at $T = 17^{\circ}\text{C}$ and $T = -10^{\circ}\text{C}$

IVslope at $T = 17^{\circ}\text{C}$ (ATC)



IVslope at $T = -10^{\circ}\text{C}$ (ATC)

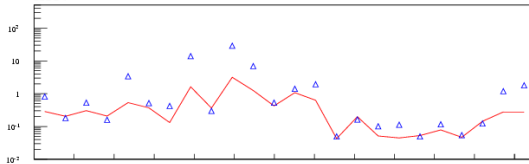


Current recalculation to $T = 17^{\circ}\text{C}$

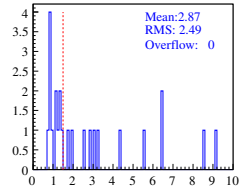
Cross check of recalculated values with measured values

$T = 17^{\circ}\text{C (ATC)}$
 $T = -10^{\circ}\text{C (ATC)}$
 $T = -10^{\circ}\text{C (BTC)}$

I150V

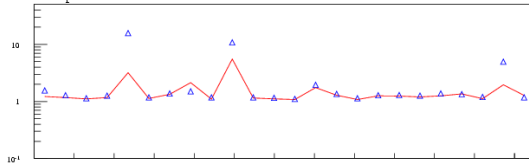


I150V ratio

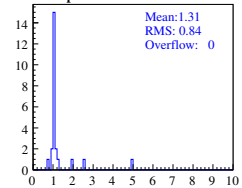


$T = 17^{\circ}\text{C (ATC)}$
 $T = -10^{\circ}\text{C (ATC)}$
 $T = -10^{\circ}\text{C (BTC)}$

IVslope

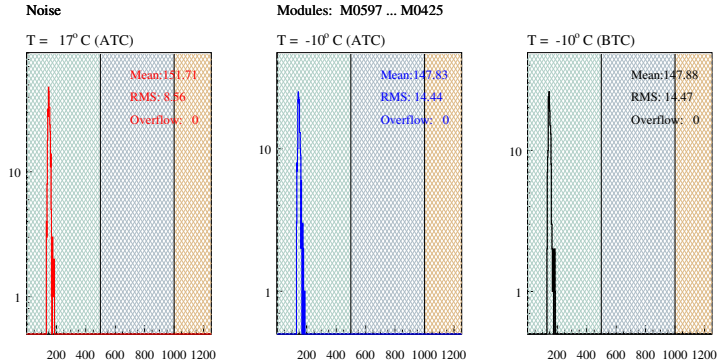


IVslope ratio



Noise

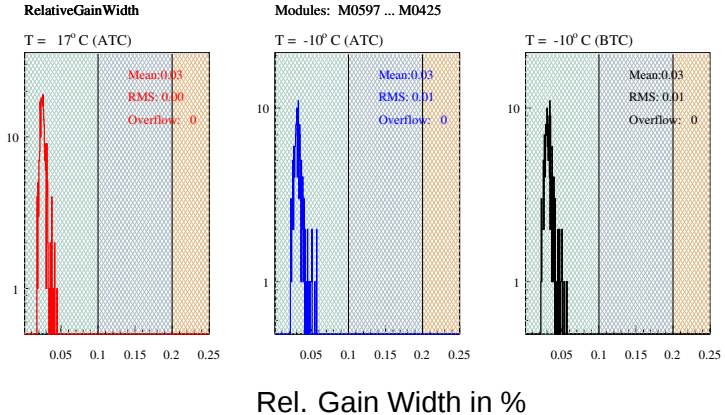
MeanNoise of chips



Noise in e^-

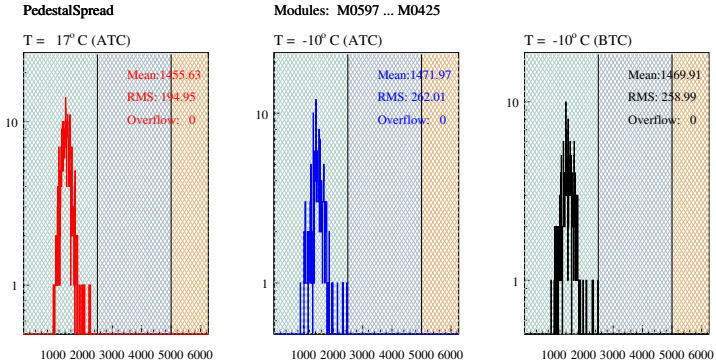
Relative Gain Width

RelativeGainWidth of chips



Pedestal Spread

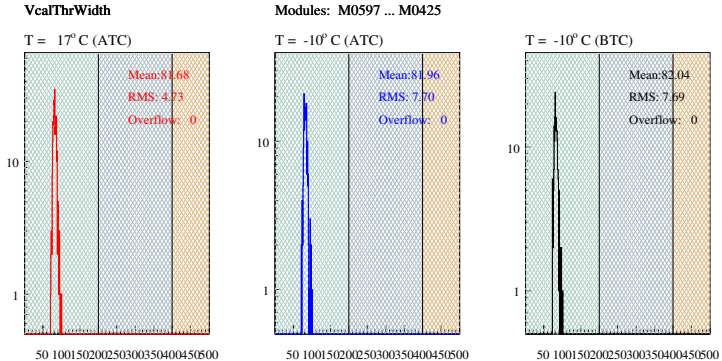
PedestalSpread of chips



Pedestal Spread in e^-

Vcal Threshold Width

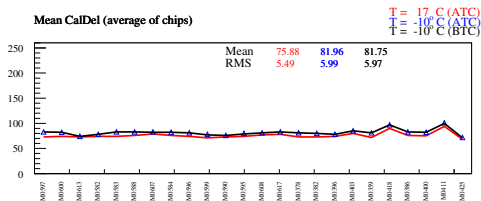
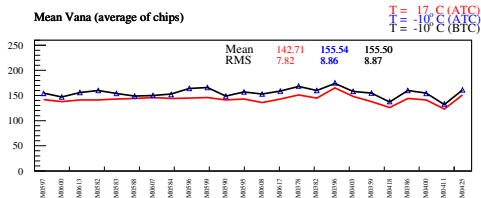
VcalThresholdWidth of chips



Vcal Thr. Width in e^-

Operational parameters I

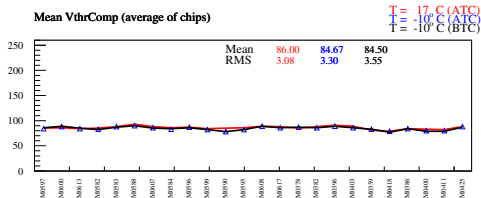
Mean DACs I



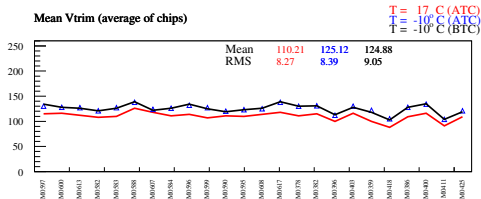
Operational parameters II

Mean DACs II

Mean VthrComp (average of chips)



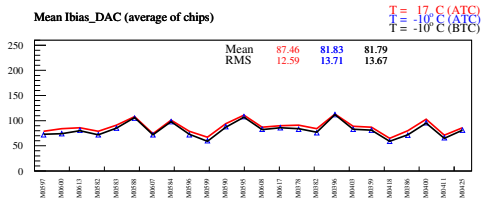
Mean Vtrim (average of chips)



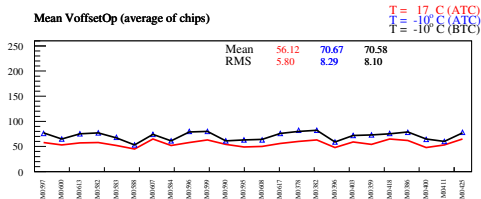
Operational parameters III

Mean DACs III

Mean Ibias_DAC (average of chips)



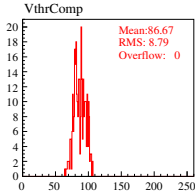
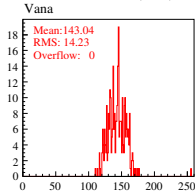
Mean VoffsetOp (average of chips)



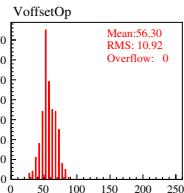
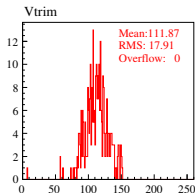
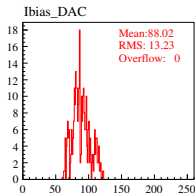
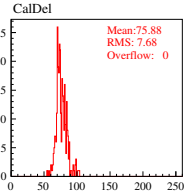
Operational parameters at $T = +17^{\circ}\text{C}$ (ATC)

DAC distribution (of chips)

DACs at $T = 17^{\circ}\text{C}$ (ATC)



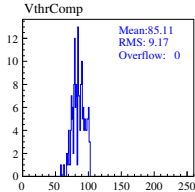
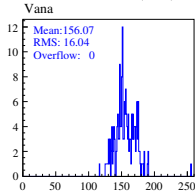
Modules: M0597 ... M0425



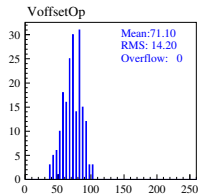
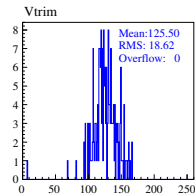
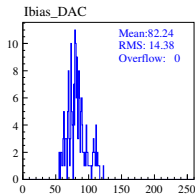
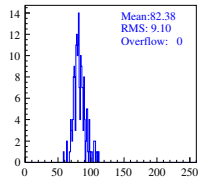
Operational parameters at $T = -10^{\circ}\text{C}$ (ATC)

DAC distribution (of chips)

DACs at $T = -10^{\circ}\text{C}$ (ATC)



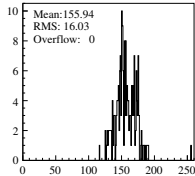
Modules: M0597 ... M0425
CalDel



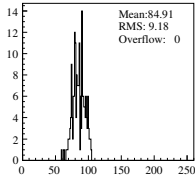
Operational parameters at $T = +17^{\circ}\text{C}$ (BTC)

DAC distribution (of chips)

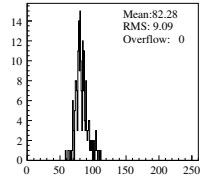
DACs at $T = -10^{\circ}\text{C}$ (BTC)
Vana



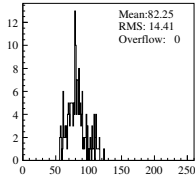
VthrComp



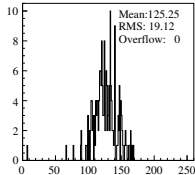
Modules: M0597 ... M0425
CalDel



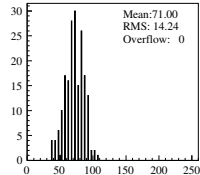
Ibias_DAC



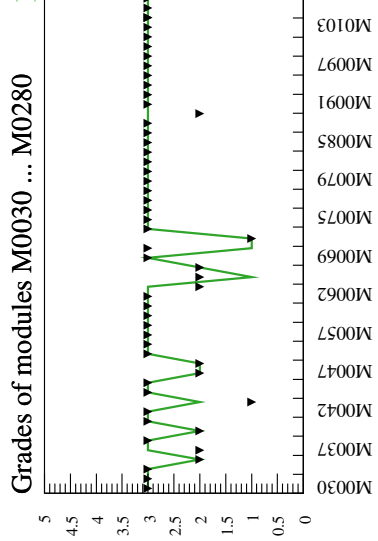
Vtrim



VoffsetOp



Retest Grades

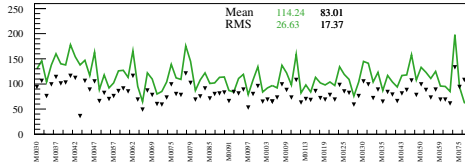


Operational parameters

Mean DACs I

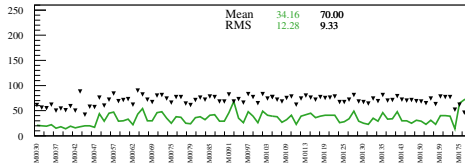
Mean Ibias_DAC (average of chips)

T = -10° C (ATC)
T = -10° C (ATC retest)



Mean VoffsetOp (average of chips)

T = -10° C (ATC)
T = -10° C (ATC retest)

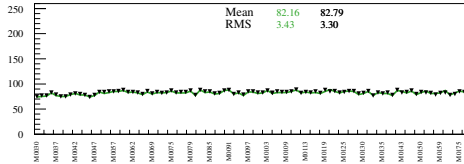


Operational parameters

Mean DACs II

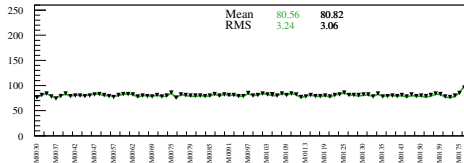
Mean VthrComp (average of chips)

T = -10. C (ATC)
T = -10° C (ATC retest)



Mean CalDel (average of chips)

T = -10. C (ATC)
T = -10° C (ATC retest)

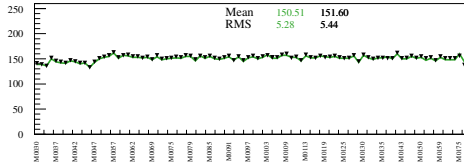


Operational parameters

Mean DACs III

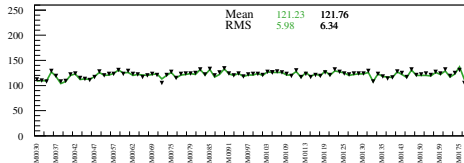
Mean Vana (average of chips)

T = -10° C (ATC)
T = -10° C (ATC retest)



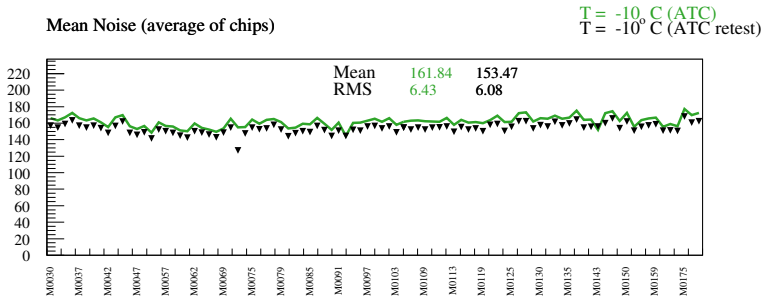
Mean Vtrim (average of chips)

T = -10° C (ATC)
T = -10° C (ATC retest)



Performance parameters

Mean **Noise** [e^-] vs. Module Nr.

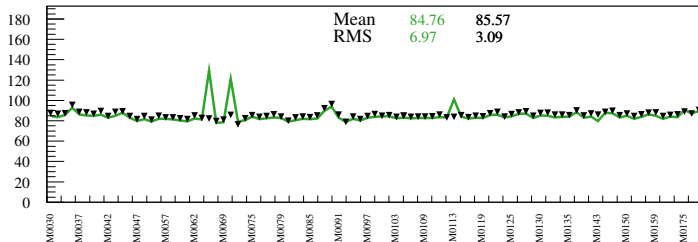


Performance parameters

Mean **VcalThresholdWidth** [e^-] vs. Module Nr.

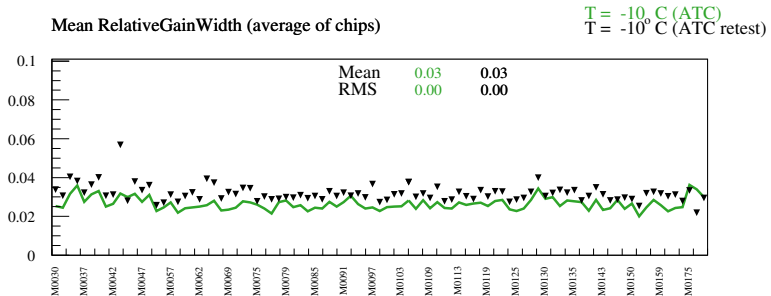
Mean VcalThrWidth (average of chips)

$T = -10^\circ\text{C}$ (ATC)
 $T = -10^\circ\text{C}$ (ATC retest)



Performance parameters

Mean **RelativeGainWidth** [%] vs. Module Nr.



Performance parameters

Mean **PedestalSpread** in [e^-] vs. Module Nr.

Mean PedestalSpread (average of chips)

$T = -10^\circ \text{C}$ (ATC)
 $T = -10^\circ \text{C}$ (ATC retest)

