BPIX Module Testing Status - Week 5

5th February 2007

Production overview

Production Status: 432 modules produced (392 / 40)

- 304/64 graded as A/B → 85%
- 64 graded as C → 15%

Module Testing Report of Week 5:

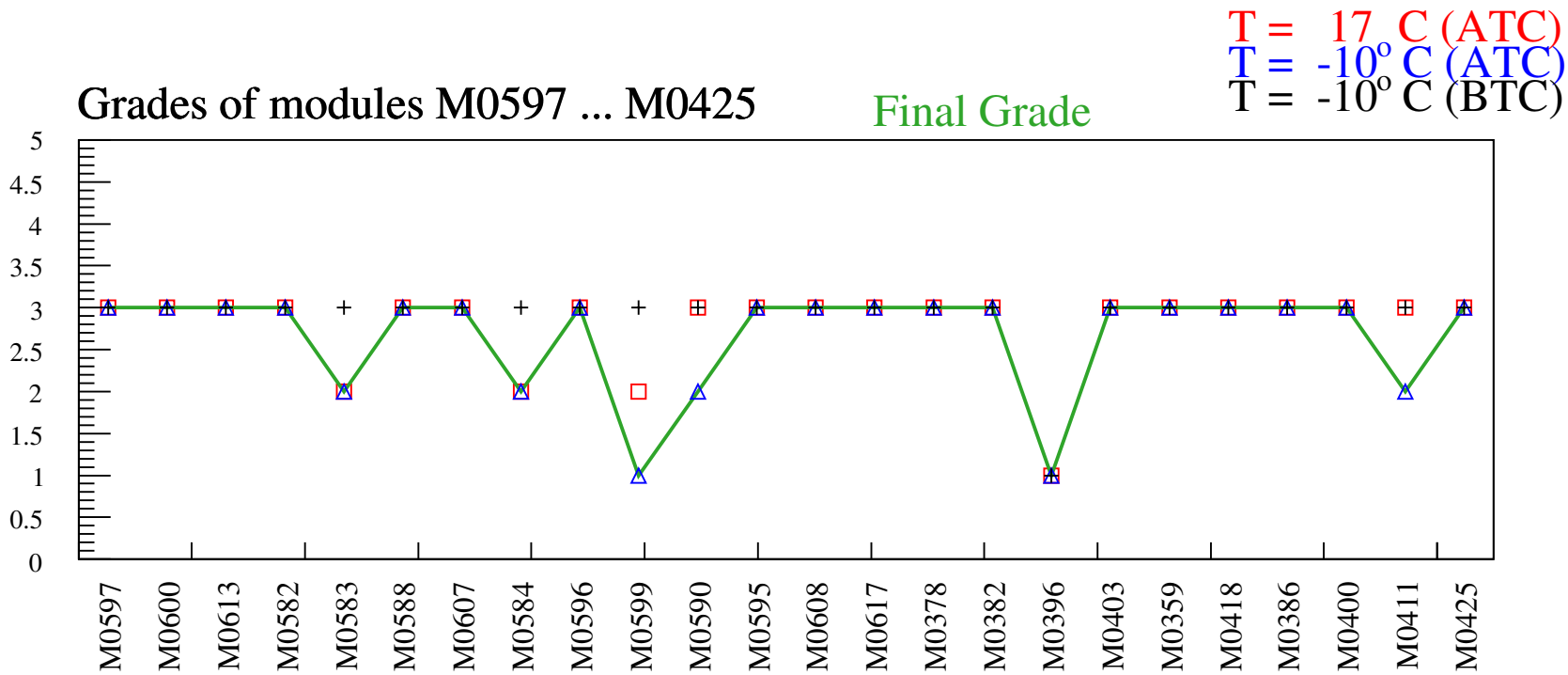
- 14/10 modules fully tested and therm. cycled (0 retested)

	Modules			*Half-Modules*		
Grade	**A**	**B**	**C**	**A**	**B**	**C**
T = -10^o C, BTC*	14	0	0	9	0	1
T = -10^o C, ATC	10	3	1	8	1	1
T = $+17^o$ C, ATC	11	3	0	9	0	1
Final Grade	10	3	1	8	1	1

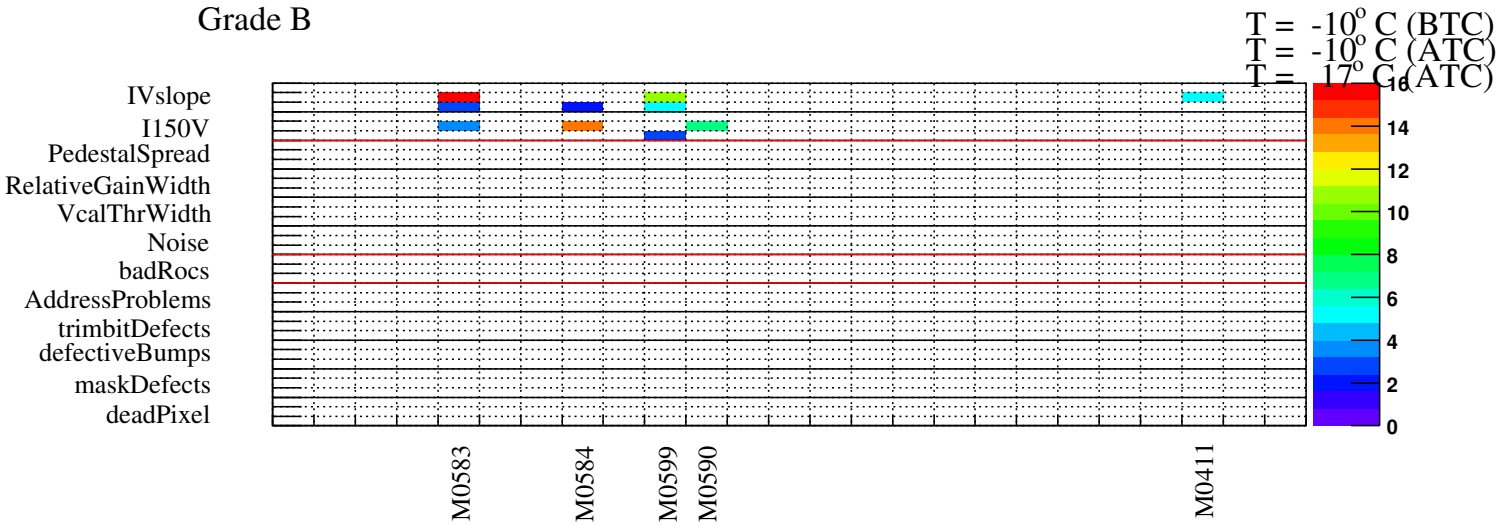
- no retests with new DAC settings

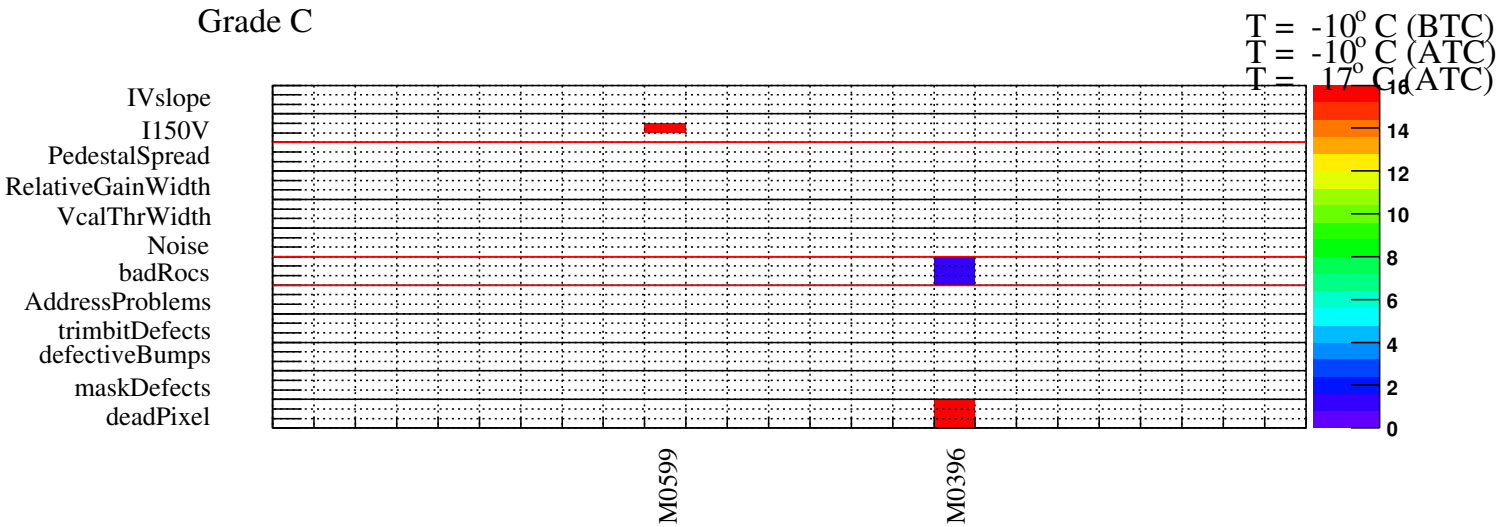
*without IV-criteria

Production summary



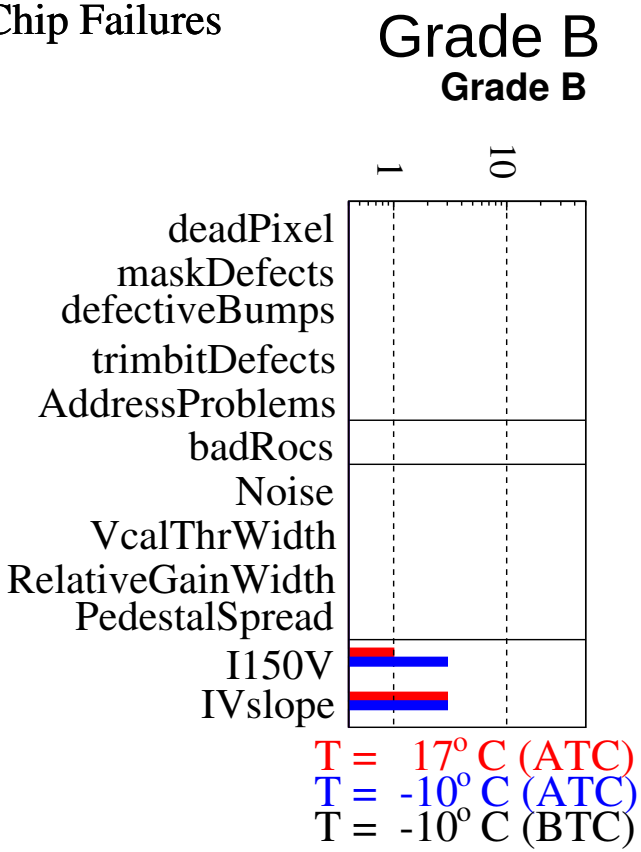
Module Failures Overview

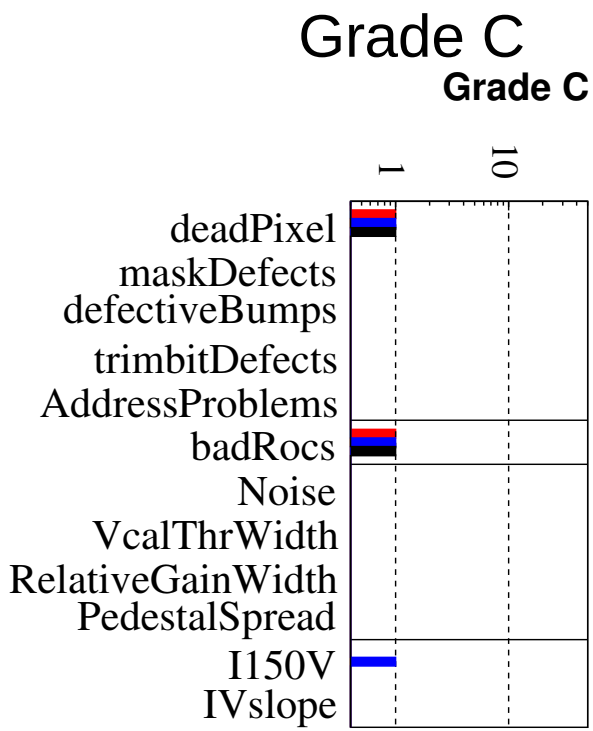




Production quality

Chip Failures





← Pixel defects

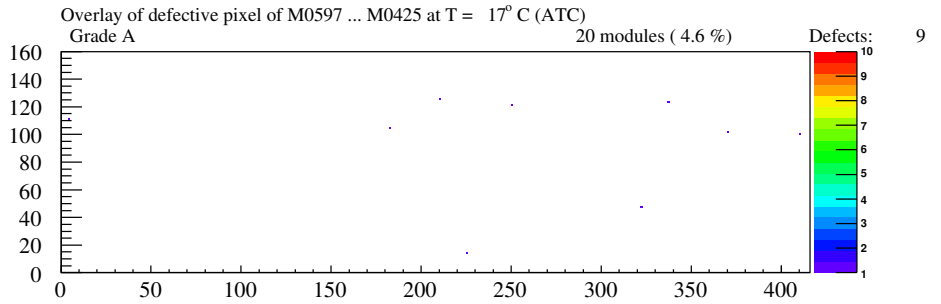
← Chip performance

← Module IV

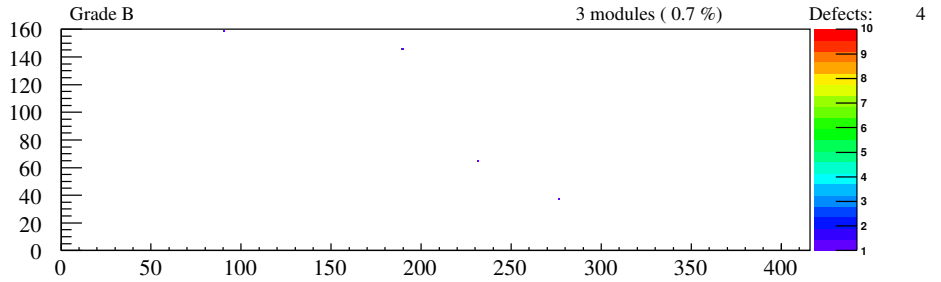
Defective pixel $T = 17^oC$ (ATC)

Overlay of all fully tested modules at T = $+17^o$ C (ATC)

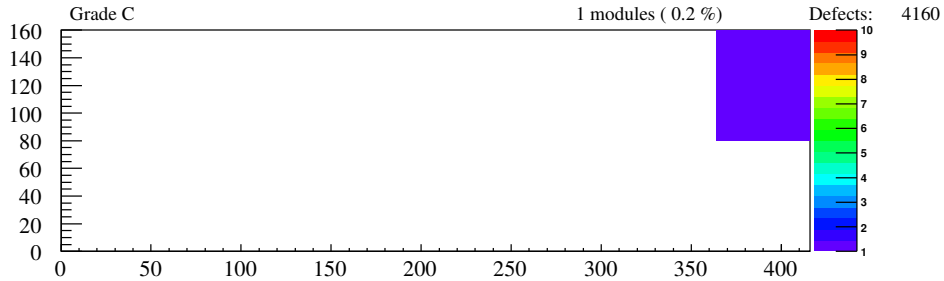
Grade A
(20 modules)



Grade B
(3 modules)



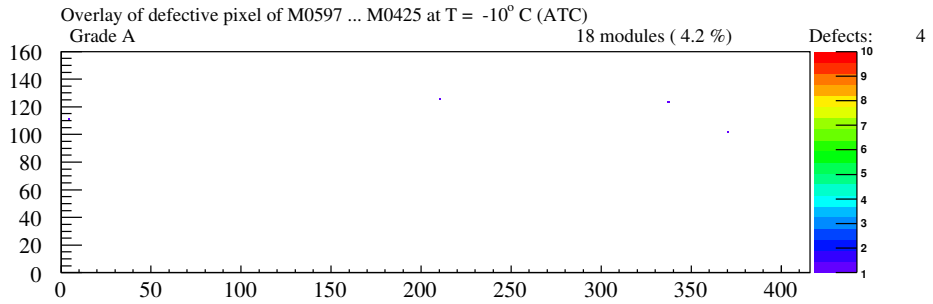
Grade C
(1 modules)



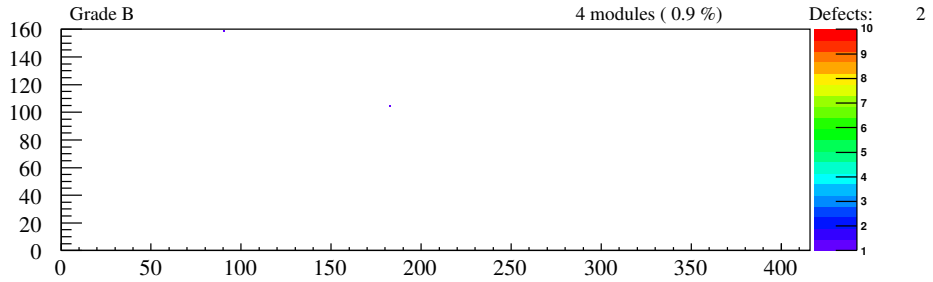
Defective pixel $T = -10^oC$ (ATC)

Overlay of all fully tested modules at T = -10^o C (ATC)

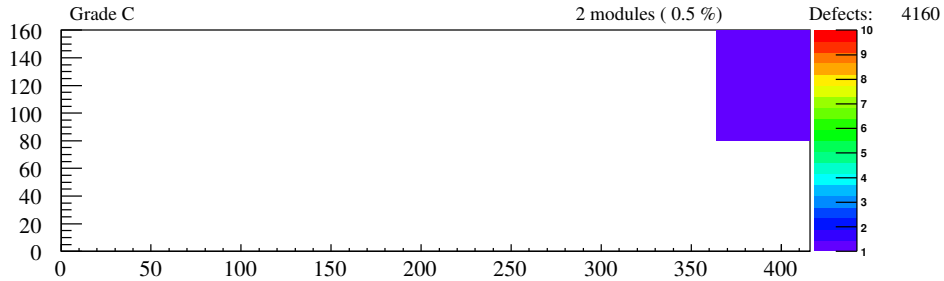
Grade A
(18 modules)



Grade B
(4 modules)



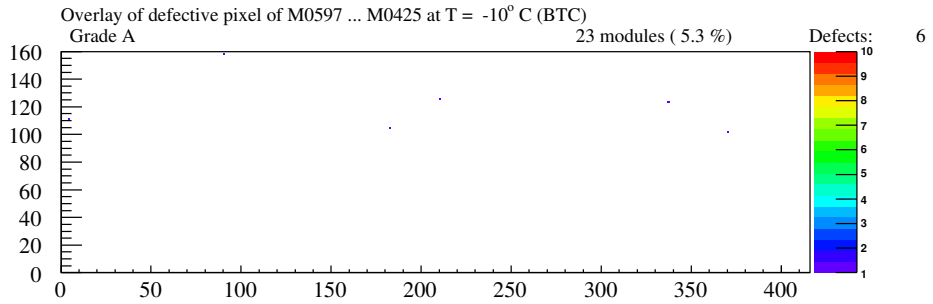
Grade C
(2 modules)



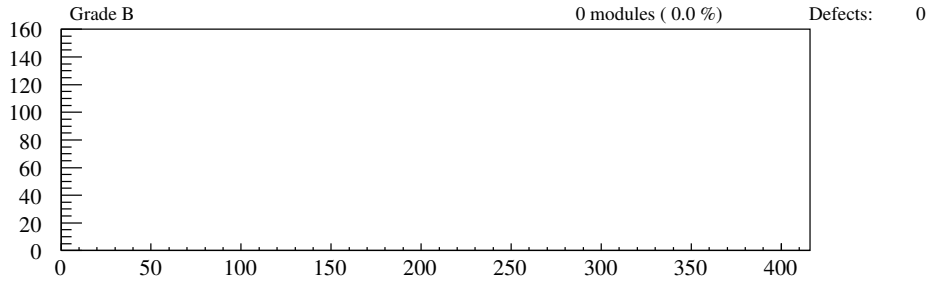
Defective pixel $T = -10^oC$ (BTC)

Overlay of all fully tested modules at T = -10^o C (BTC)

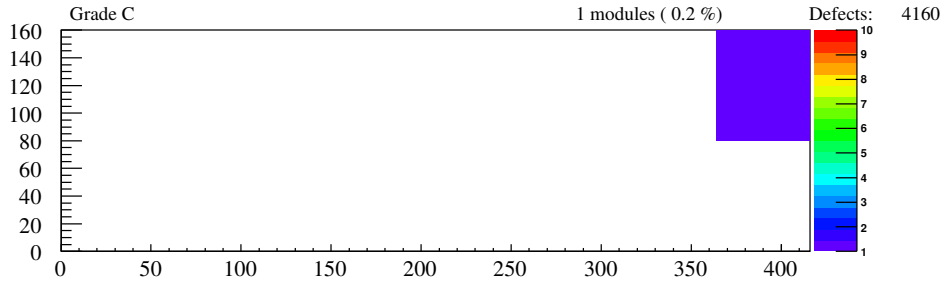
Grade A
(23 modules)



Grade B
(0 modules)



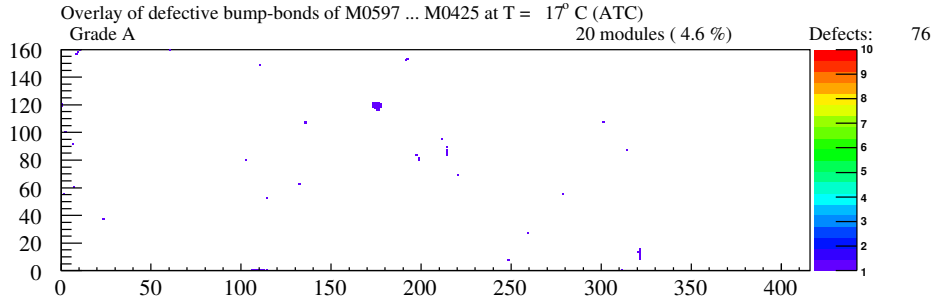
Grade C
(1 modules)



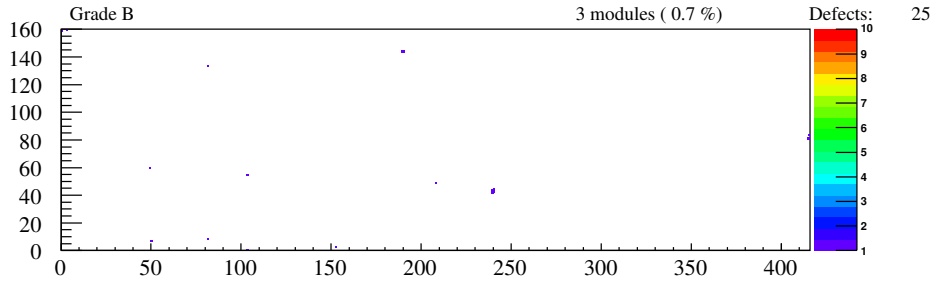
Defective bump-bonds $T = 17^oC$ (ATC)

Overlay of all fully tested modules at T = $+17^o$ C (ATC)

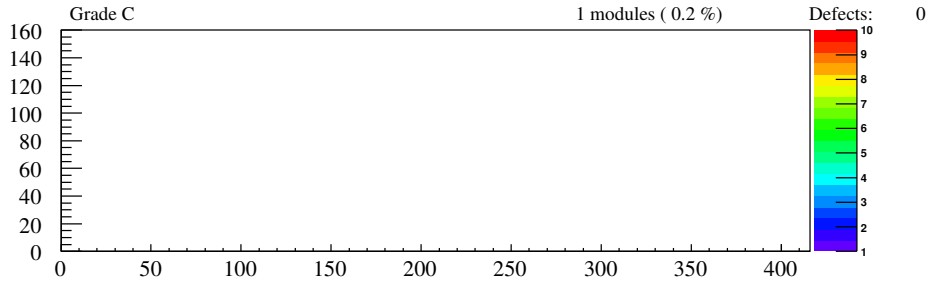
Grade A
(20 modules)



Grade B
(3 modules)



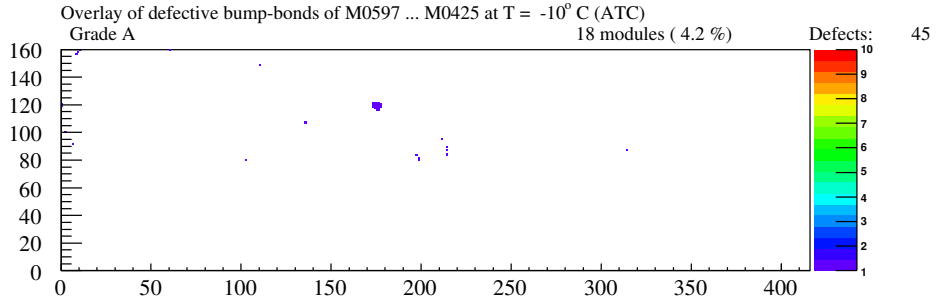
Grade C
(1 modules)



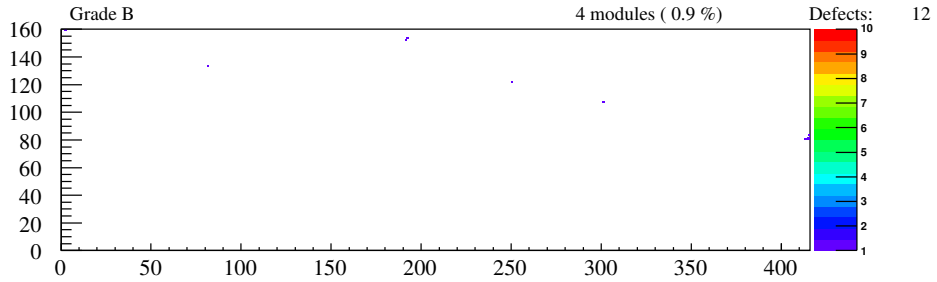
Defective bump-bonds $T = -10^{o}C$ (ATC)

Overlay of all fully tested modules at T = -10^{o} C (ATC)

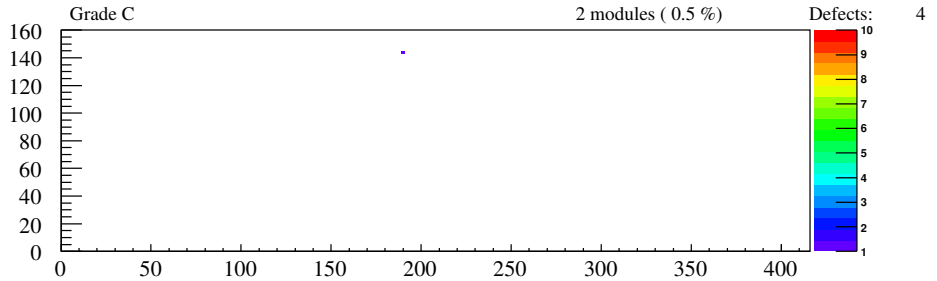
Grade A
(18 modules)



Grade B
(4 modules)



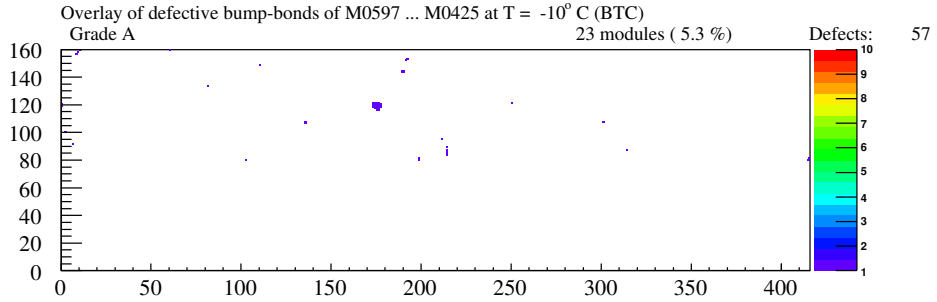
Grade C
(2 modules)



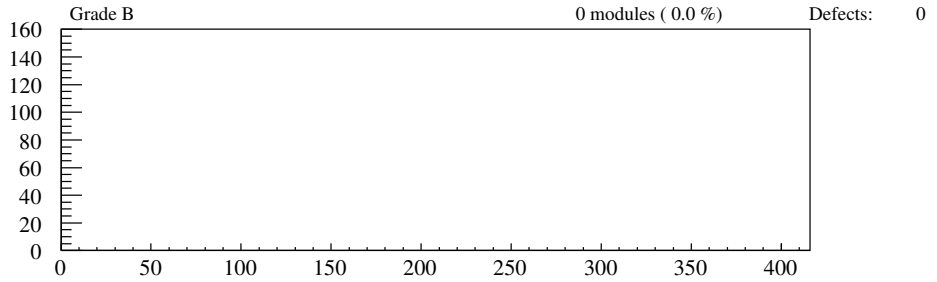
Defective bump-bonds $T = -10^oC$ (BTC)

Overlay of all fully tested modules at T = -10^o C (BTC)

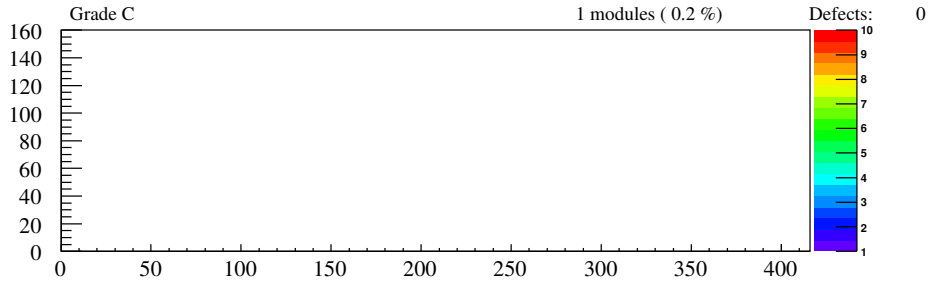
Grade A
(23 modules)



Grade B
(0 modules)

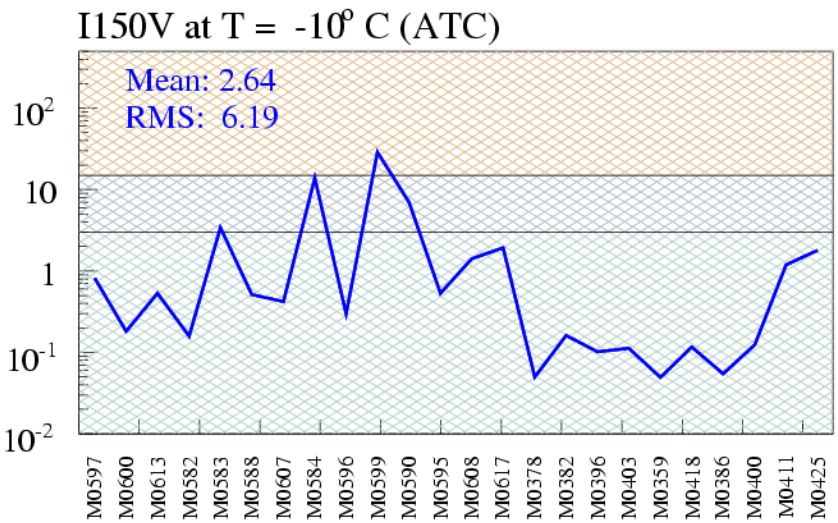


Grade C
(1 modules)

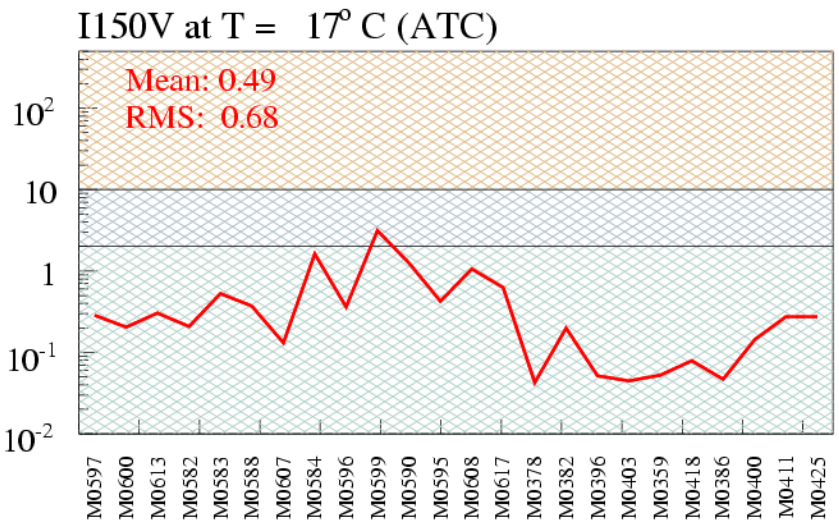


Current at 150 V

Current at 150 V (in μA) at $T = 17^oC$ and $T = -10^oC$



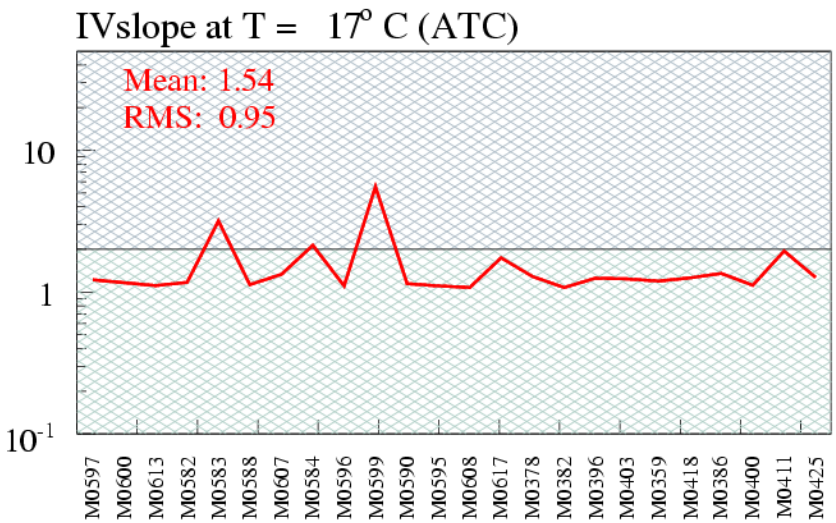
recalculated

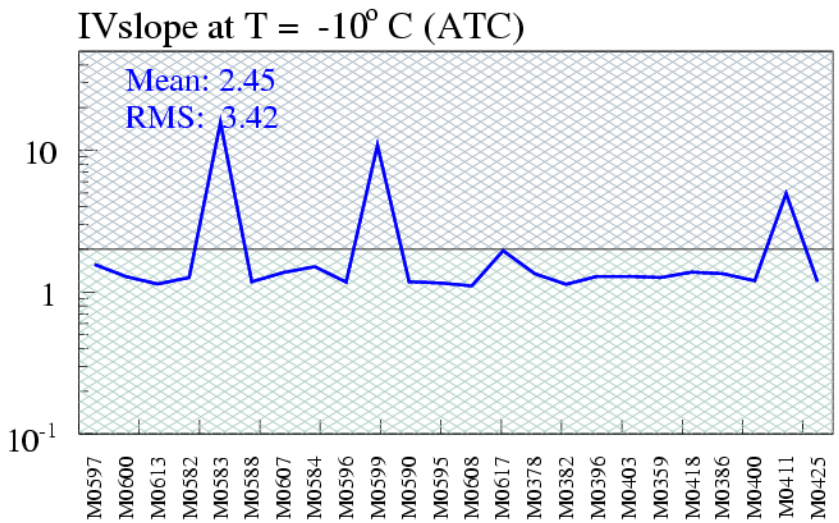


measured

Slope of IV-Curve

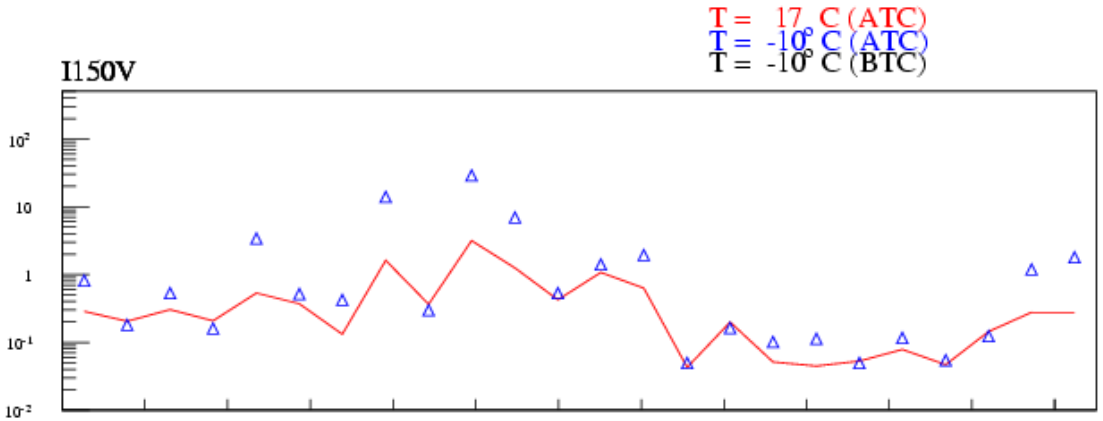
Slope of IV-Curveat $T = 17^oC$ and $T = -10^oC$

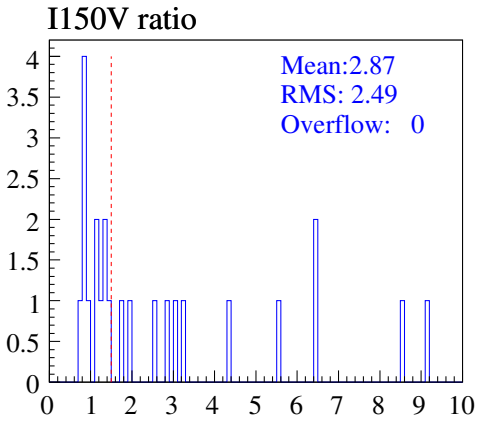


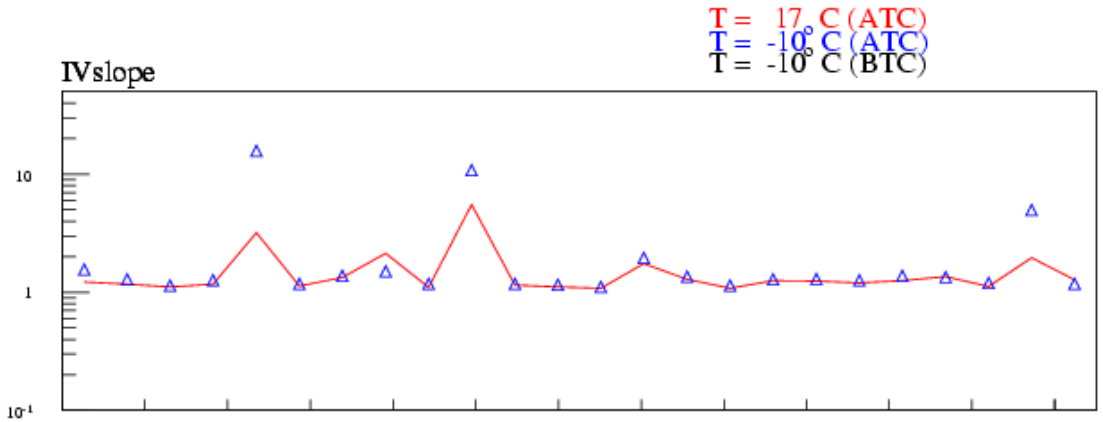


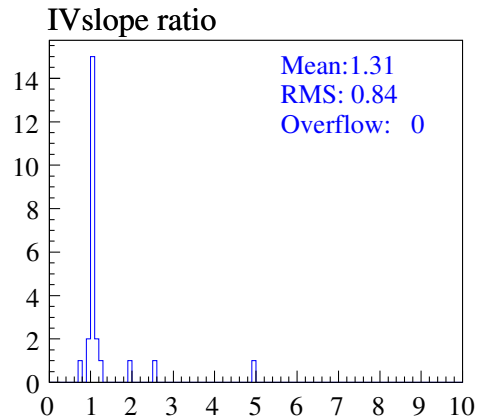
Current recalculation to $T = 17^oC$

Cross check of recalculated values with measured values



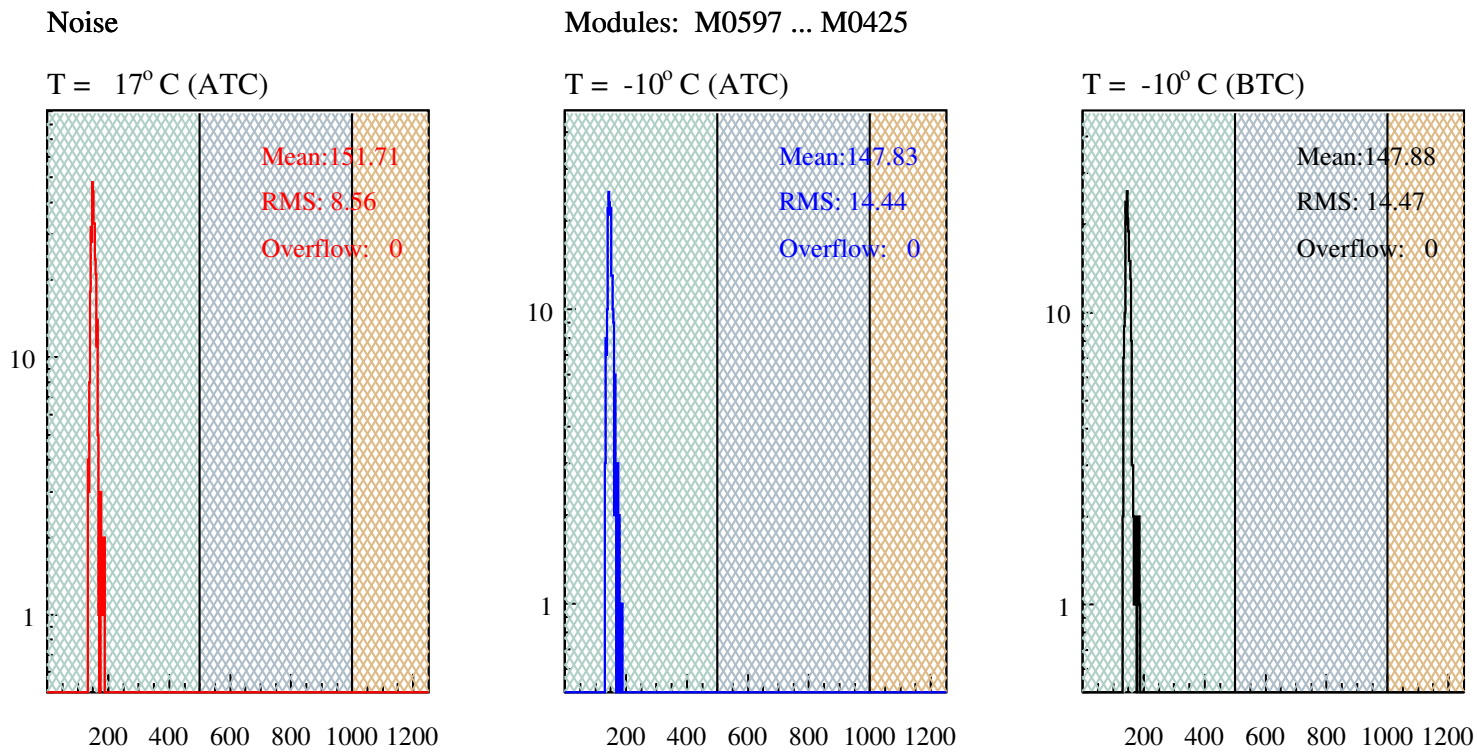






Noise

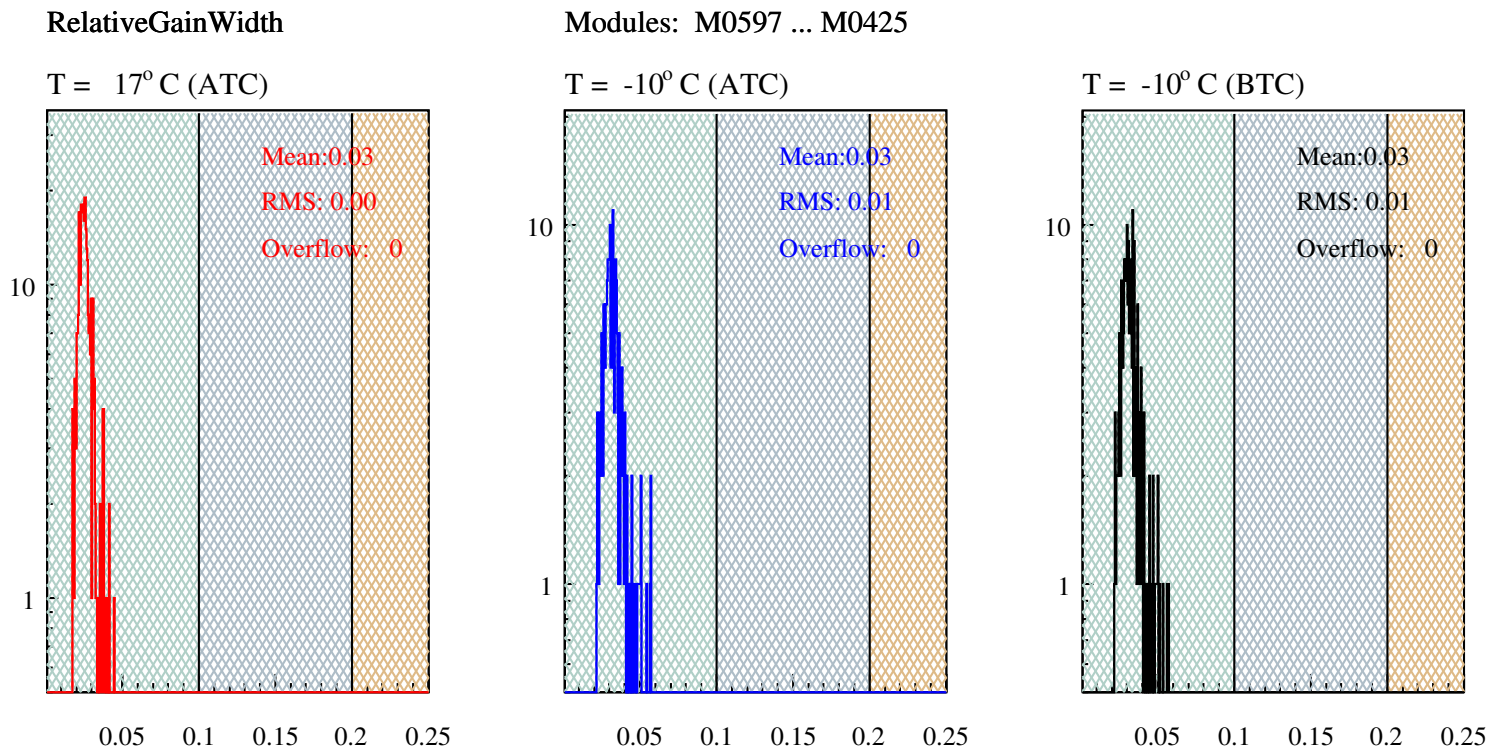
MeanNoise of chips



Noise in e^-

Relative Gain Width

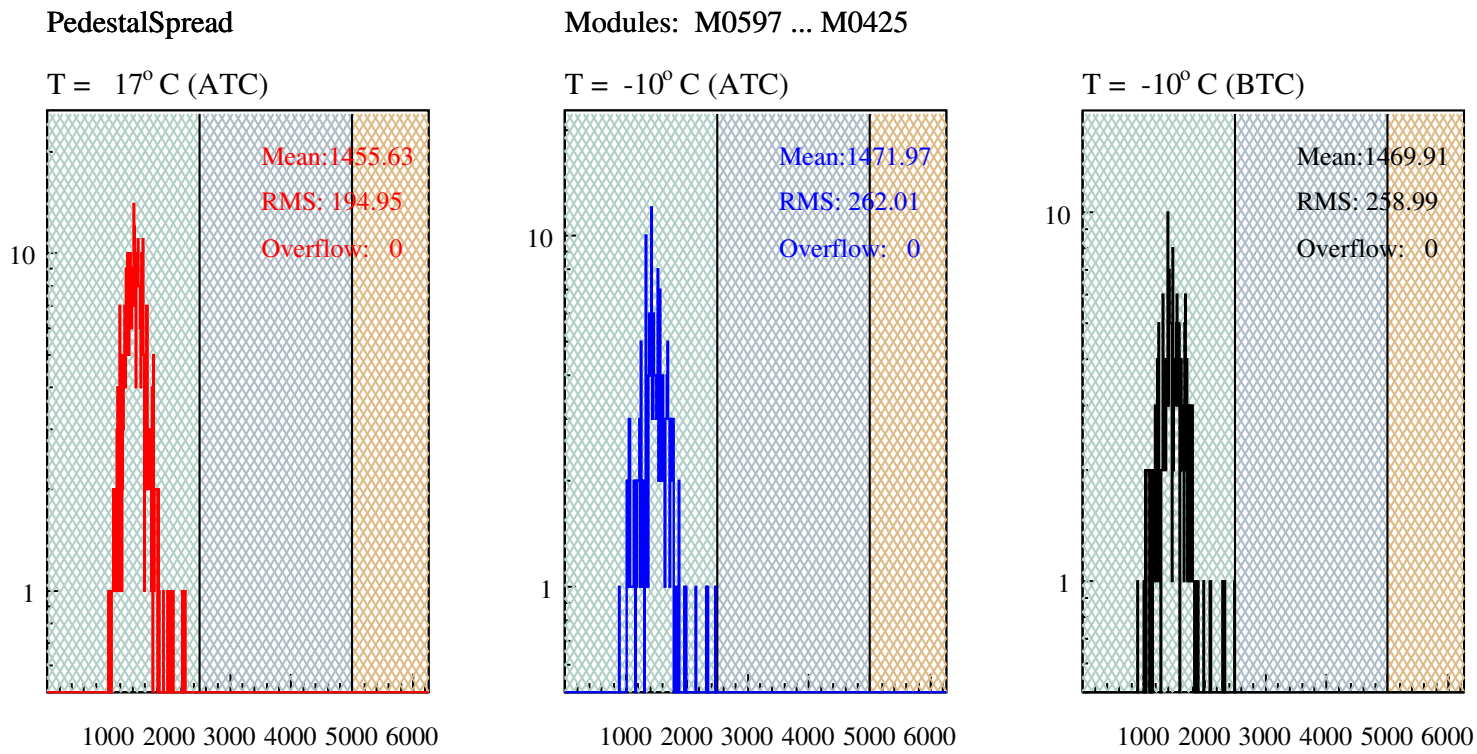
RelativeGainWidth of chips



Rel. Gain Width in %

Pedestal Spread

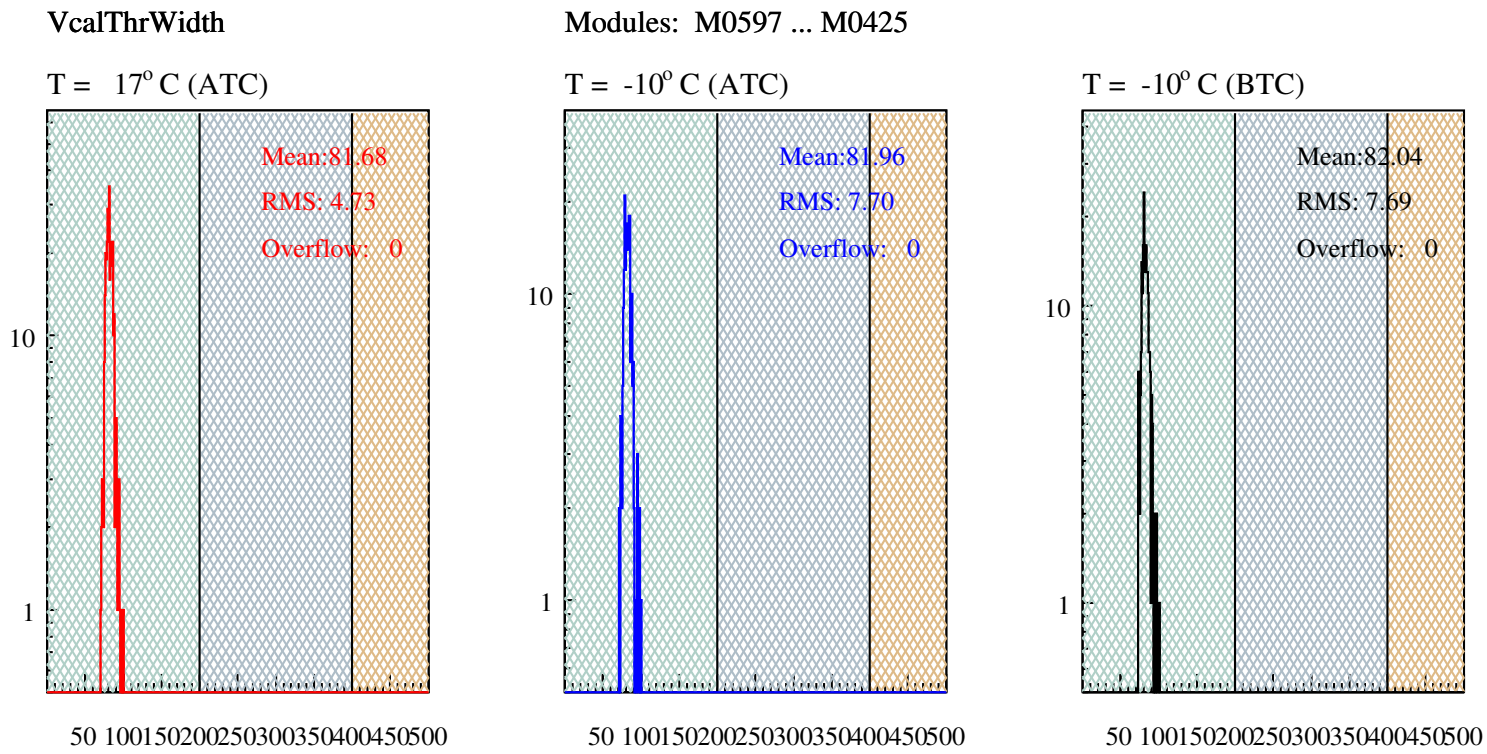
PedestalSpread of chips



Pedestal Spread in e^-

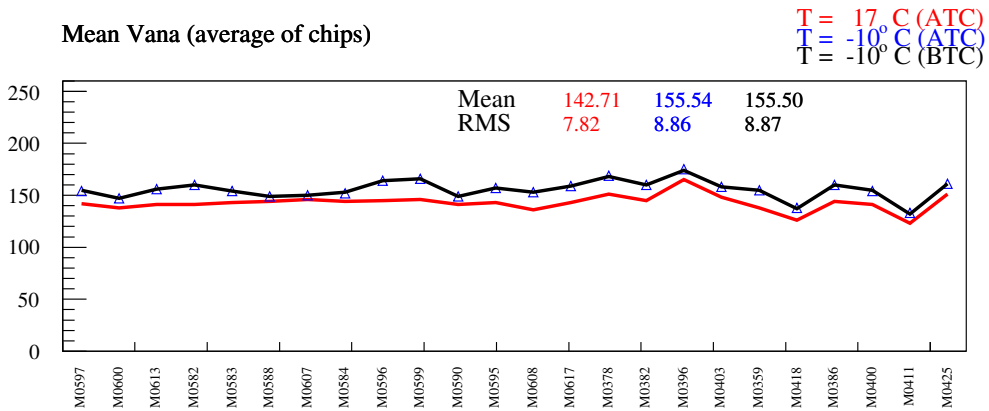
Vcal Threshold Width

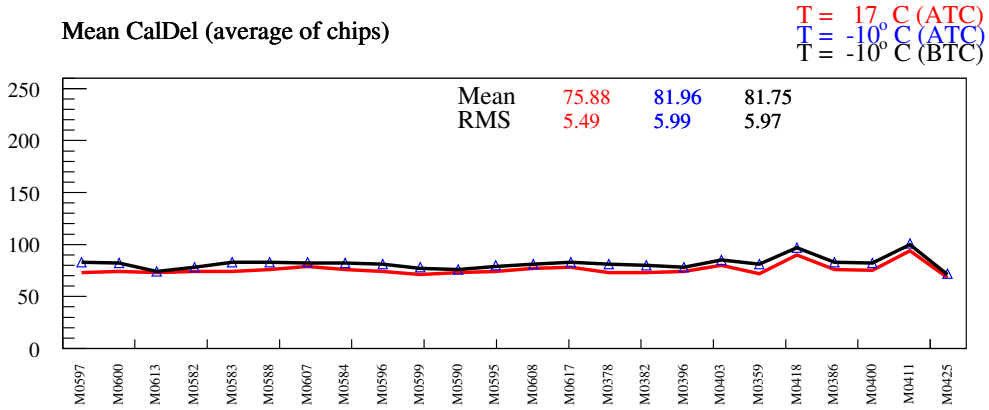
VcalThresholdWidth of chips



Operational parameters I

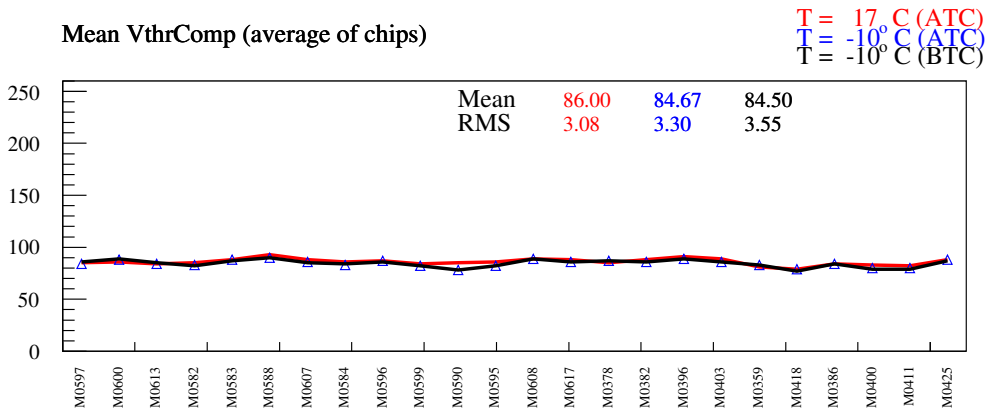
Mean DACs I

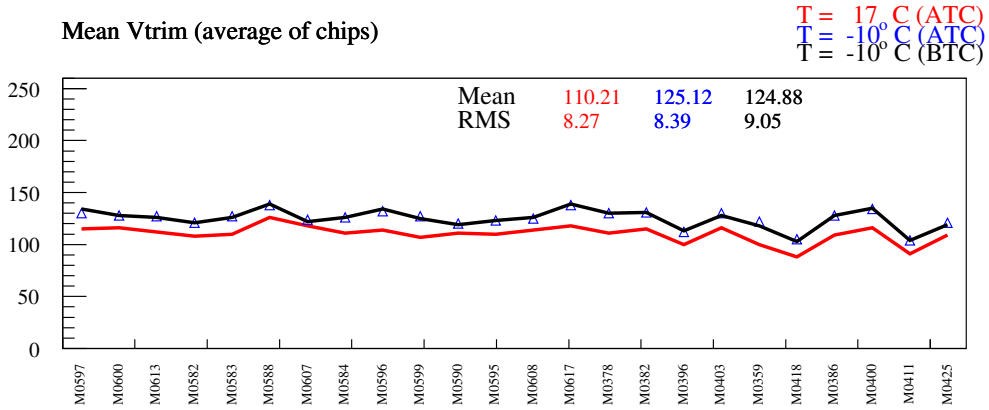




Operational parameters II

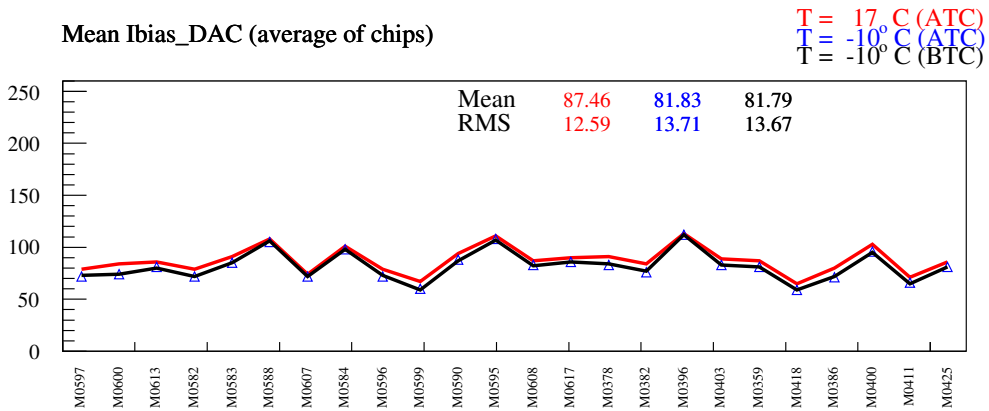
Mean DACs II

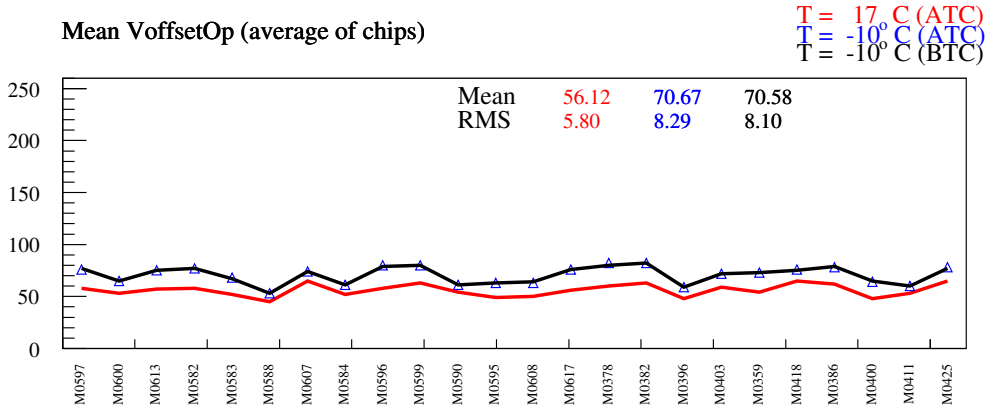




Operational parameters III

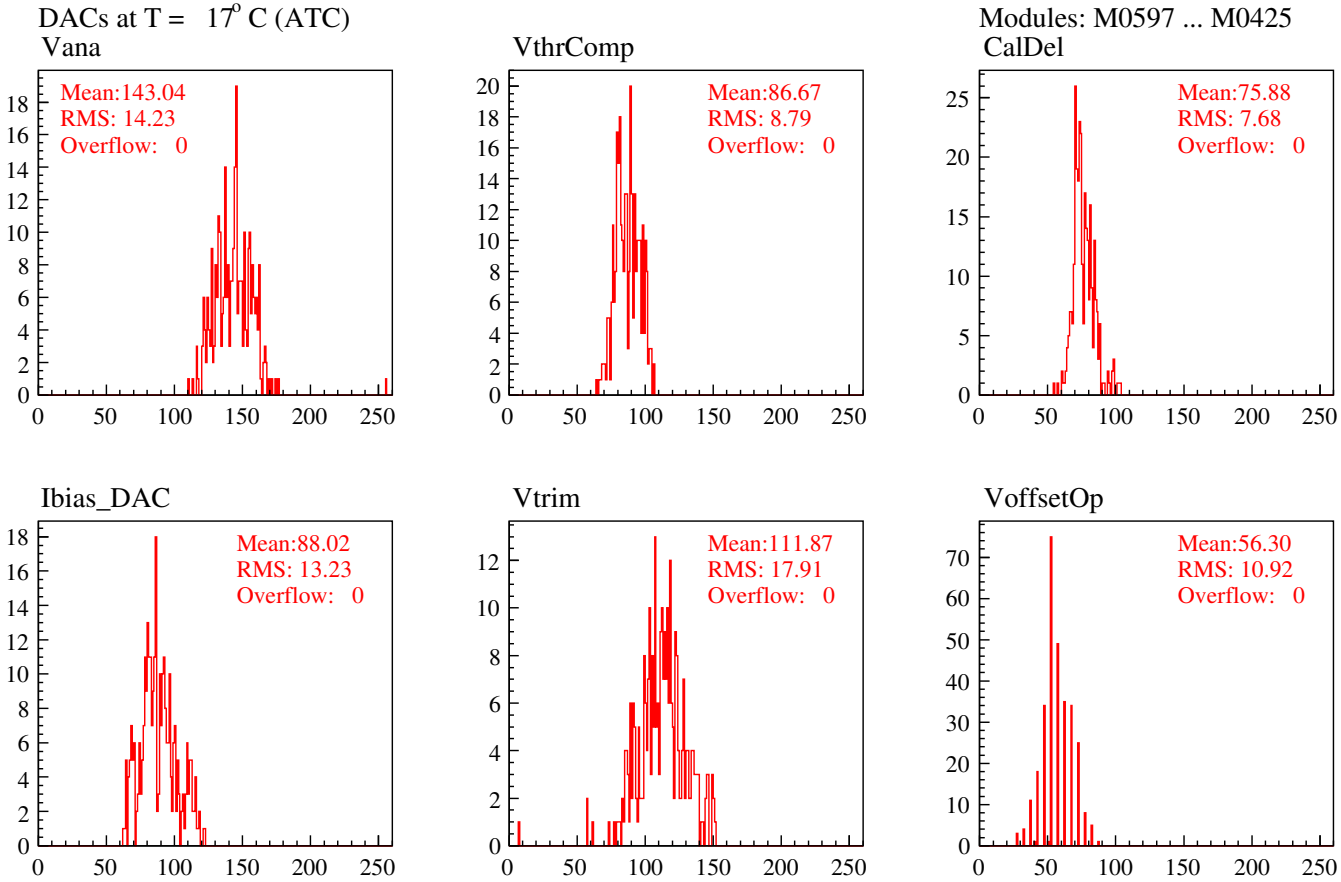
Mean DACs III





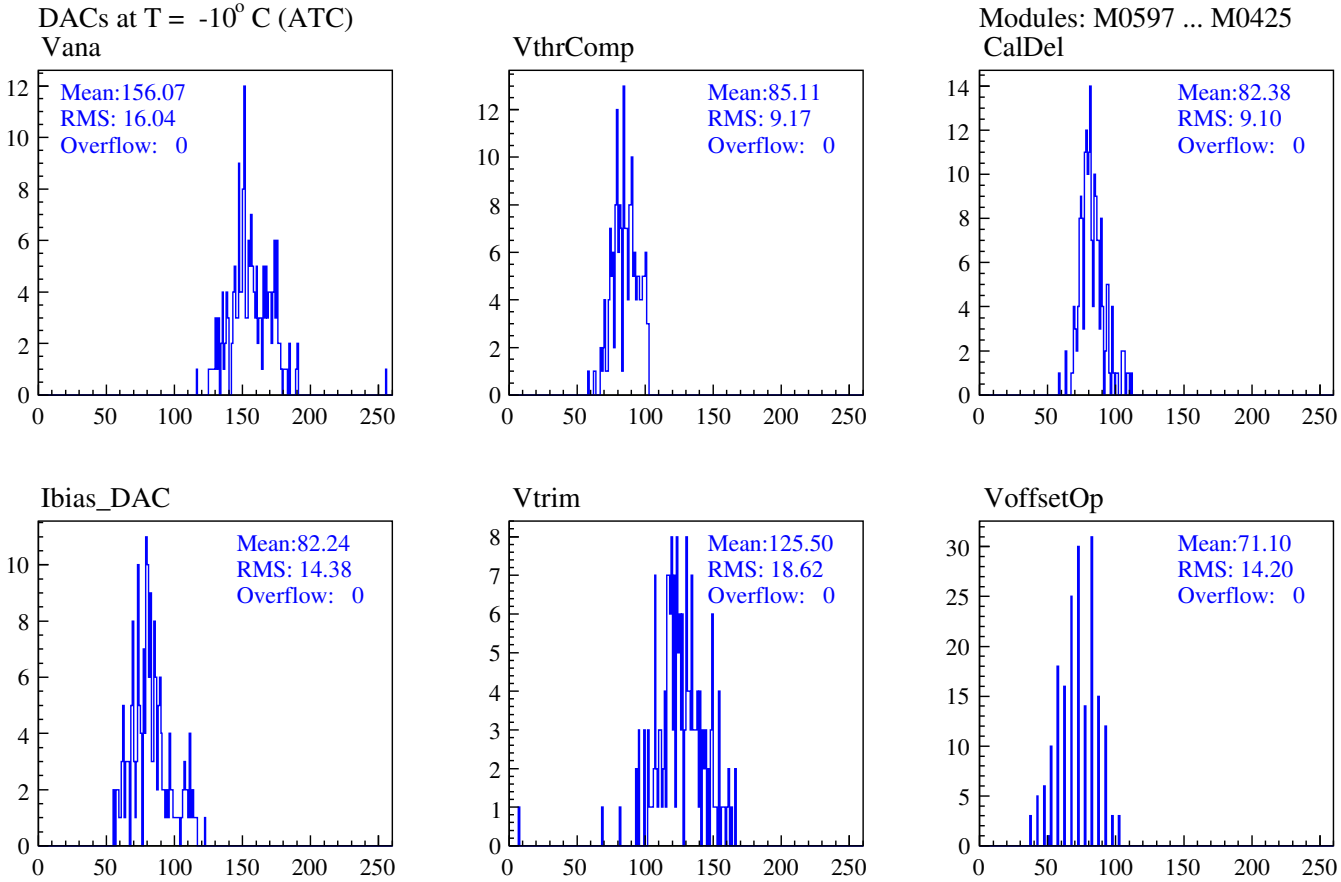
Operational parameters at $T = +17^{o}C$ (ATC)

DAC distribution (of chips)



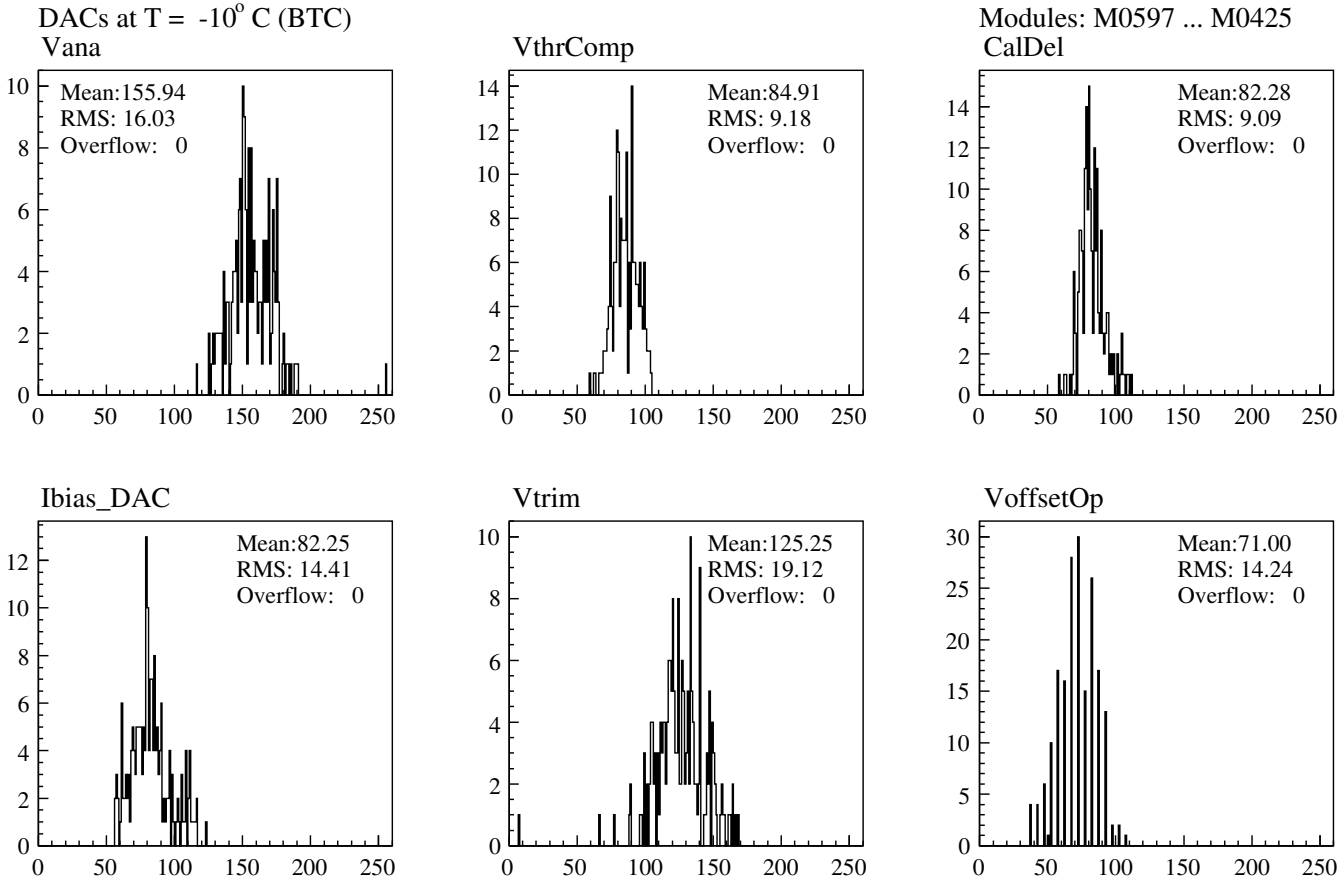
Operational parameters at $T = -10^oC$ (ATC)

DAC distribution (of chips)

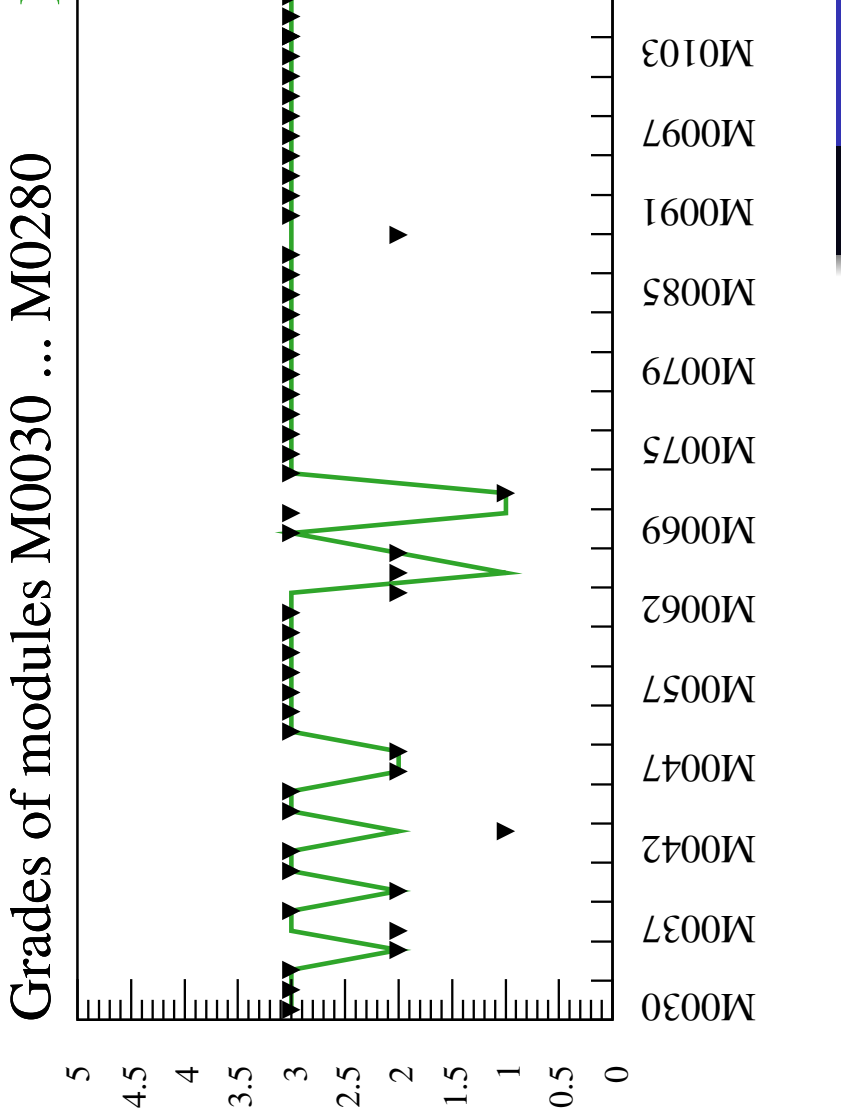


Operational parameters at $T = +17^oC$ (BTC)

DAC distribution (of chips)

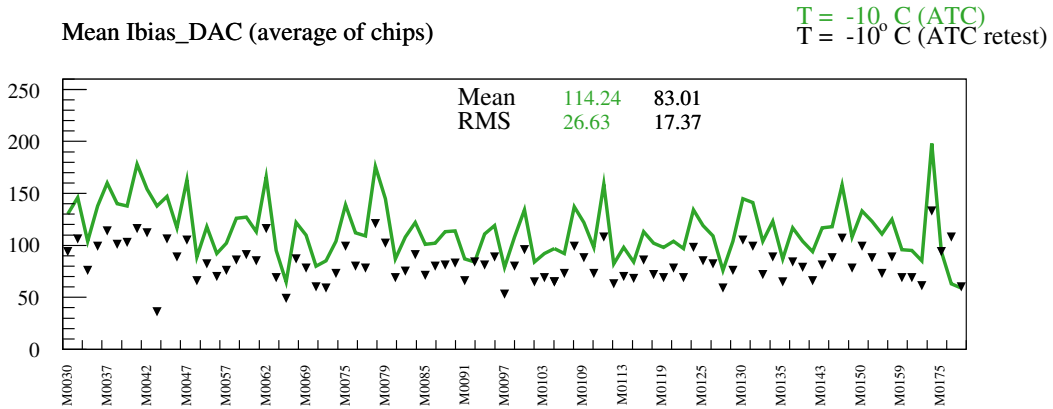


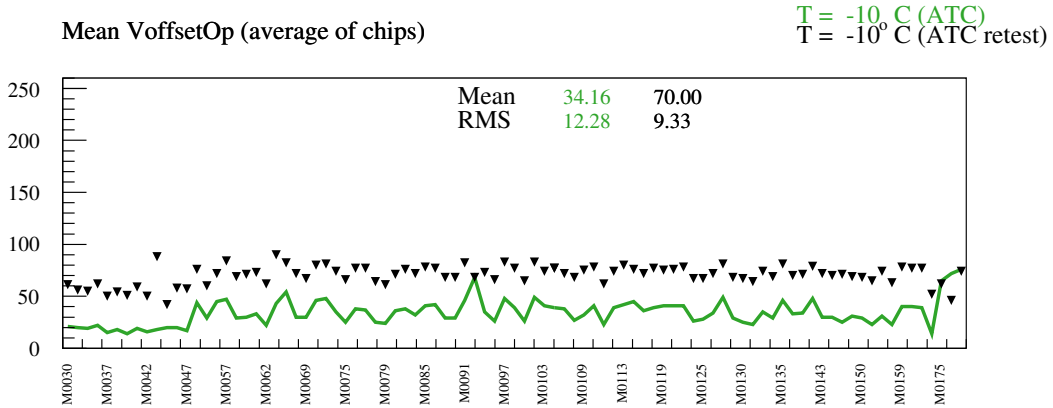
Retest Grades



Operational parameters

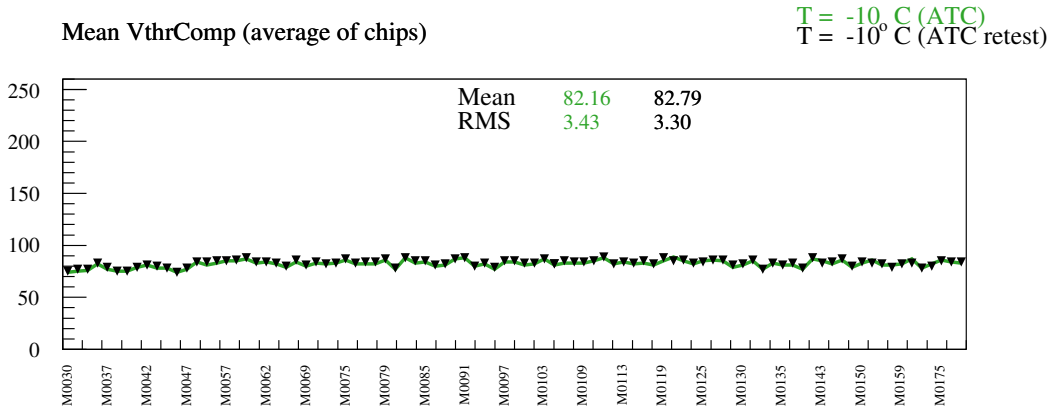
Mean DACs I

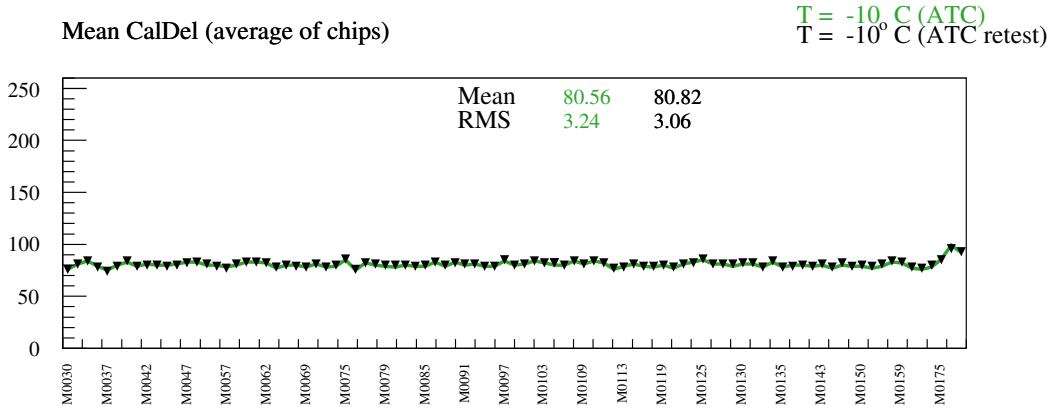




Operational parameters

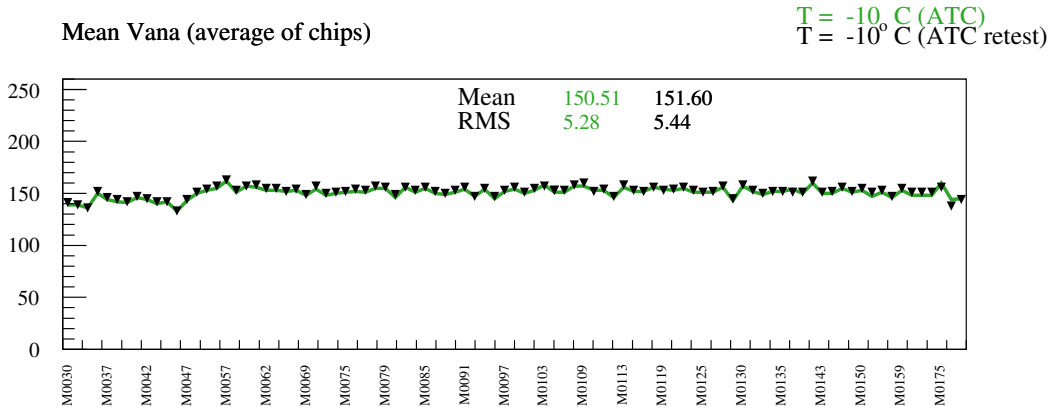
Mean DACs II

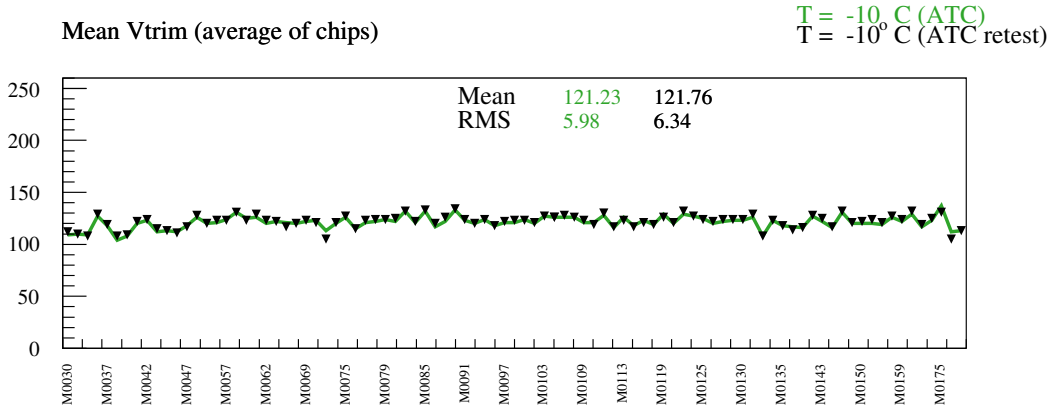




Operational parameters

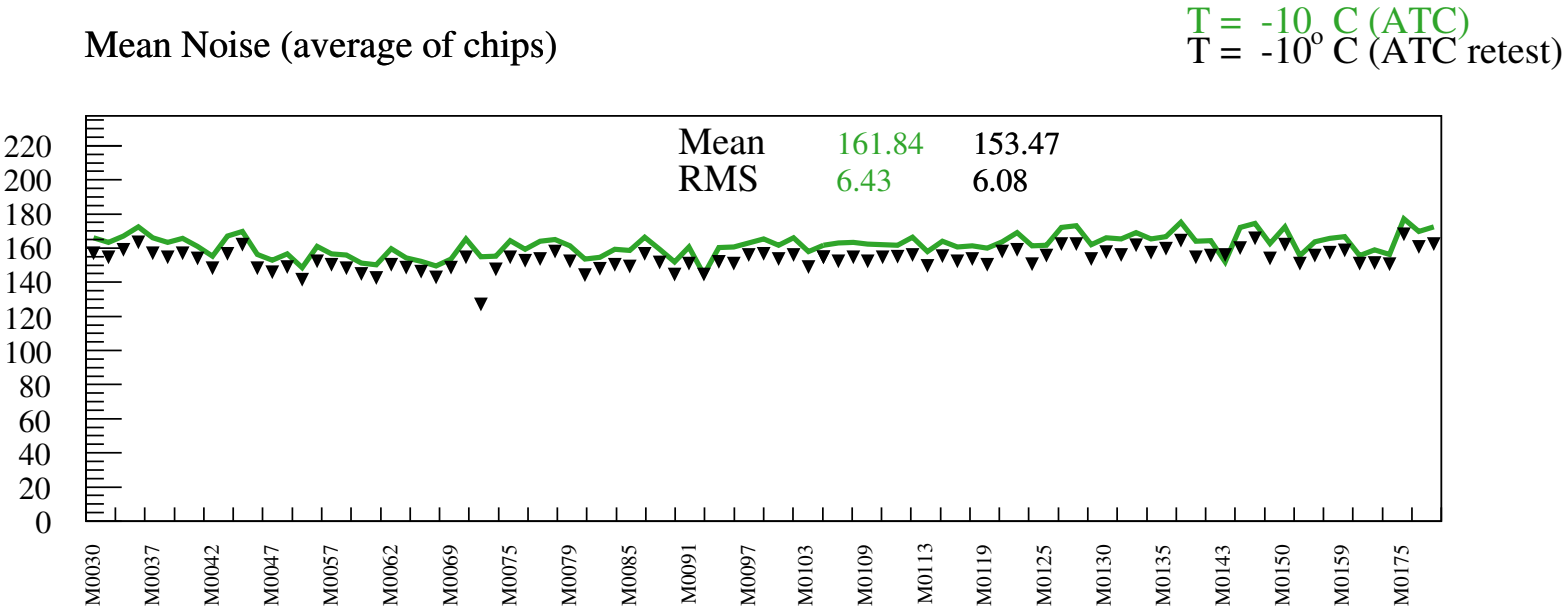
Mean DACs III





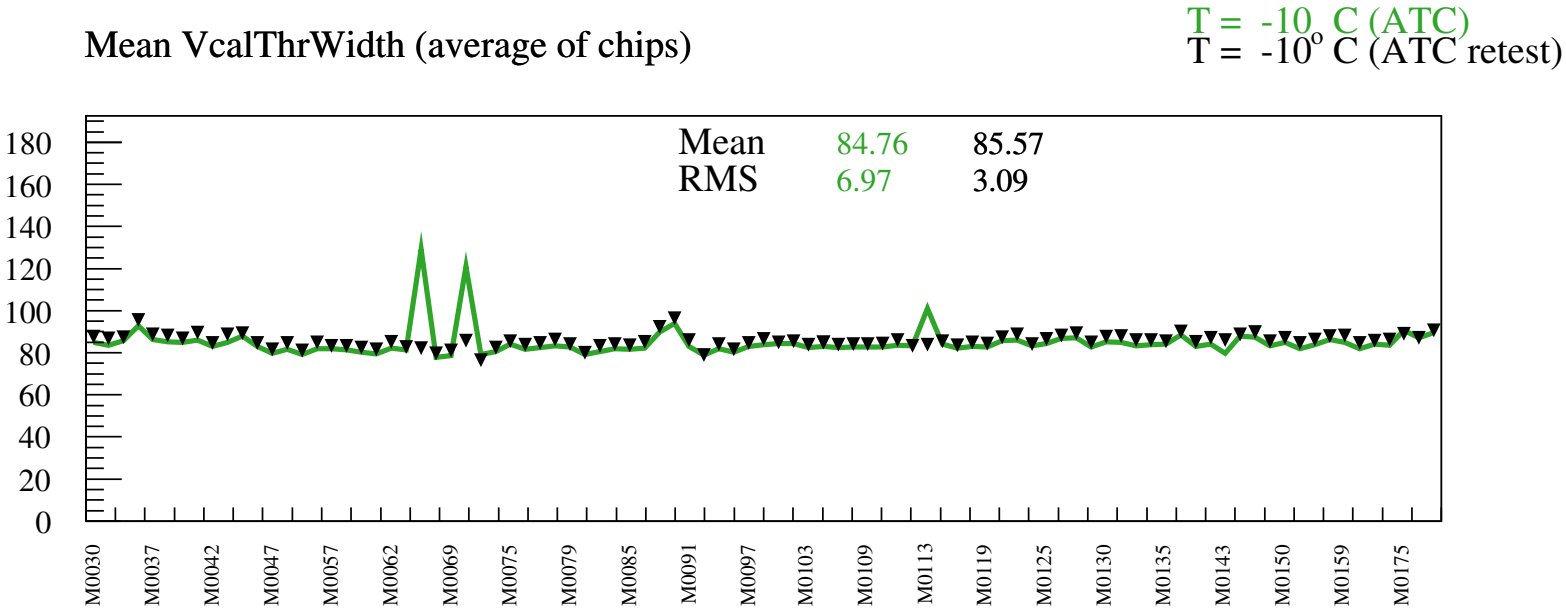
Performance parameters

Mean **Noise** [e^-] vs. Module Nr.



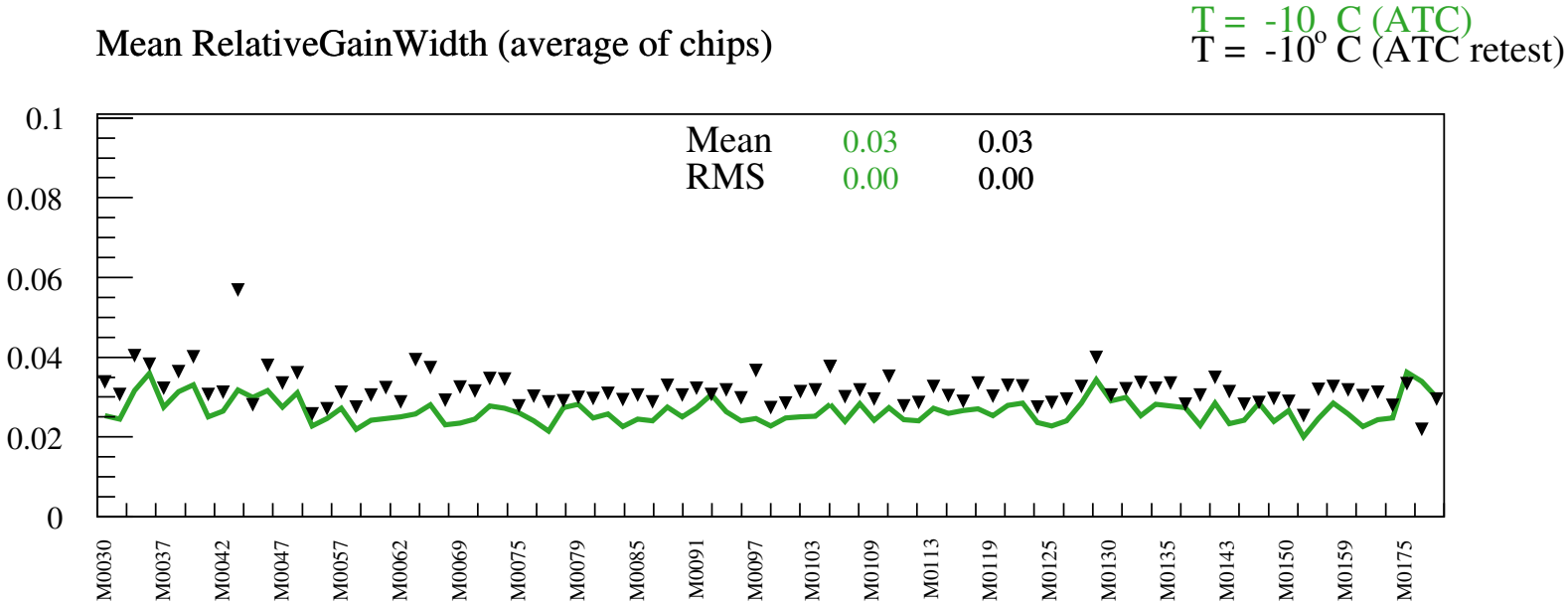
Performance parameters

Mean **VcalThresholdWidth** [e^-] vs. Module Nr.



Performance parameters

Mean **RelativeGainWidth** [%] vs. Module Nr.



Performance parameters

Mean **PedestalSpread** in [e^-] vs. Module Nr.