

BPIX Module Testing Status - Week 30

10th January 2007

Production overview

Production Status: 115 modules produced (112 / 3)

- 72/12 graded as A/B → 73%
- 31 graded as C → 27%

Module Testing Report of Week 30:

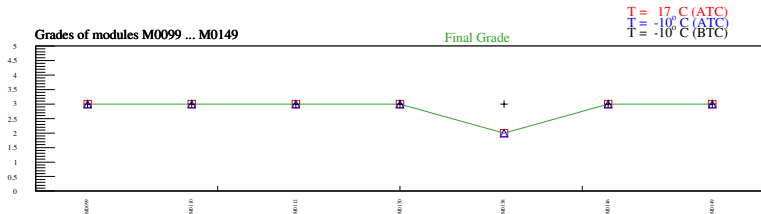
- 7/— modules fully tested and therm. cycled (4 retested)

	<i>Modules</i>			<i>Half-Modules</i>		
Grade	A	B	C	A	B	C
T = -10° C, BTC*	7	0	0	—	—	—
T = -10° C, ATC	6	1	0	—	—	—
T = $+17^{\circ}$ C, ATC	6	1	0	—	—	—
Final Grade	6	1	0	—	—	—

- no retests with new DAC settings

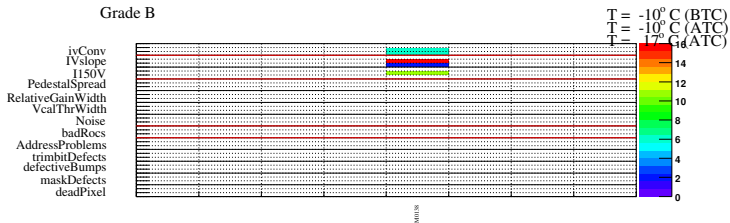
*without IV-criteria

Production summary

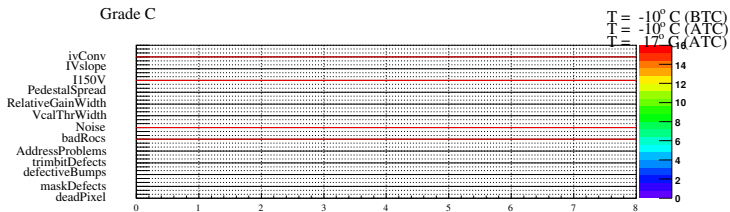


Module Failures Overview

Grade B

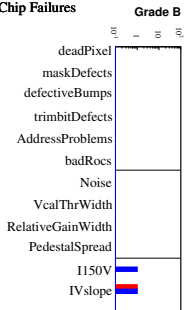


Grade C



Grade B

Chip Failures

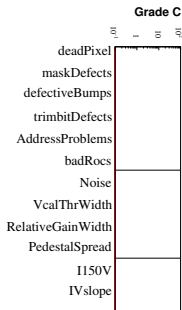


T = 17° C (ATC)

T = -10° C (ATC)

T = -10° C (BTC)

Grade C Failures



← Pixel defects

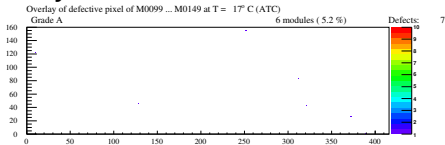
← Chip performance

← Module IV

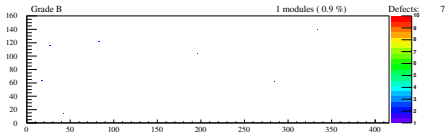
Defective pixel $T = 17^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = +17^{\circ}\text{C}$ (ATC)

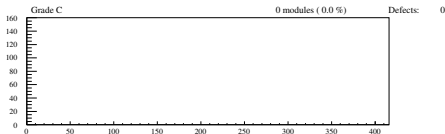
Grade A
(6 modules)



Grade B
(1 modules)



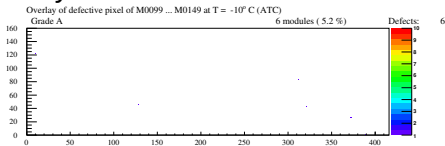
Grade C
(0 modules)



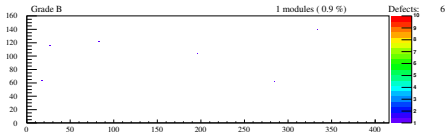
Defective pixel $T = -10^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (ATC)

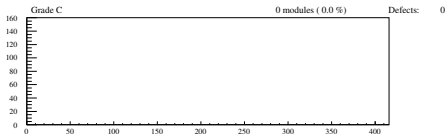
Grade A
(6 modules)



Grade B
(1 modules)



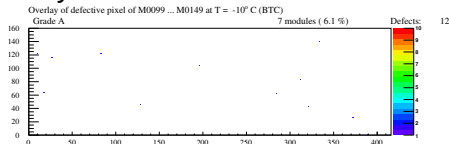
Grade C
(0 modules)



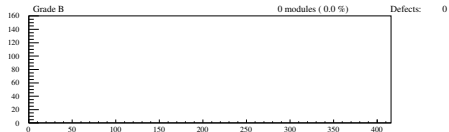
Defective pixel $T = -10^{\circ}\text{C}$ (BTC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (BTC)

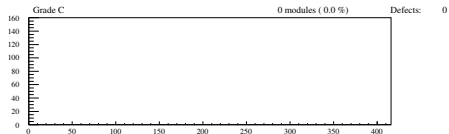
Grade A
(7 modules)



Grade B
(0 modules)



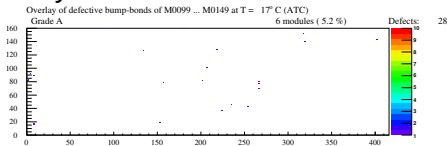
Grade C
(0 modules)



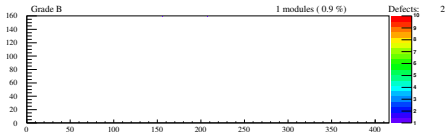
Defective bump-bonds $T = 17^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = +17^{\circ}\text{C}$ (ATC)

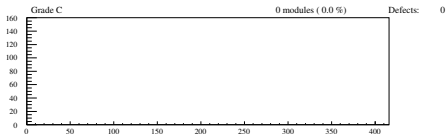
Grade A
(6 modules)



Grade B
(1 modules)



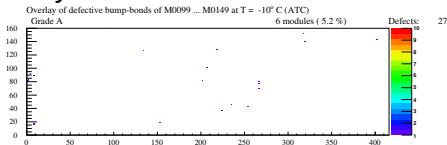
Grade C
(0 modules)



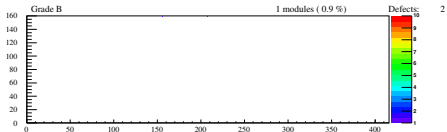
Defective bump-bonds $T = -10^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (ATC)

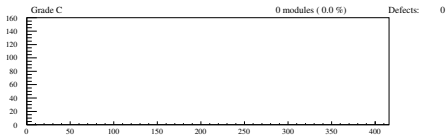
Grade A
(6 modules)



Grade B
(1 modules)



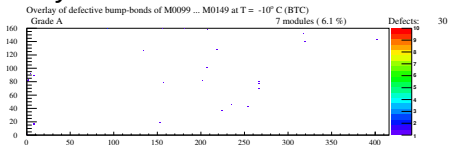
Grade C
(0 modules)



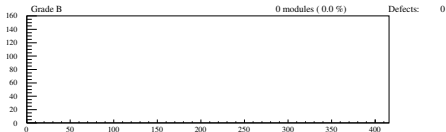
Defective bump-bonds $T = -10^{\circ}\text{C}$ (BTC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (BTC)

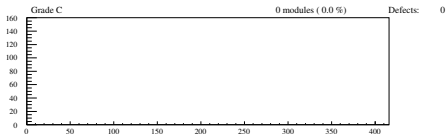
Grade A
(7 modules)



Grade B
(0 modules)



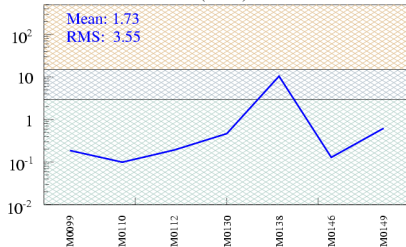
Grade C
(0 modules)



Current at 150 V

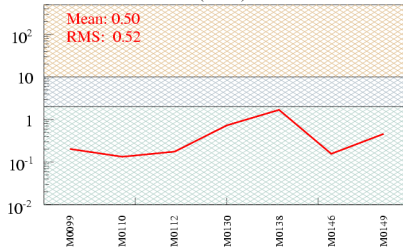
Current at 150 V (in μA) at $T = 17^\circ\text{C}$ and $T = -10^\circ\text{C}$

I150V at $T = -10^\circ\text{C}$ (ATC)



recalculated

I150V at $T = 17^\circ\text{C}$ (ATC)

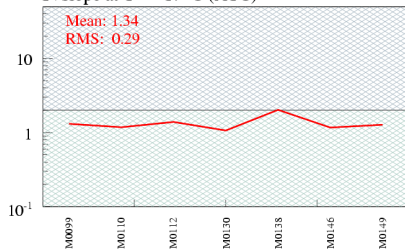


measured

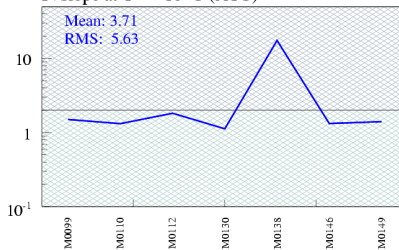
Slope of IV-Curve

Slope of IV-Curve at $T = 17^{\circ}\text{C}$ and $T = -10^{\circ}\text{C}$

IVslope at $T = 17^{\circ}\text{C}$ (ATC)



IVslope at $T = -10^{\circ}\text{C}$ (ATC)

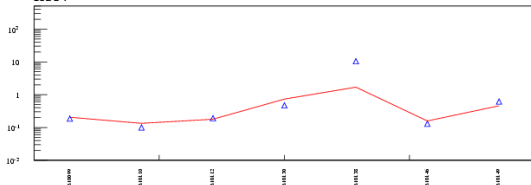


Current recalculation to $T = 17^{\circ}\text{C}$

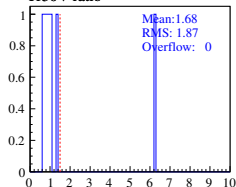
Cross check of recalculated values with measured values

$T = 17^{\circ}\text{C}$ (ATC)
 $T = -10^{\circ}\text{C}$ (ATC)
 $T = -10^{\circ}\text{C}$ (BTC)

I150V

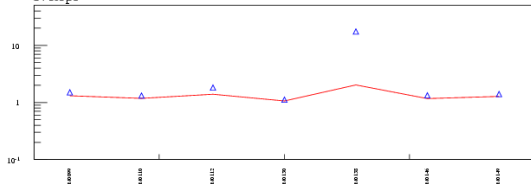


I150V ratio

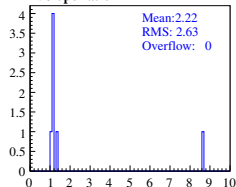


$T = 17^{\circ}\text{C}$ (ATC)
 $T = -10^{\circ}\text{C}$ (ATC)
 $T = -10^{\circ}\text{C}$ (BTC)

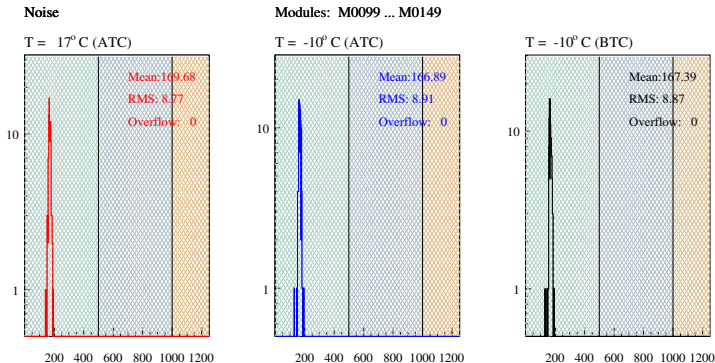
IVslope



IVslope ratio

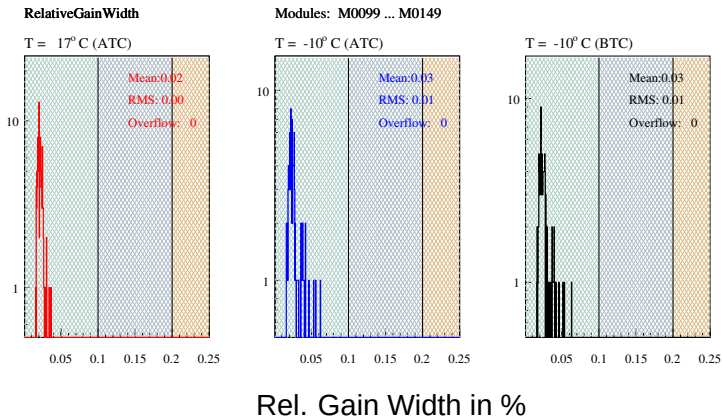


MeanNoise of chips

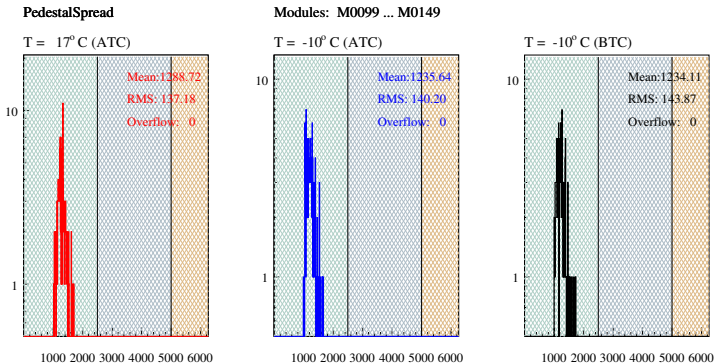


Relative Gain Width

RelativeGainWidth of chips



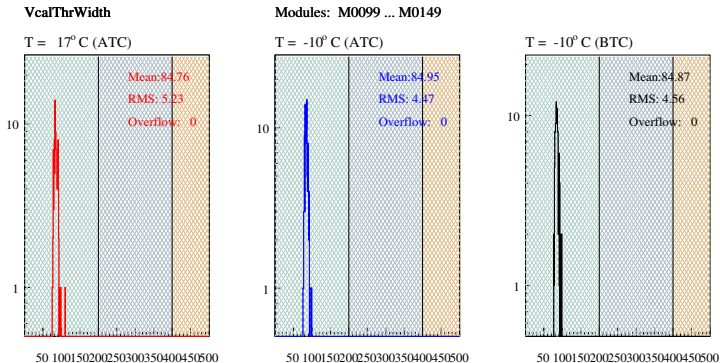
PedestalSpread of chips



Pedestal Spread in e^-

Vcal Threshold Width

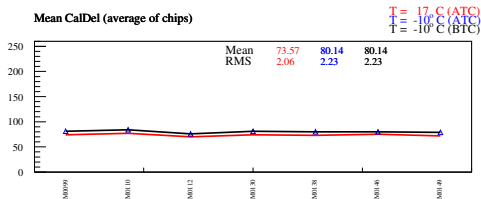
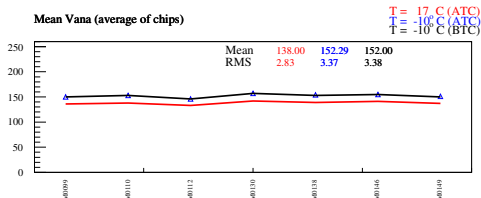
VcalThresholdWidth of chips



Vcal Thr. Width in e^-

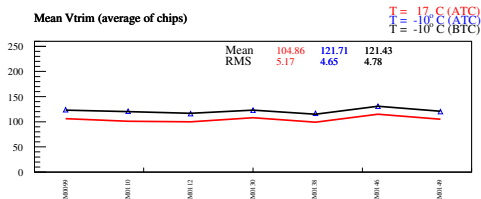
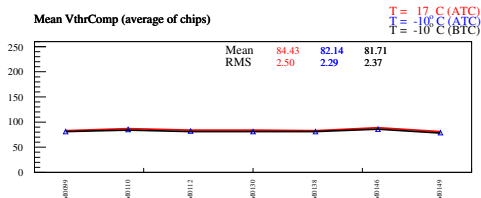
Operational parameters I

Mean DACs I



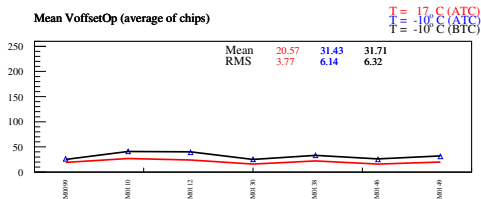
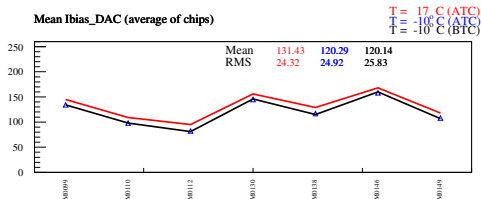
Operational parameters II

Mean DACs II



Operational parameters III

Mean DACs III

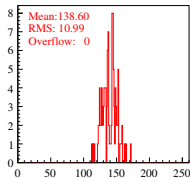


Operational parameters at $T = +17^{\circ}\text{C}$ (ATC)

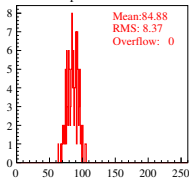
DAC distribution (of chips)

DACs at $T = 17^{\circ}\text{C}$ (ATC)

Vana

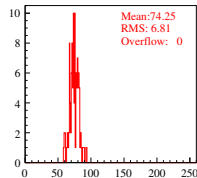


VthrComp

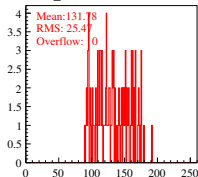


Modules: M0099 ... M0149

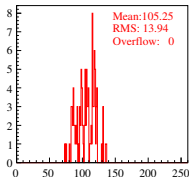
CalDel



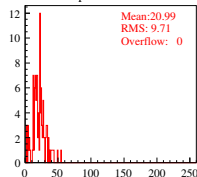
Ibias_DAC



Vtrim

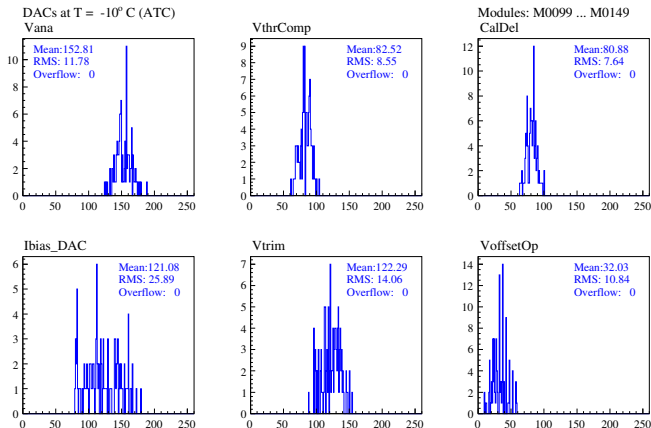


VoffsetOp



Operational parameters at $T = -10^{\circ}\text{C}$ (ATC)

DAC distribution (of chips)

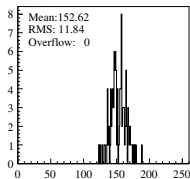


Operational parameters at $T = +17^{\circ}\text{C}$ (BTC)

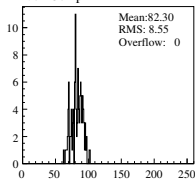
DAC distribution (of chips)

DACs at $T = -10^{\circ}\text{C}$ (BTC)

Vana

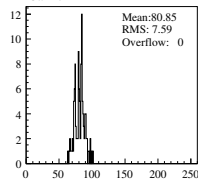


VthrComp

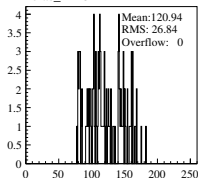


Modules: M0099 ... M0149

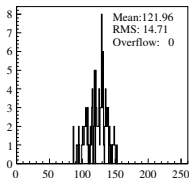
CalDel



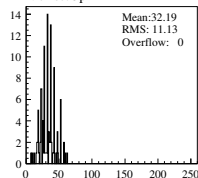
Ibias_DAC



Vtrim



VoffsetOp

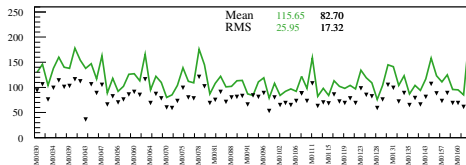


Operational parameters

Mean DACs I

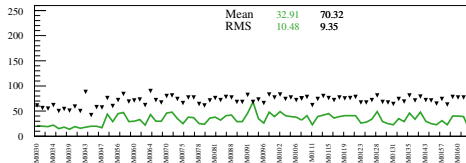
Mean Ibias_DAC (average of chips)

T = -10 C (ATC)
T = -10° C (ATC retest)



Mean VoffsetOp (average of chips)

T = -10 C (ATC)
T = -10° C (ATC retest)

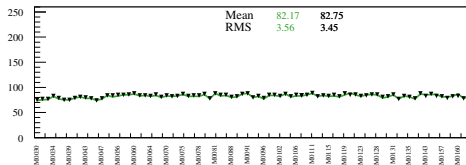


Operational parameters

Mean DACs II

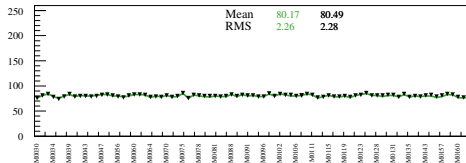
Mean VthrComp (average of chips)

T = -10° C (ATC)
T = -10° C (ATC retest)



Mean CalDel (average of chips)

T = -10° C (ATC)
T = -10° C (ATC retest)

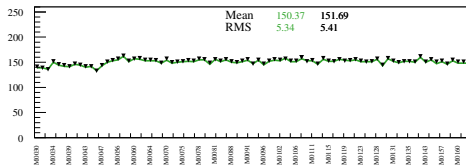


Operational parameters

Mean DACs III

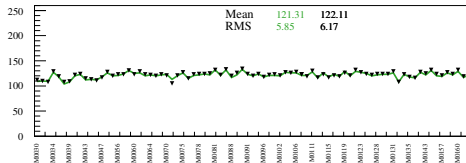
Mean Vana (average of chips)

T = -10° C (ATC)
T = -10° C (ATC retest)



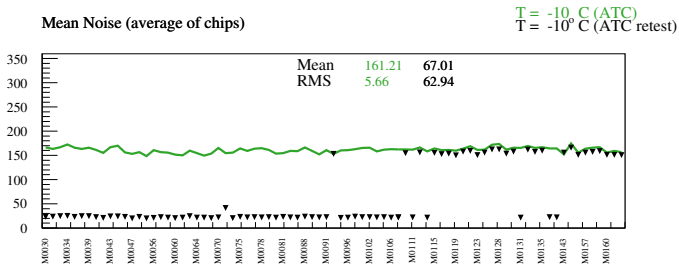
Mean Vtrim (average of chips)

T = -10° C (ATC)
T = -10° C (ATC retest)



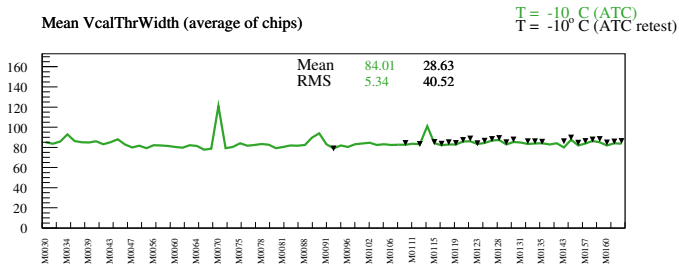
Performance parameters

Mean **Noise** [e^-] vs. Module Nr.



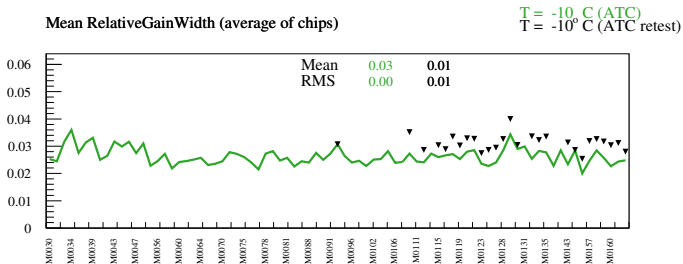
Performance parameters

Mean **VcalThresholdWidth** [e^-] vs. Module Nr.



Performance parameters

Mean **RelativeGainWidth** [%] vs. Module Nr.



Performance parameters

Mean PedestalSpread in $[e^-]$ vs. Module Nr.

