BPIX Module Testing Status - Week 30

10th January 2007

Production overview

Production Status: 115 modules produced (112 / 3)

- 72/12 graded as A/B $\rightarrow$ 73%
- 31 graded as C $\rightarrow$ 27%

Module Testing Report of Week 30:

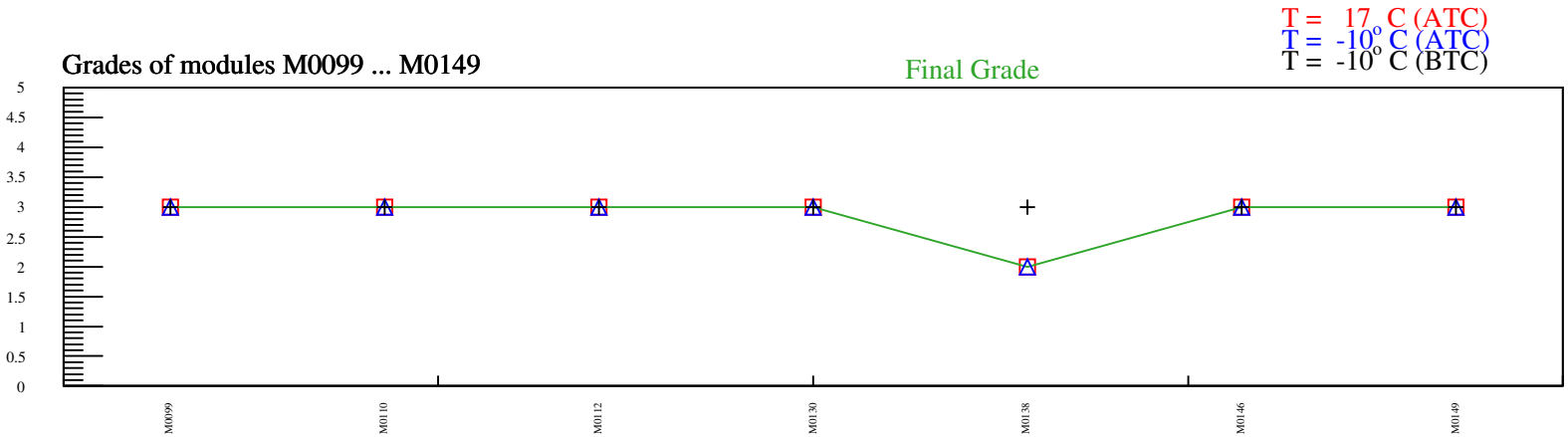
- 7/$-$ modules fully tested and therm. cycled (4 retested)

	Modules			*Half-Modules*		
Grade	**A**	**B**	**C**	**A**	**B**	**C**
T = -10^o C, BTC*	7	0	0	–	–	–
T = -10^o C, ATC	6	1	0	–	–	–
T = $+17^o$ C, ATC	6	1	0	–	–	–
Final Grade	6	1	0	–	–	–

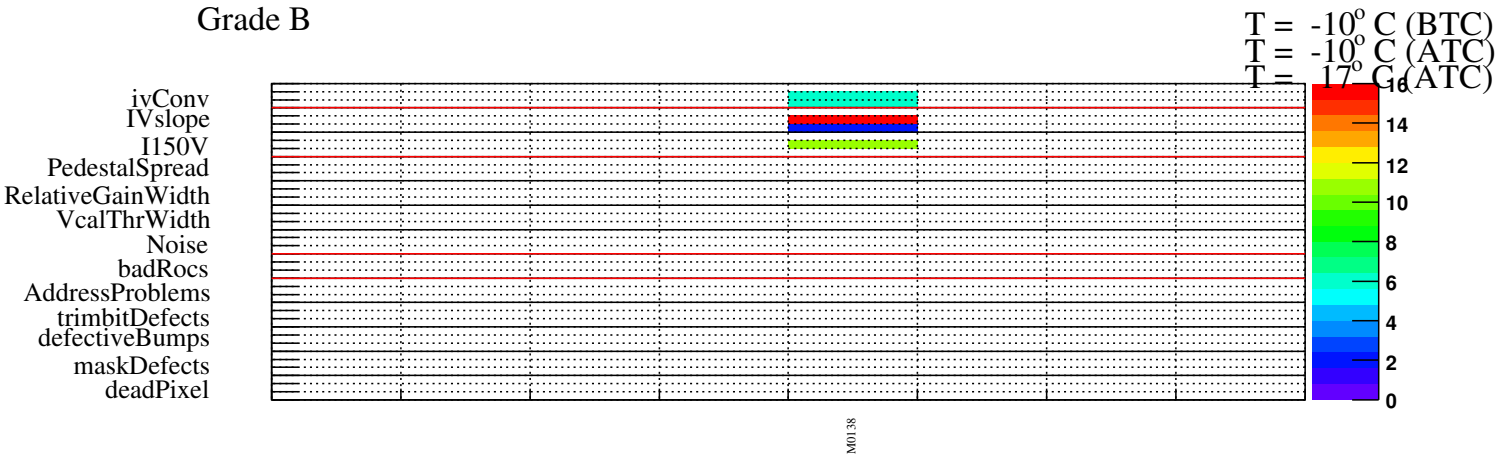
- no retests with new DAC settings

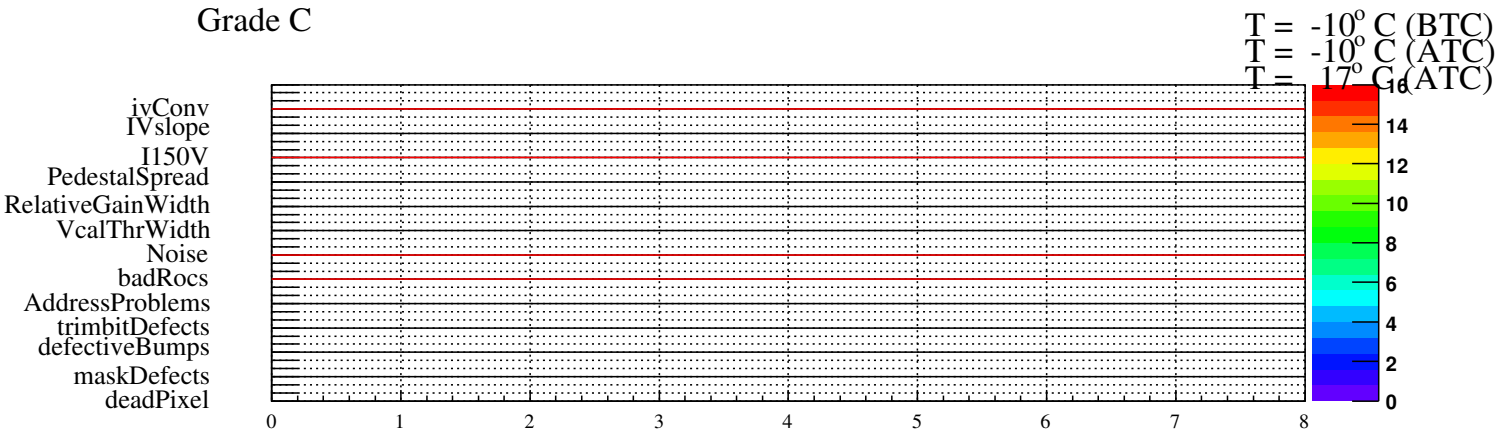
*without IV-criteria

Production summary



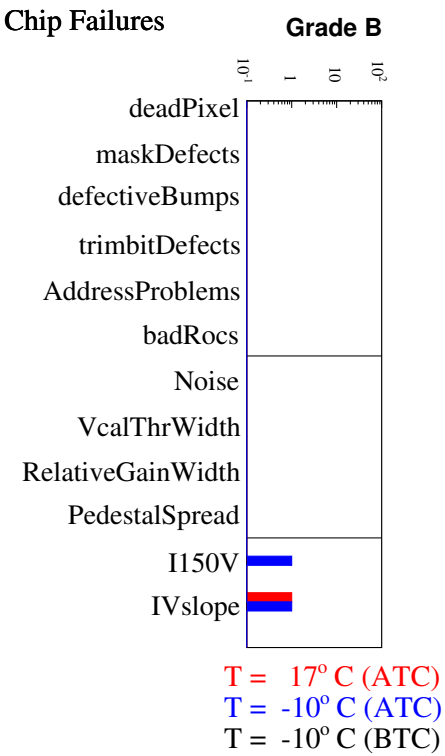
Module Failures Overview



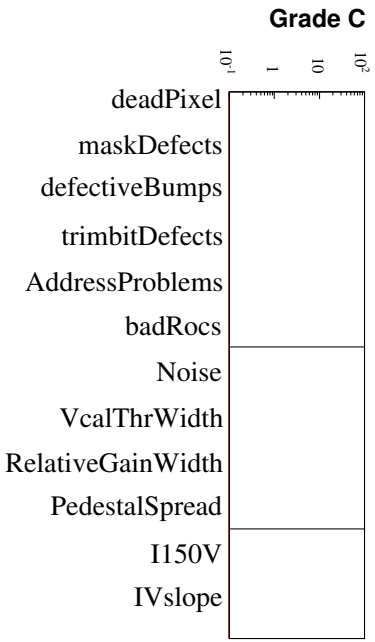


Production quality

Grade B



Grade C Failures



← Pixel defects

← Chip performance

← Module IV

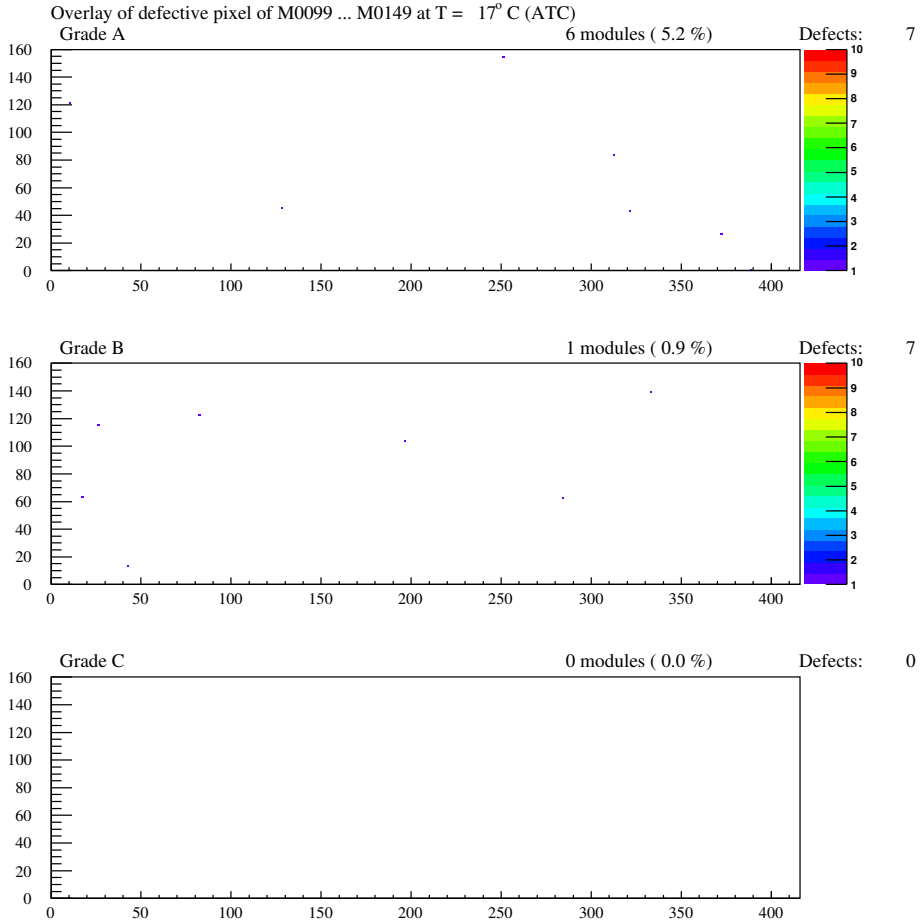
Defective pixel $T = 17^oC$ (ATC)

Overlay of all fully tested modules at T = $+17^o$ C (ATC)

Grade A
(6 modules)

Grade B
(1 modules)

Grade C
(0 modules)



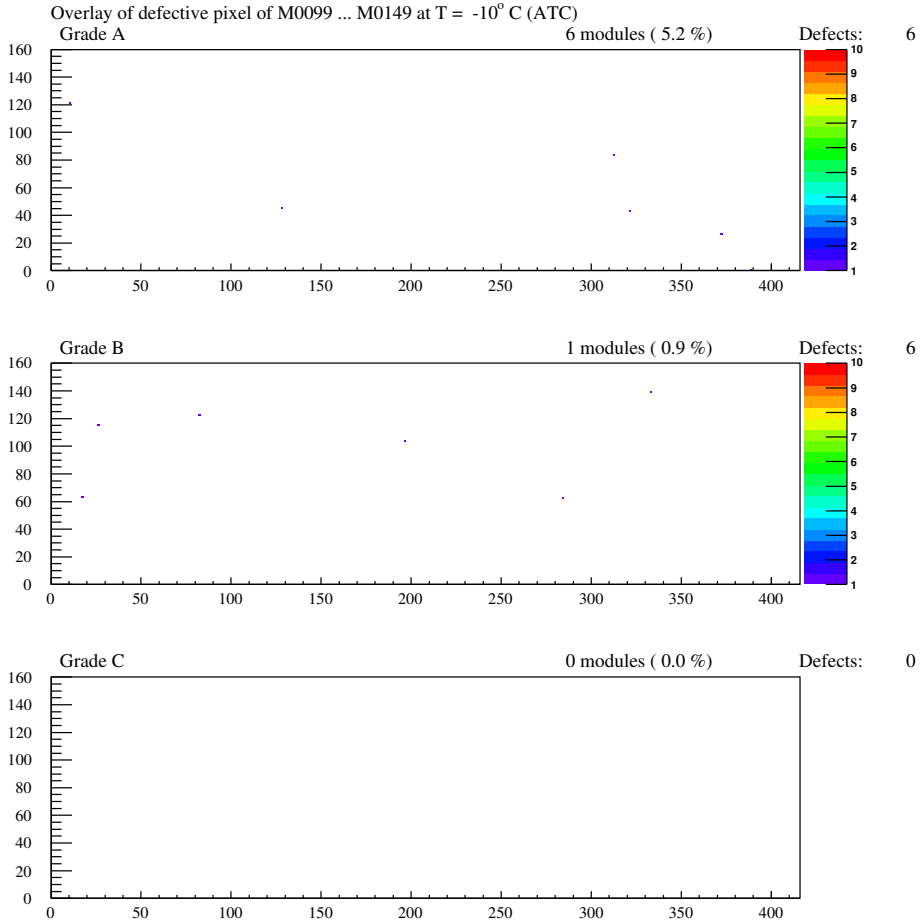
Defective pixel $T = -10^{o}C$ (ATC)

Overlay of all fully tested modules at T = -10^{o} C (ATC)

Grade A
(6 modules)

Grade B
(1 modules)

Grade C
(0 modules)



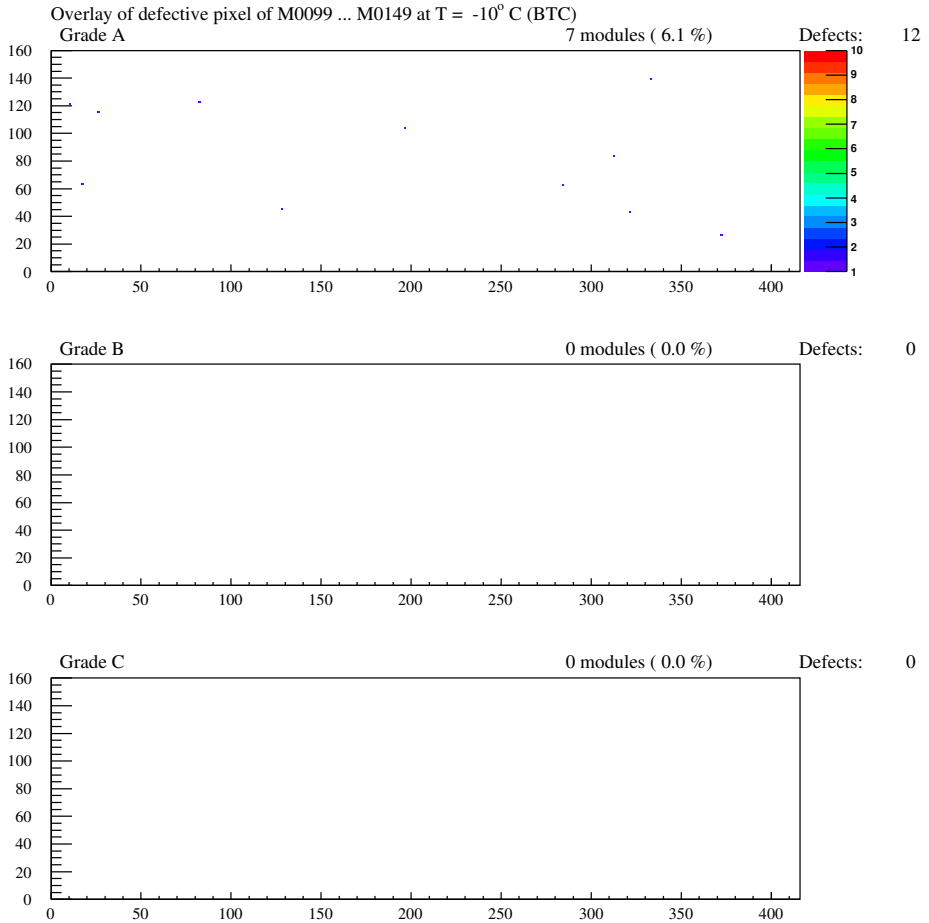
Defective pixel $T = -10^{o}C$ (BTC)

Overlay of all fully tested modules at T = -10^{o} C (BTC)

Grade A
(7 modules)

Grade B
(0 modules)

Grade C
(0 modules)



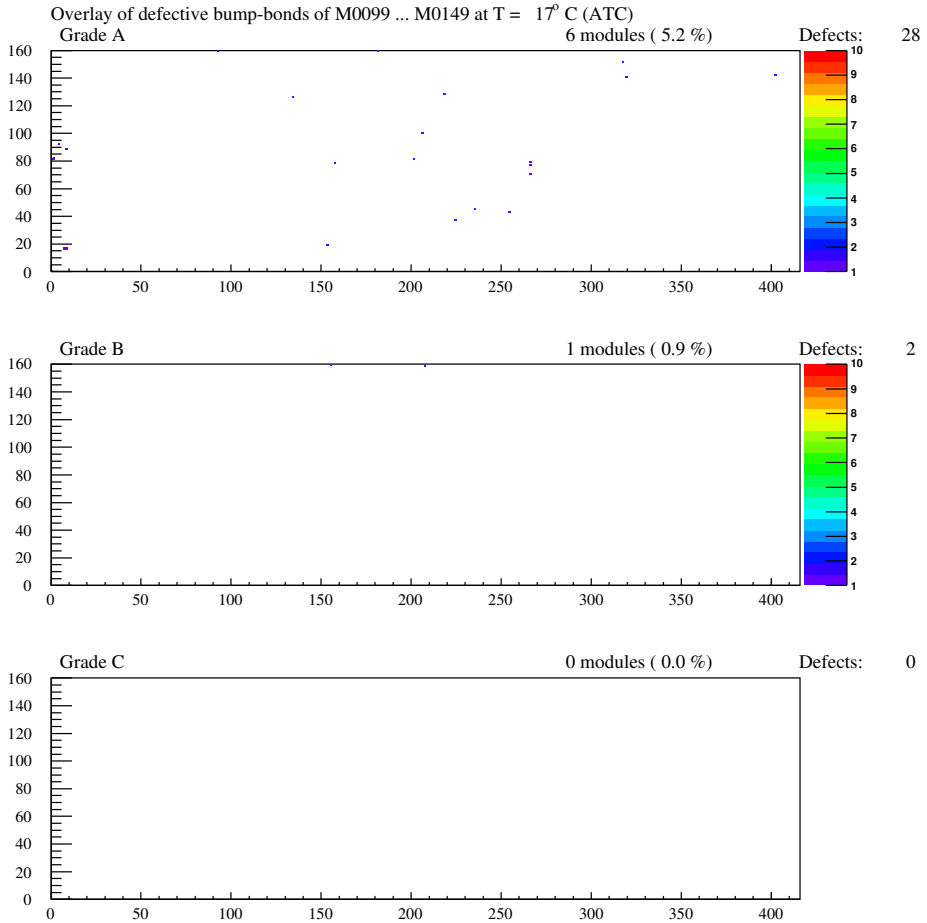
Defective bump-bonds $T = 17^{o}C$ (ATC)

Overlay of all fully tested modules at T = $+17^{o}$ C (ATC)

Grade A
(6 modules)

Grade B
(1 modules)

Grade C
(0 modules)



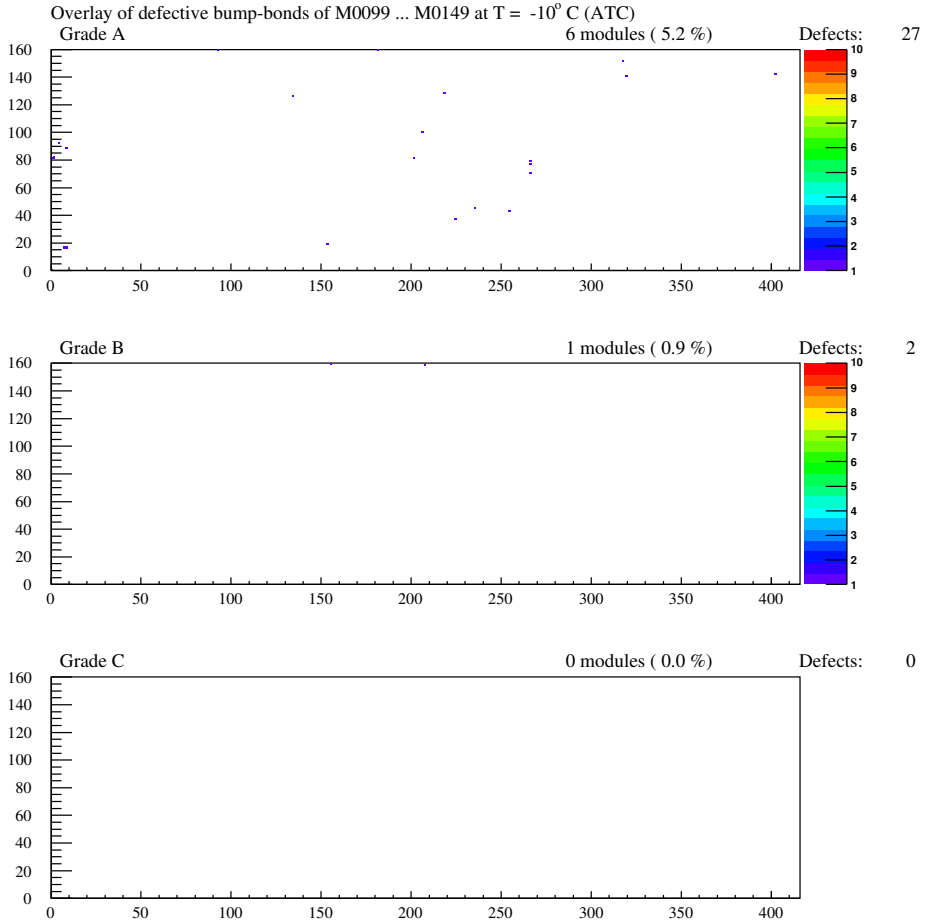
Defective bump-bonds $T = -10^{o}C$ (ATC)

Overlay of all fully tested modules at T = -10^{o} C (ATC)

Grade A
(6 modules)

Grade B
(1 modules)

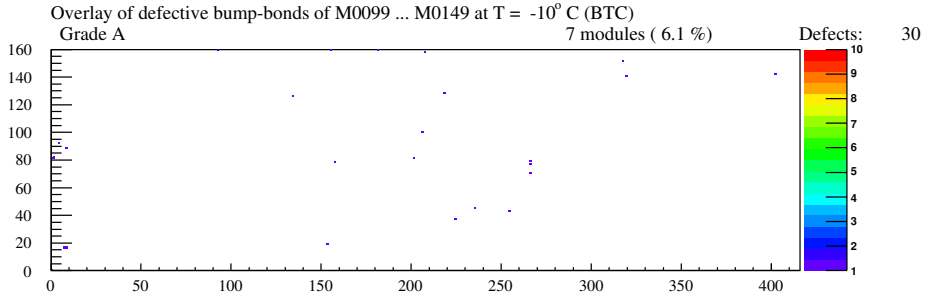
Grade C
(0 modules)



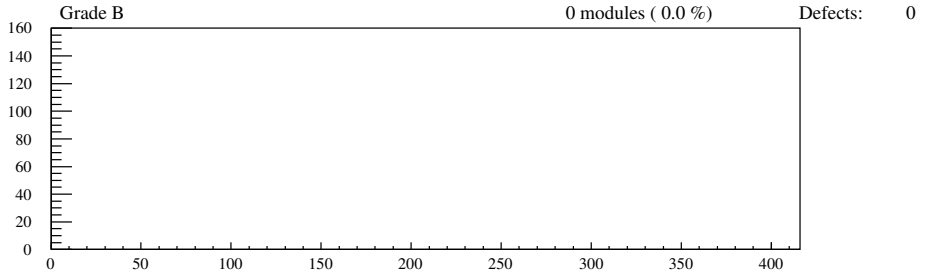
Defective bump-bonds $T = -10^{o}C$ (BTC)

Overlay of all fully tested modules at T = -10^{o} C (BTC)

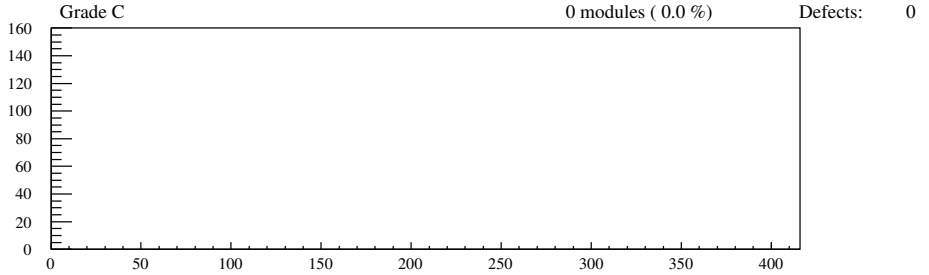
Grade A
(7 modules)



Grade B
(0 modules)

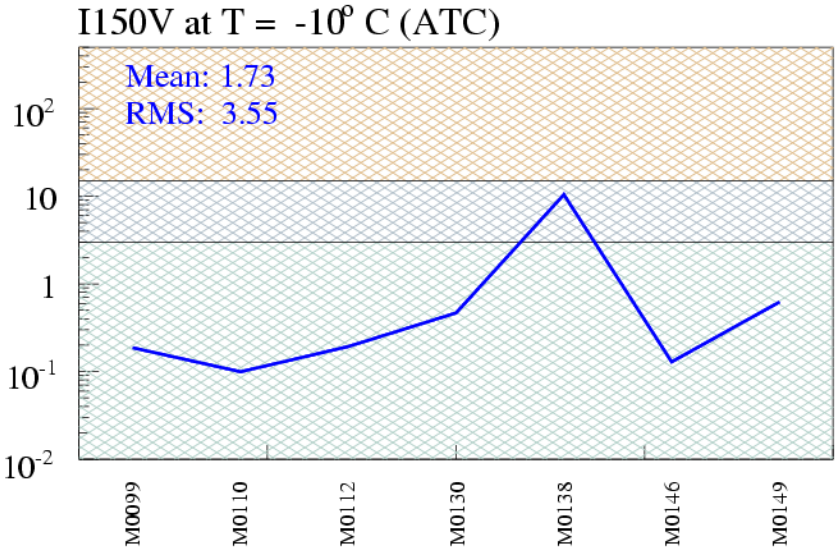


Grade C
(0 modules)

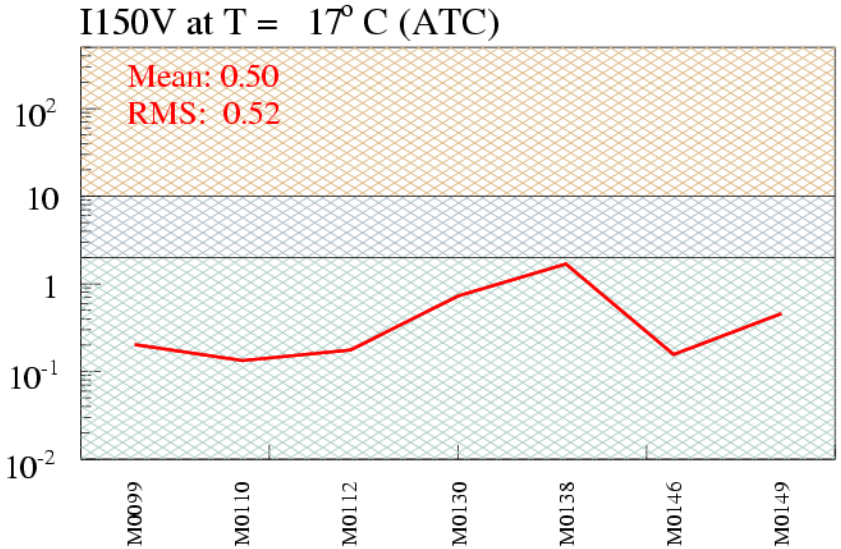


Current at 150 V

Current at 150 V (in μA) at $T = 17^oC$ and $T = -10^oC$



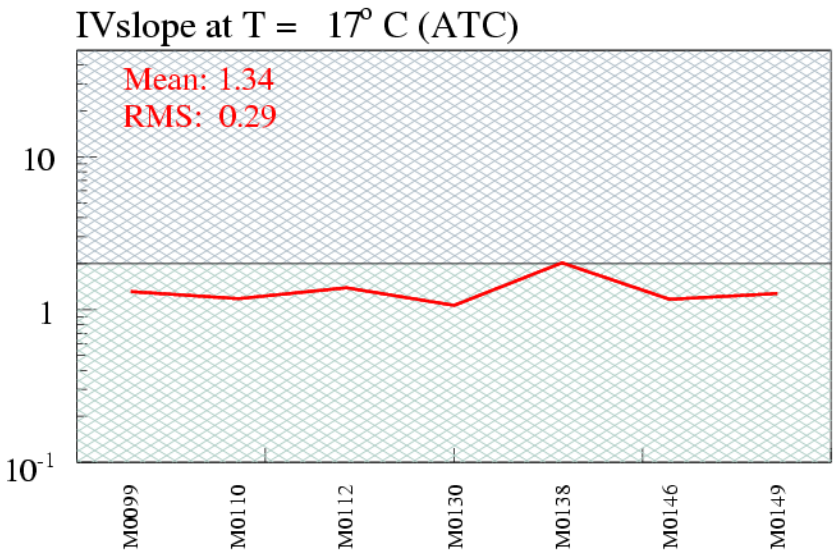
recalculated

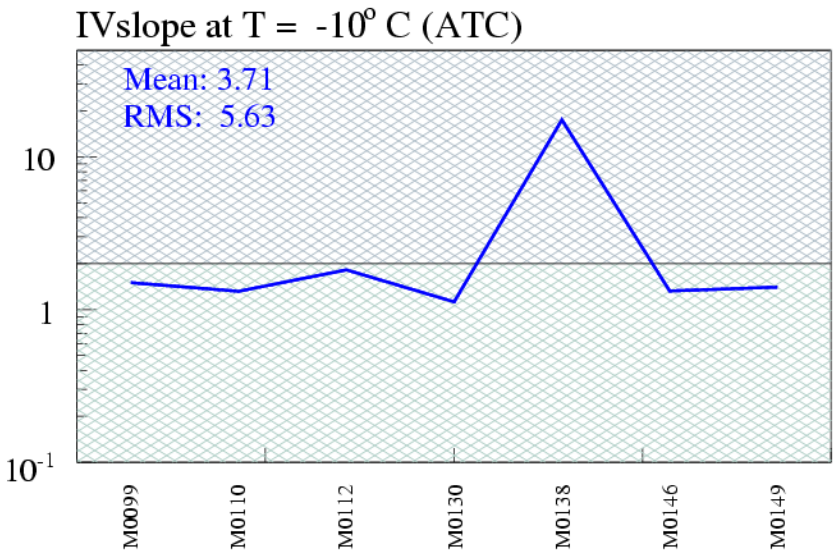


measured

Slope of IV-Curve

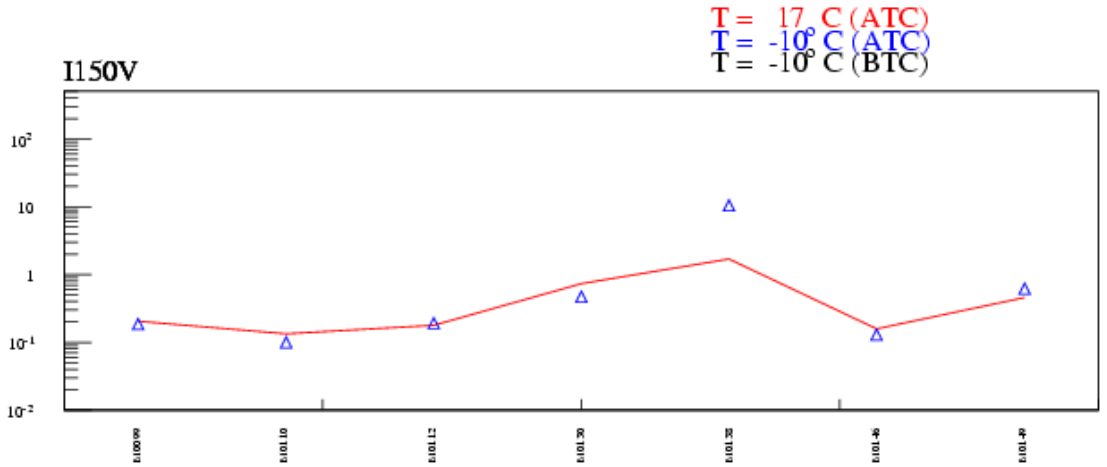
Slope of IV-Curveat $T = 17^oC$ and $T = -10^oC$

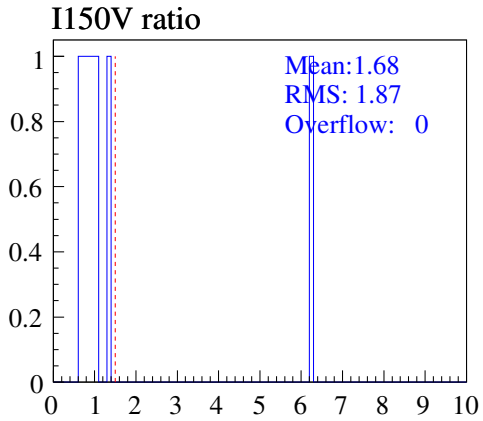


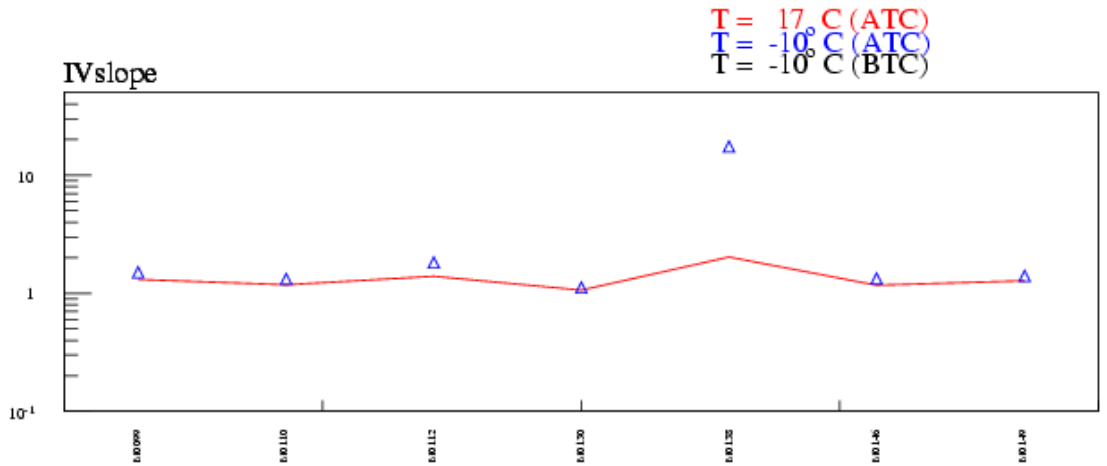


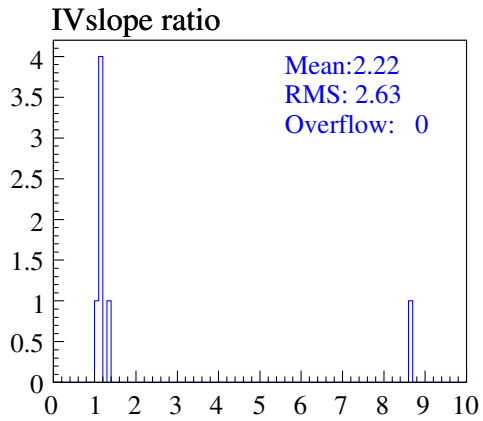
Current recalculation to $T = 17^oC$

Cross check of recalculated values with measured values

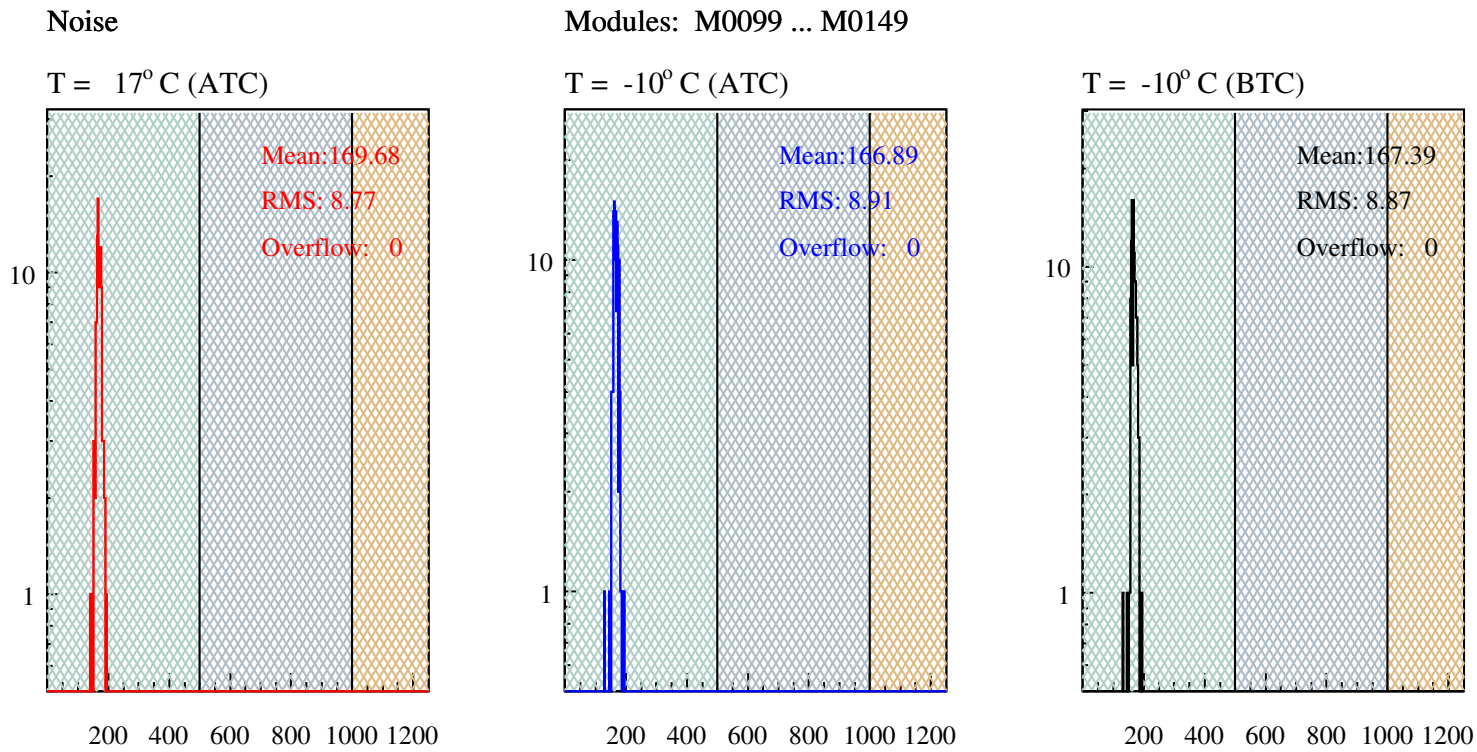








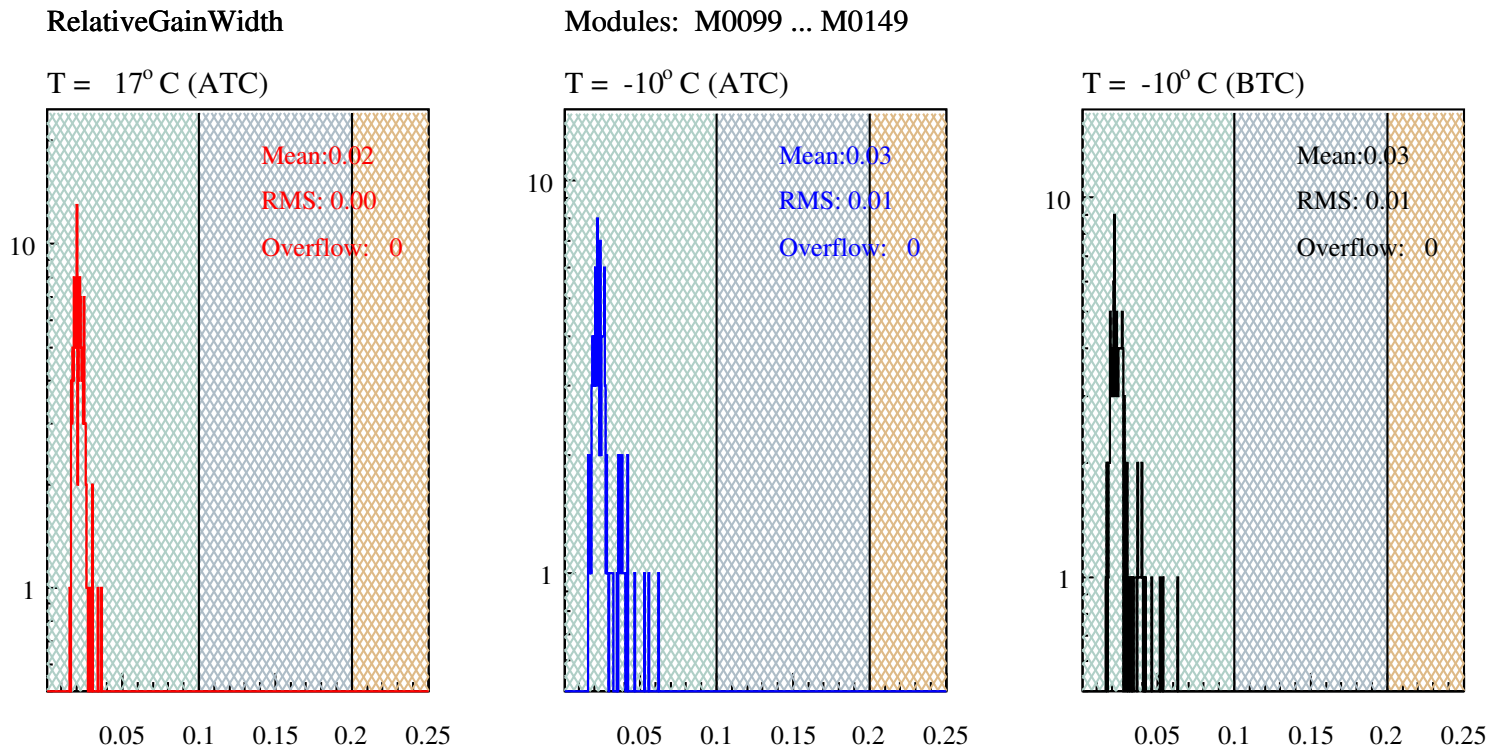
MeanNoise of chips



Noise in e^-

Relative Gain Width

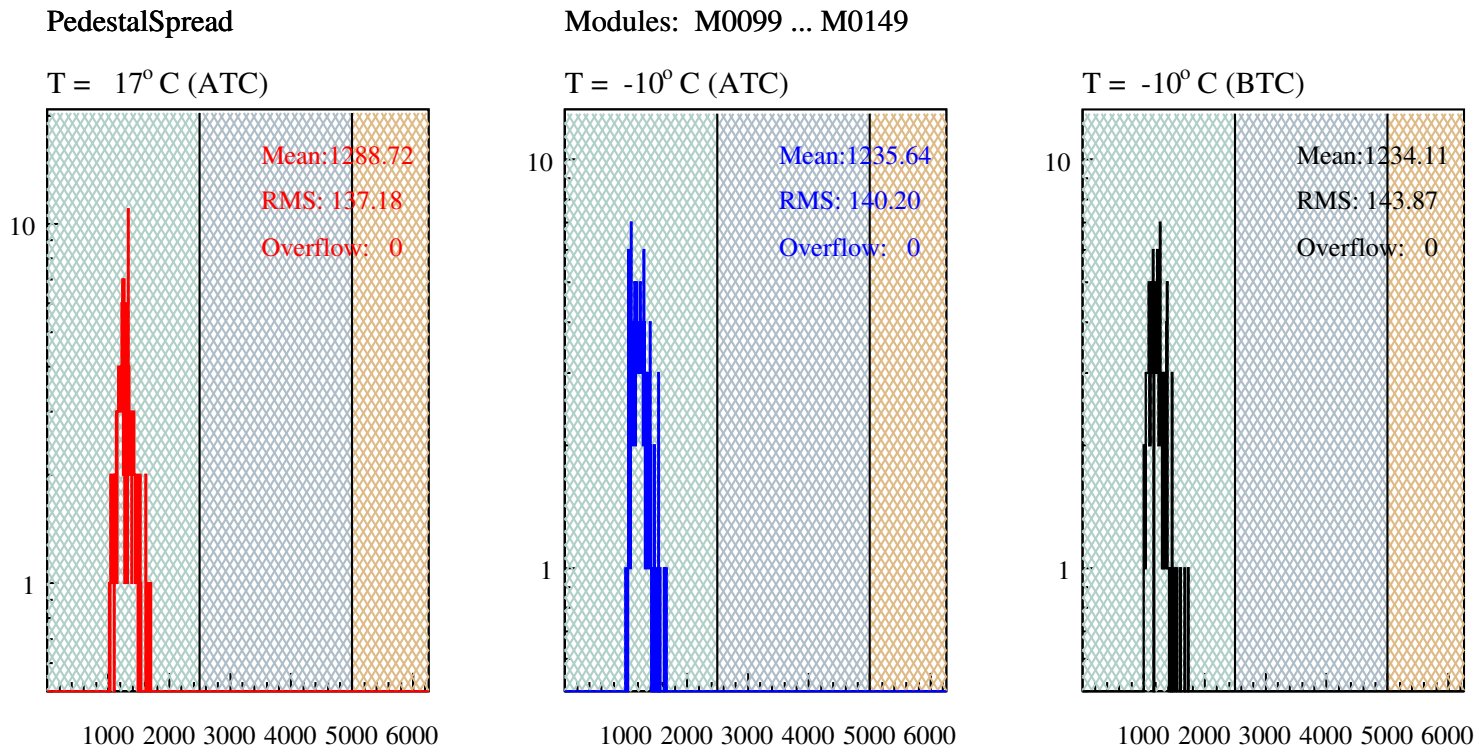
RelativeGainWidth of chips



Rel. Gain Width in %

Pedestal Spread

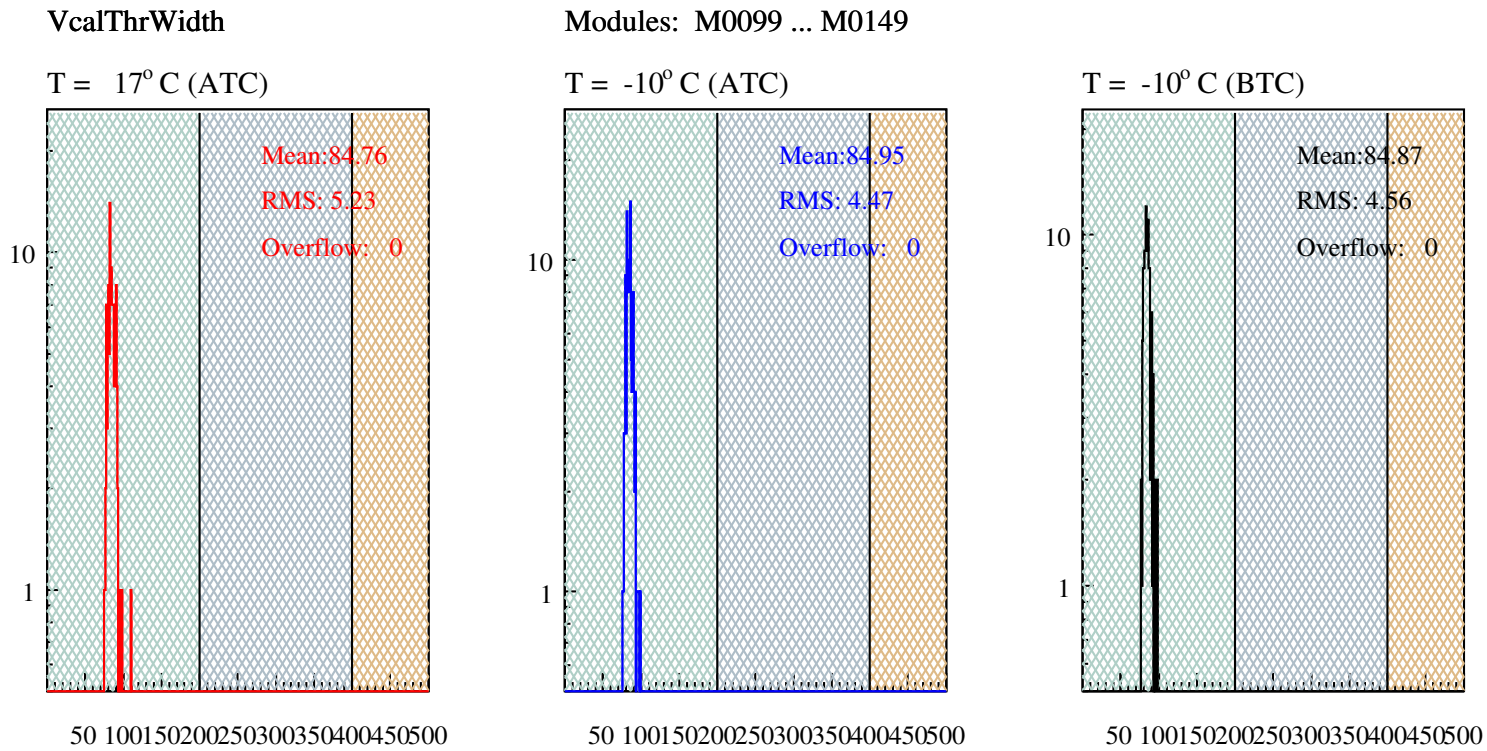
PedestalSpread of chips



Pedestal Spread in e^-

Vcal Threshold Width

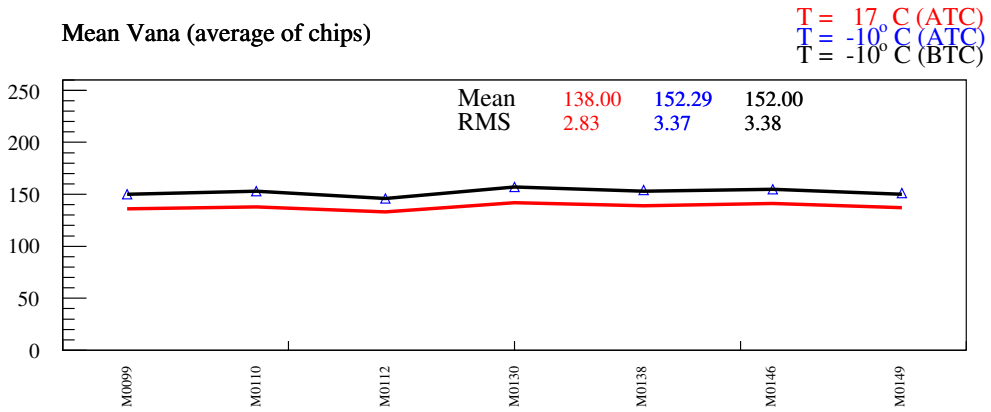
VcalThresholdWidth of chips

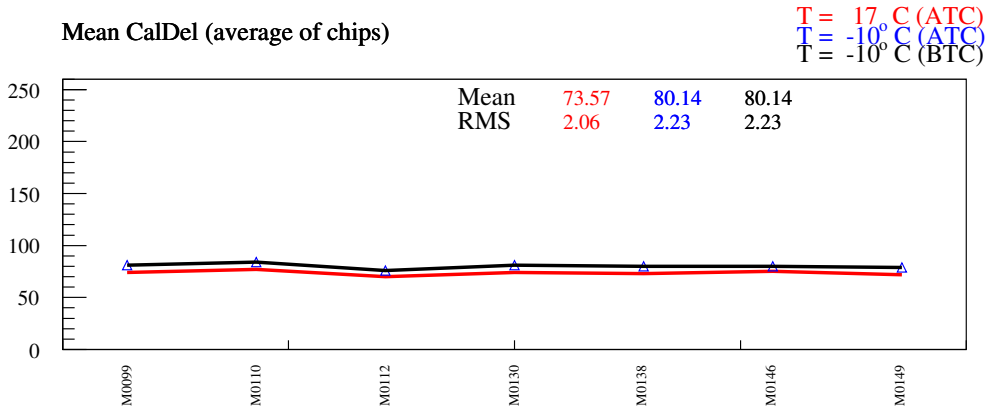


Vcal Thr. Width in e^-

Operational parameters I

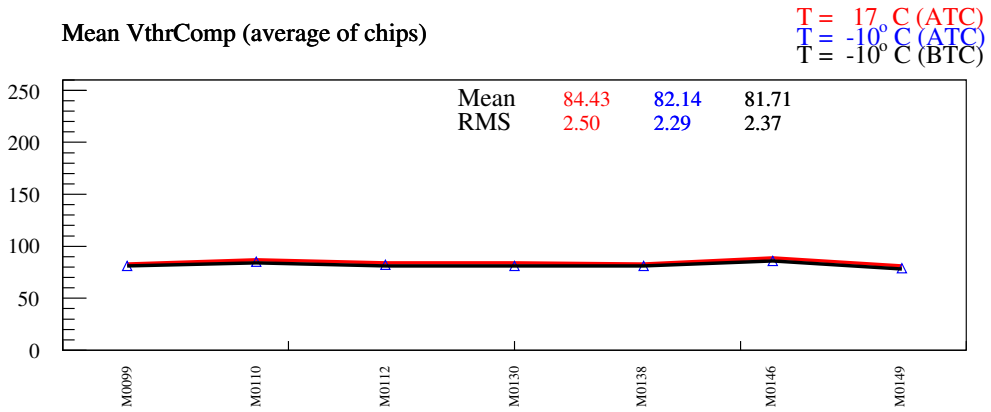
Mean DACs I

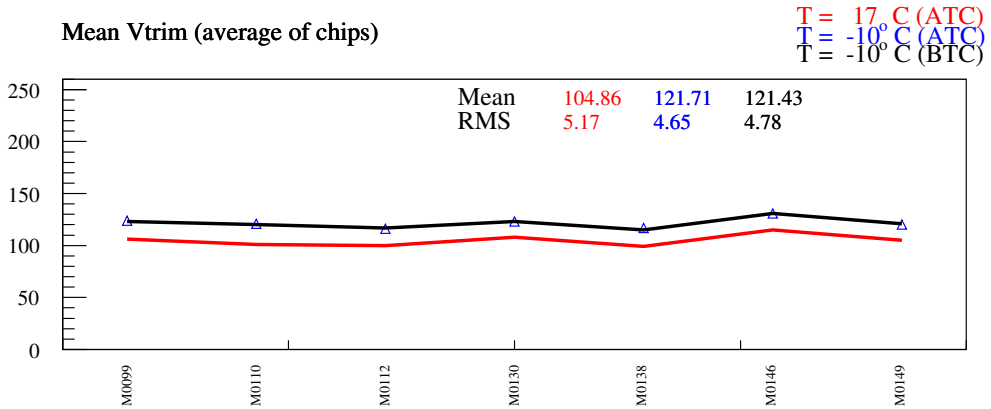




Operational parameters II

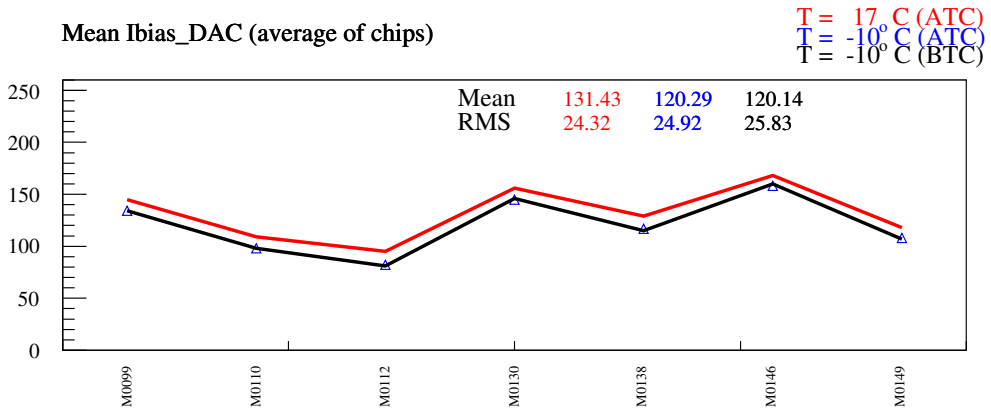
Mean DACs II

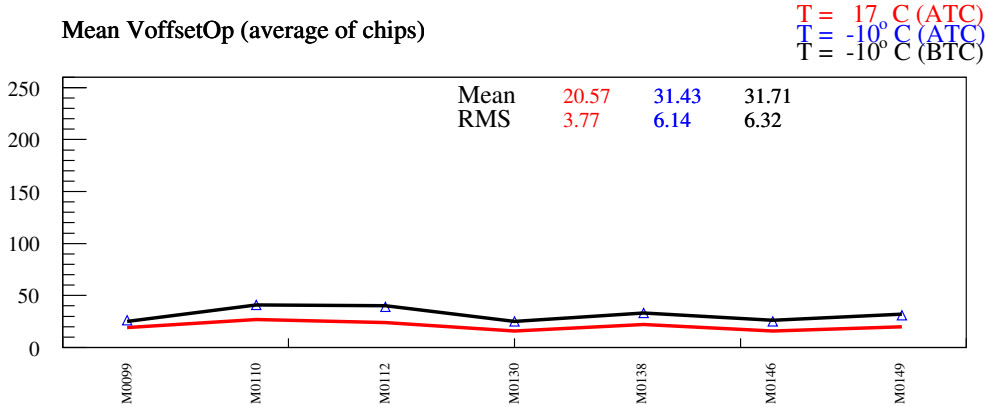




Operational parameters III

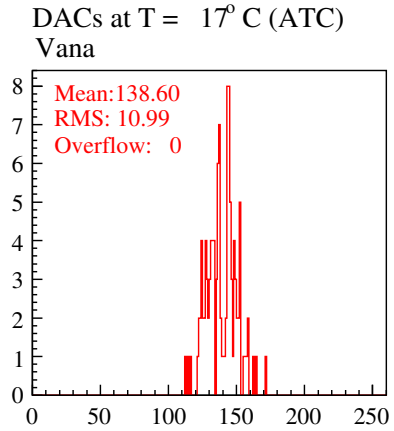
Mean DACs III

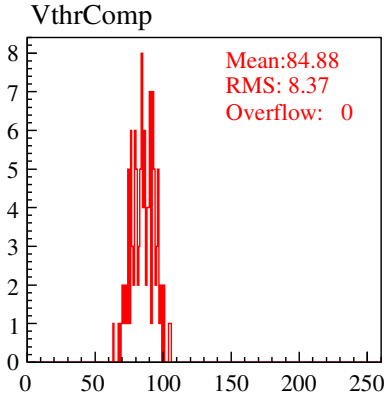


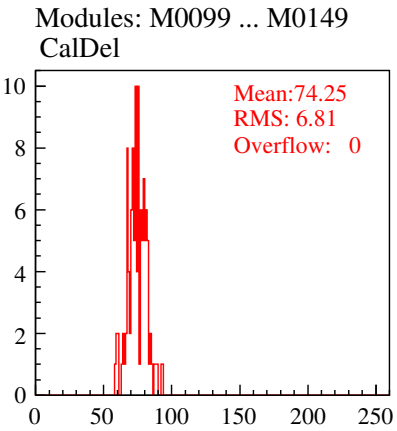


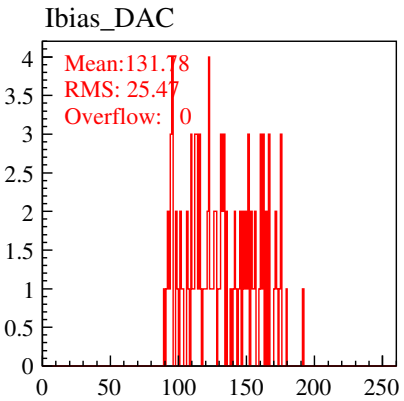
Operational parameters at $T = +17^{o}C$ (ATC)

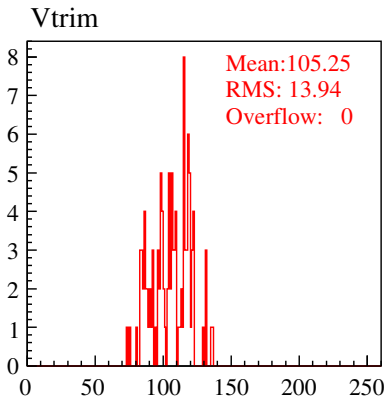
DAC distribution (of chips)

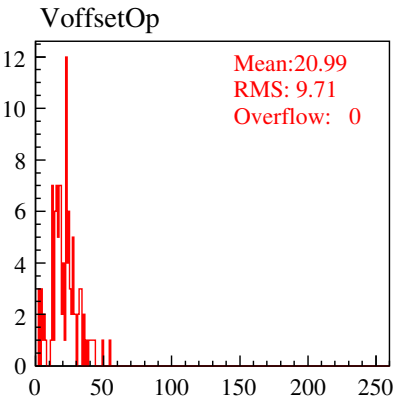






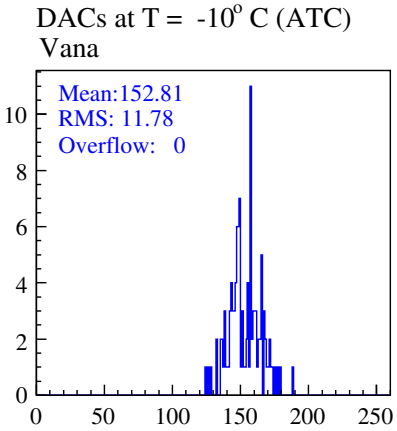


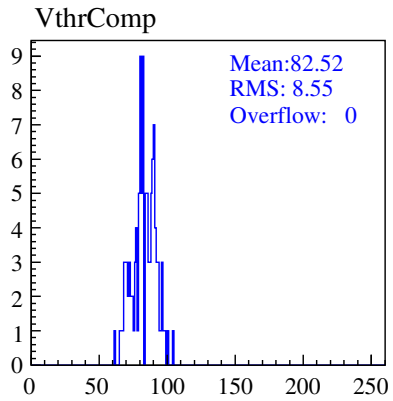


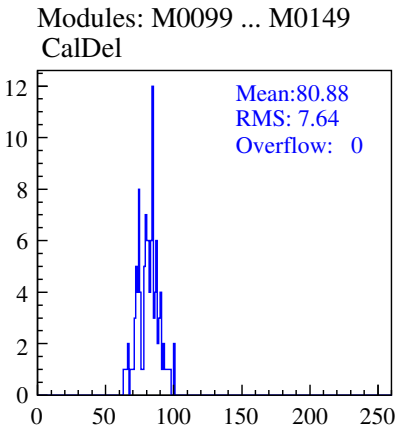


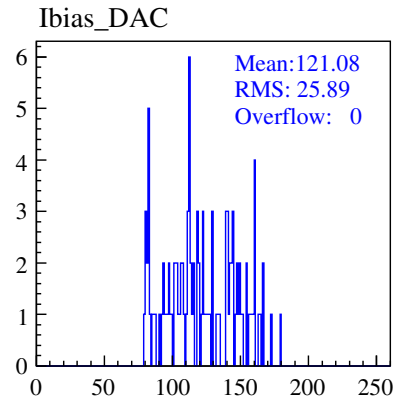
Operational parameters at $T = -10^{o}C$ (ATC)

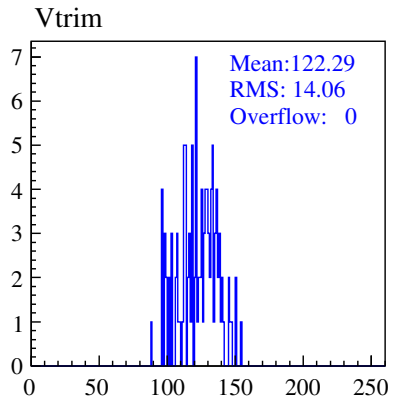
DAC distribution (of chips)

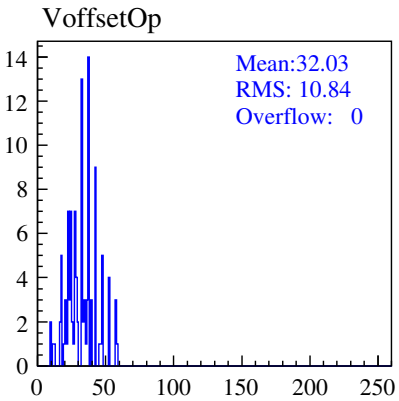






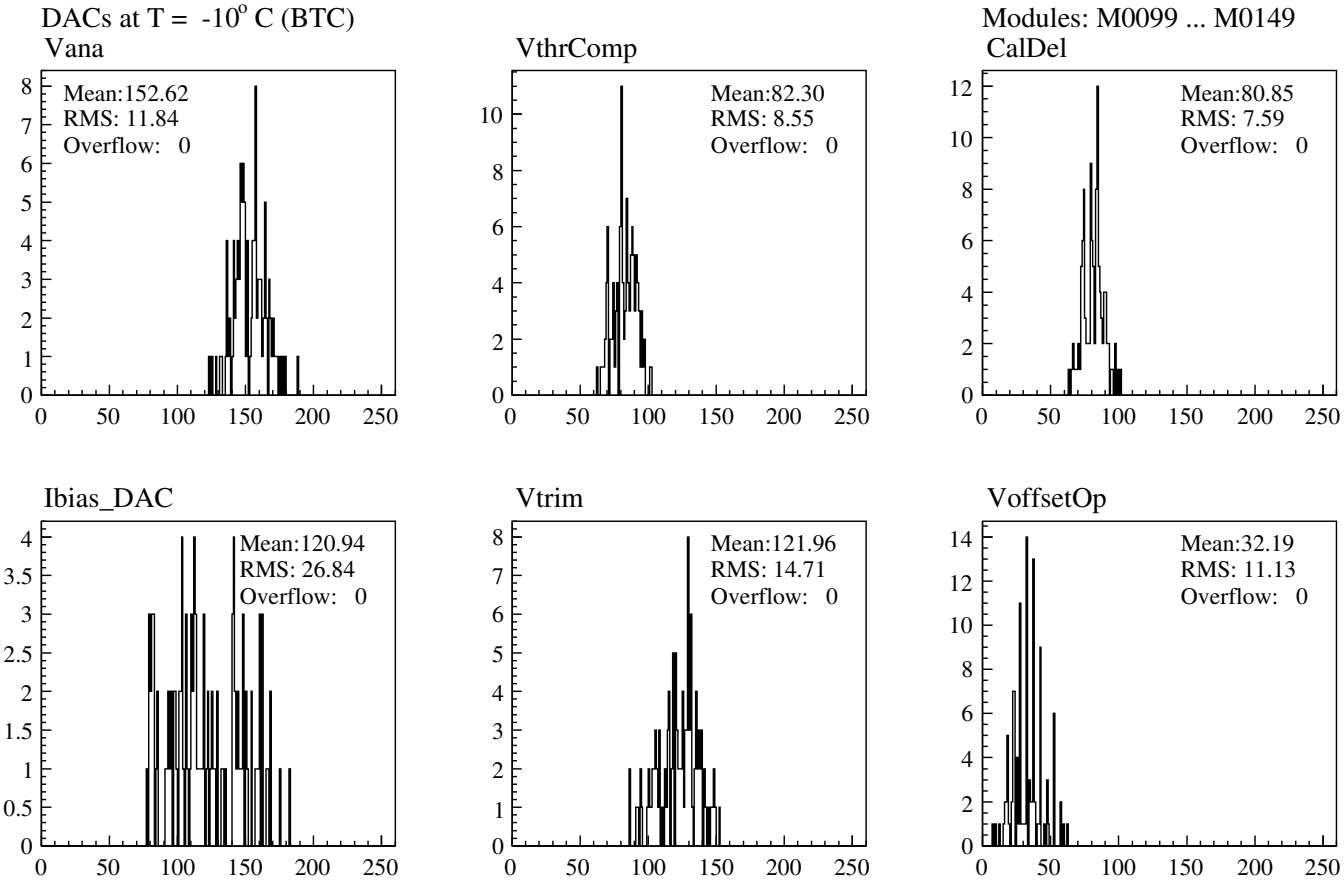






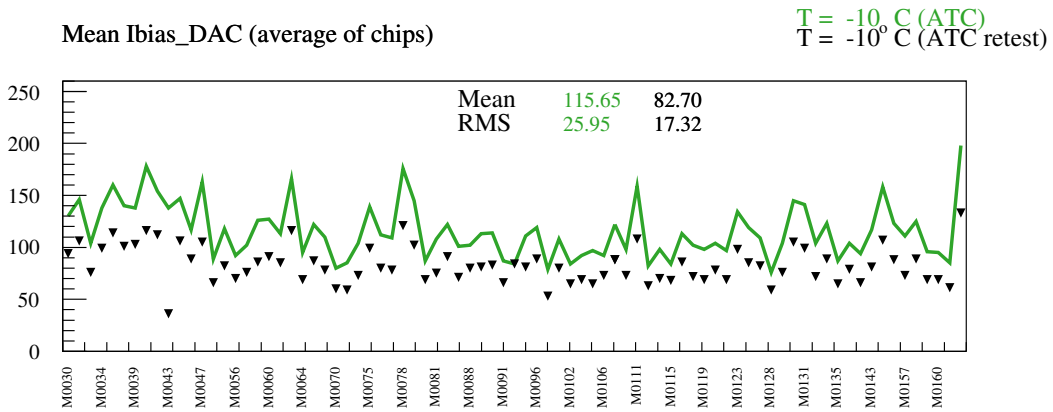
Operational parameters at $T = +17^{o}C$ (BTC)

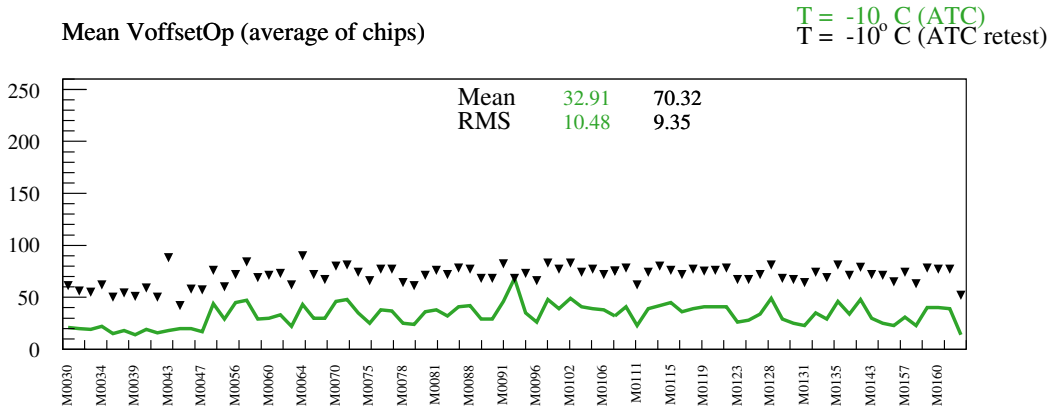
DAC distribution (of chips)



Operational parameters

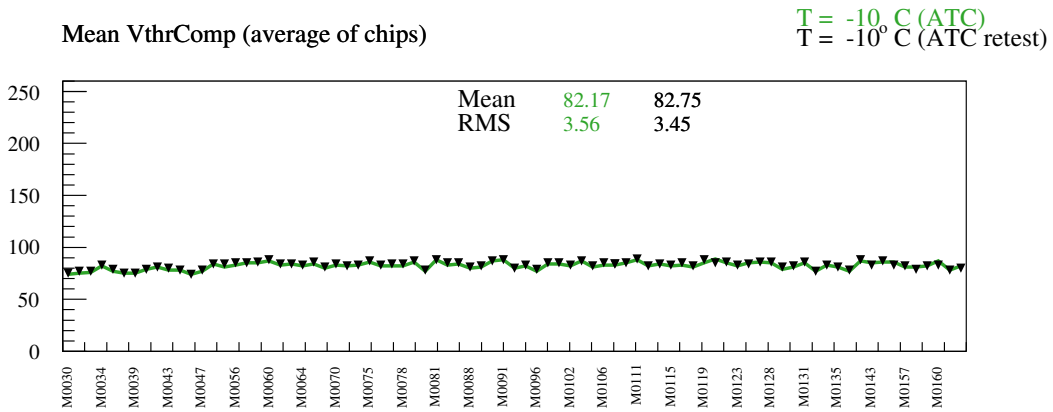
Mean DACs I

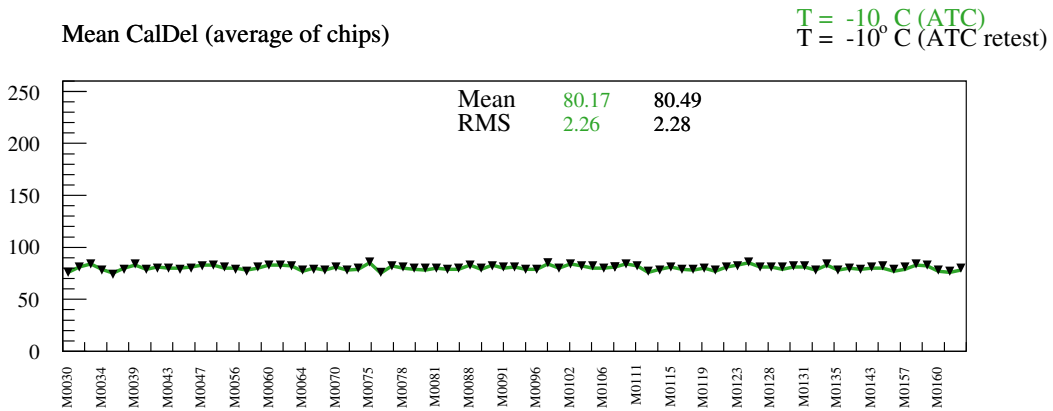




Operational parameters

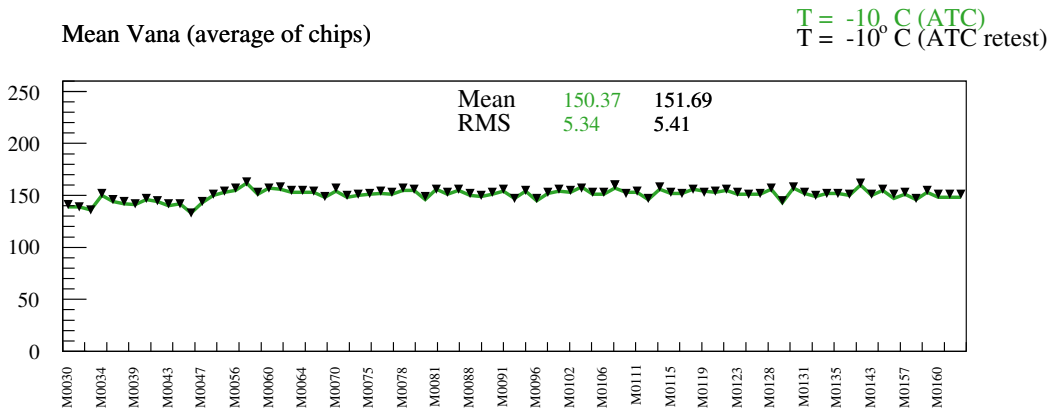
Mean DACs II

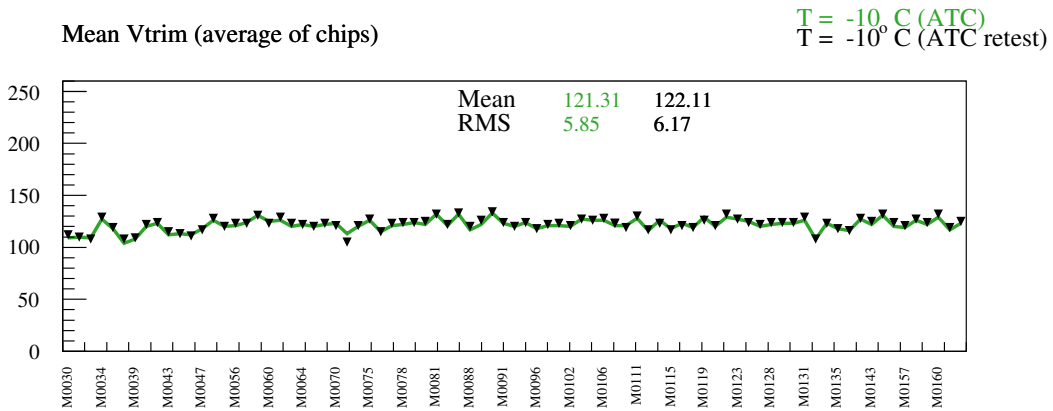




Operational parameters

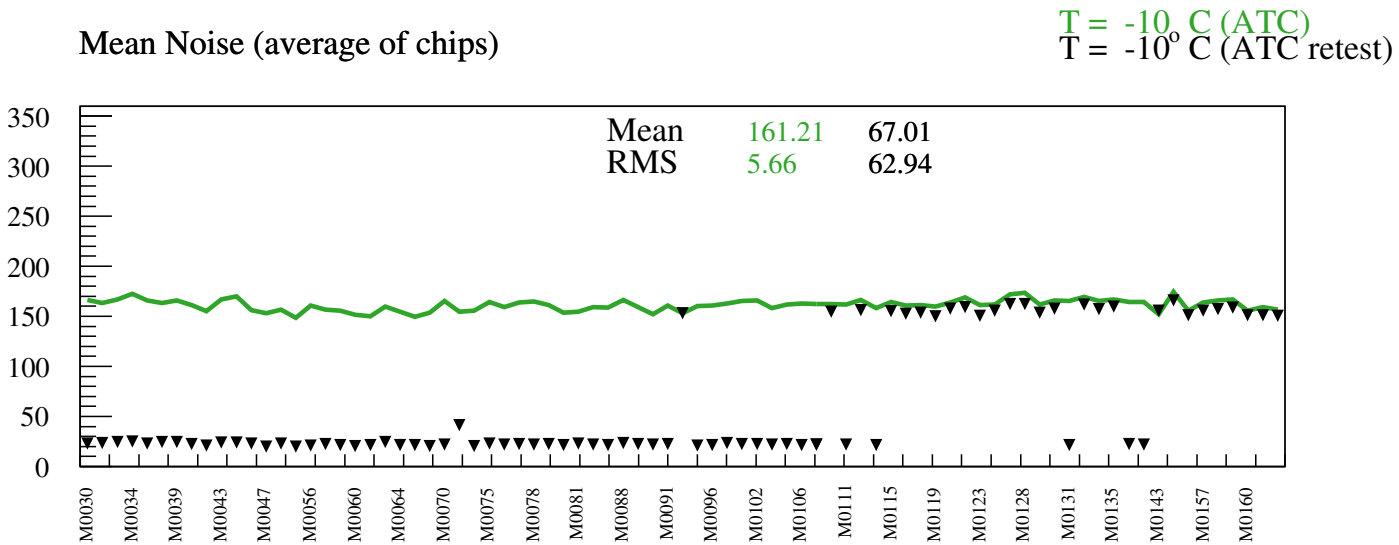
Mean DACs III





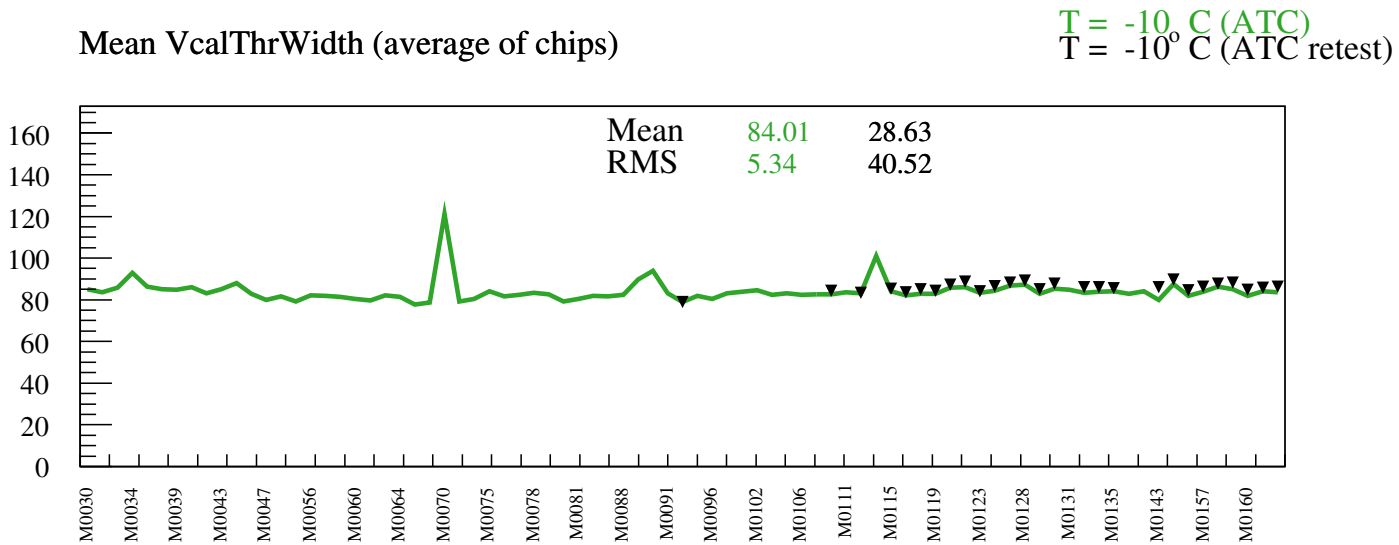
Performance parameters

Mean **Noise** [e^-] vs. Module Nr.



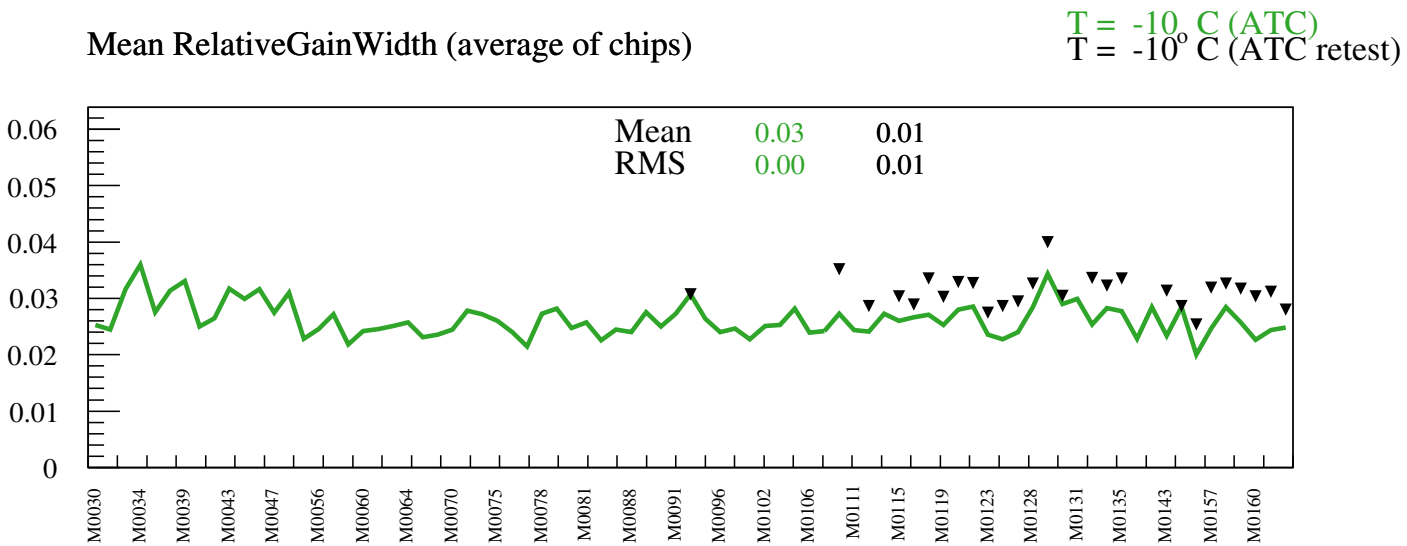
Performance parameters

Mean **VcalThresholdWidth** [e^-] vs. Module Nr.



Performance parameters

Mean **RelativeGainWidth** [%] vs. Module Nr.



Performance parameters

Mean **PedestalSpread** in [e^-] vs. Module Nr.