

BPIX Module Testing Status - Week 3

22nd January 2007

Production overview

Production Status: 379 modules produced (355 / 24)

- 264/53 graded as A/B → 84%
- 62 graded as C → 16%

Module Testing Report of Week 3:

- 23/10 modules fully tested and therm. cycled (0 retested)

	Modules			Half-Modules		
Grade	A	B	C	A	B	C
T = -10° C, BTC*	22	1	0	9	1	0
T = -10° C, ATC	16	6	1	8	2	0
T = +17° C, ATC	21	2	0	8	2	0
Final Grade	16	6	1	8	1	1

- 10 were retested with new DAC settings (2 change)

- M0067: B -> C -> overall grades - M0145: A -> B -> overall grades

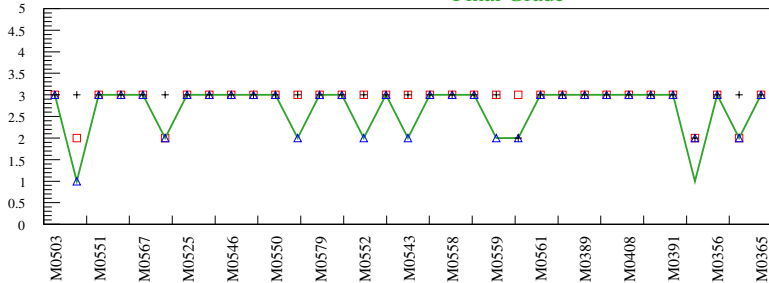
*without IV-criteria

Production summary

Grades of modules M0503 ... M0365

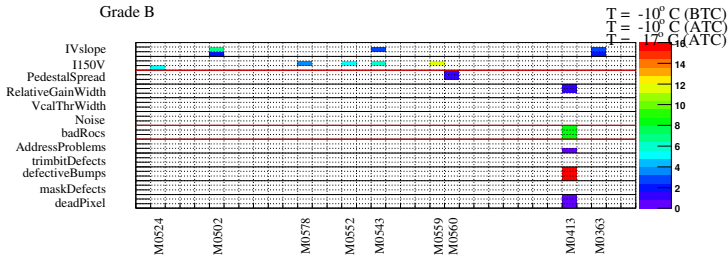
Final Grade

T = 17°C (ATC)
T = -10°C (ATC)
T = -10°C (BTC)

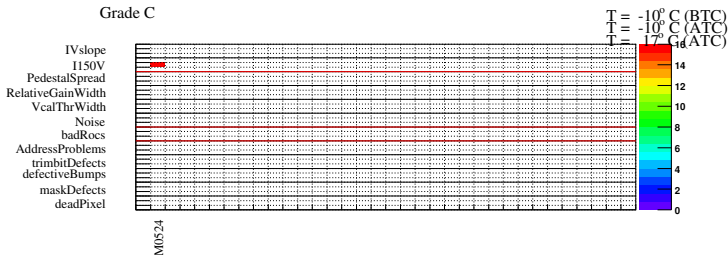


Module Failures Overview

Grade B



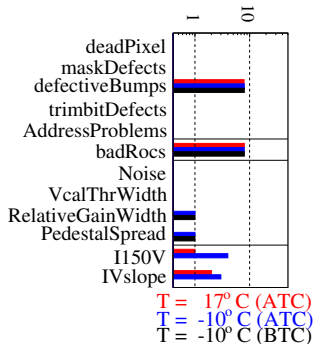
Grade C



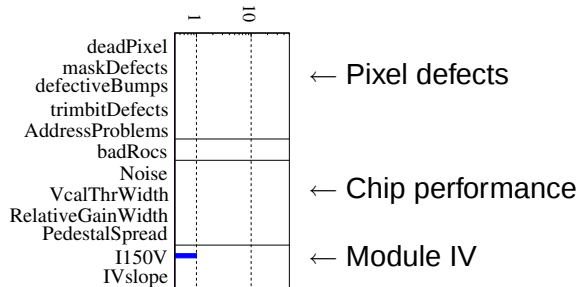
Production quality

Chip Failures

Grade B
Grade B



Grade C
Grade C



← Pixel defects

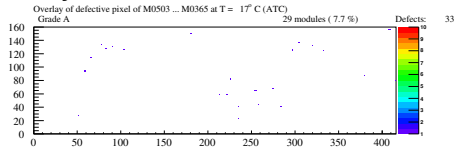
← Chip performance

← Module IV

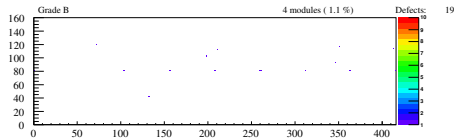
Defective pixel $T = 17^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = +17^{\circ}\text{C}$ (ATC)

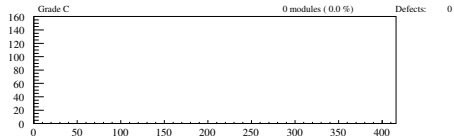
Grade A
(29 modules)



Grade B
(4 modules)



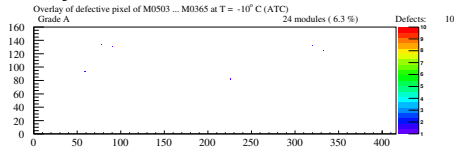
Grade C
(0 modules)



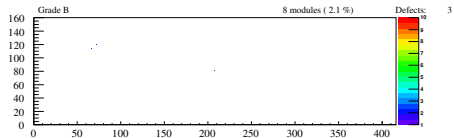
Defective pixel $T = -10^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (ATC)

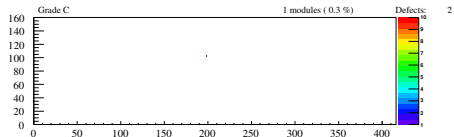
Grade A
(24 modules)



Grade B
(8 modules)



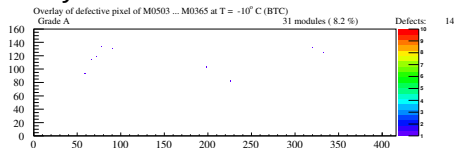
Grade C
(1 modules)



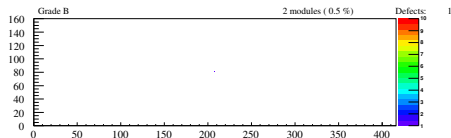
Defective pixel $T = -10^{\circ}\text{C}$ (BTC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (BTC)

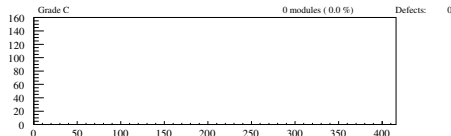
Grade A
(31 modules)



Grade B
(2 modules)



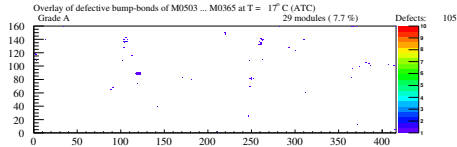
Grade C
(0 modules)



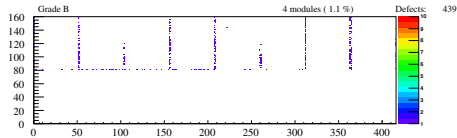
Defective bump-bonds $T = 17^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = +17^{\circ}\text{C}$ (ATC)

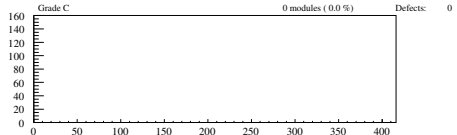
Grade A
(29 modules)



Grade B
(4 modules)



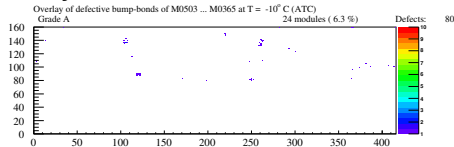
Grade C
(0 modules)



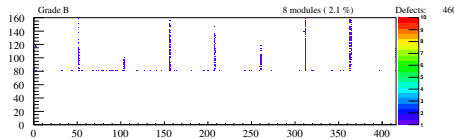
Defective bump-bonds $T = -10^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (ATC)

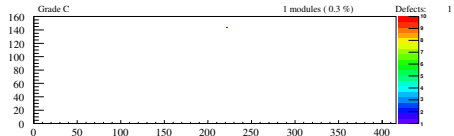
Grade A
(24 modules)



Grade B
(8 modules)



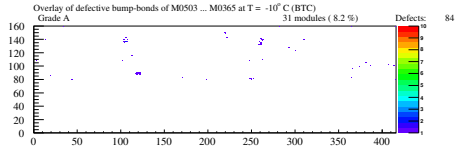
Grade C
(1 modules)



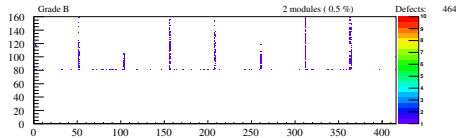
Defective bump-bonds $T = -10^{\circ}\text{C}$ (BTC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (BTC)

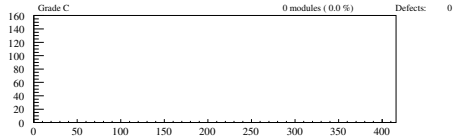
Grade A
(31 modules)



Grade B
(2 modules)

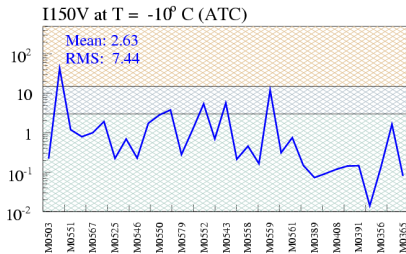


Grade C
(0 modules)

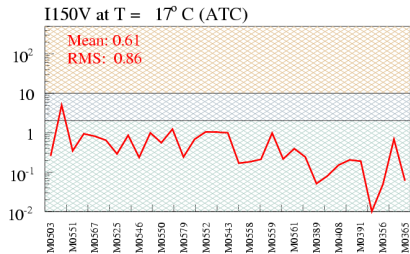


Current at 150 V

Current at 150 V (in μA) at $T = 17^\circ\text{C}$ and $T = -10^\circ\text{C}$



recalculated

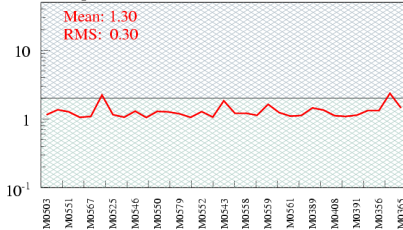


measured

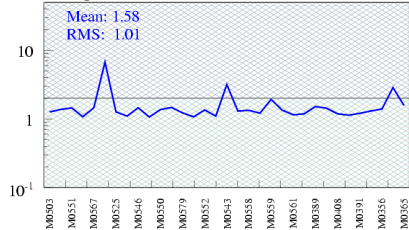
Slope of IV-Curve

Slope of IV-Curve at $T = 17^{\circ}\text{C}$ and $T = -10^{\circ}\text{C}$

IVslope at $T = 17^{\circ}\text{C}$ (ATC)

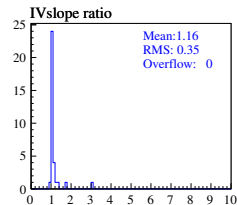
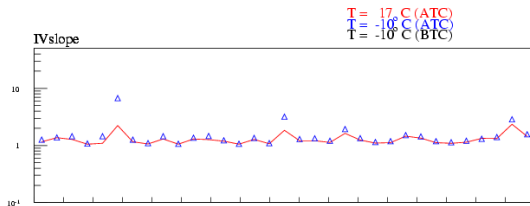
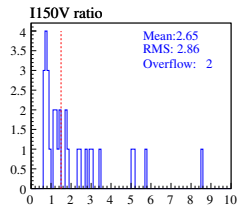
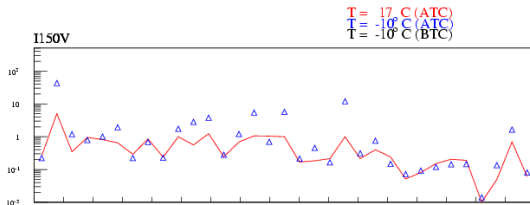


IVslope at $T = -10^{\circ}\text{C}$ (ATC)



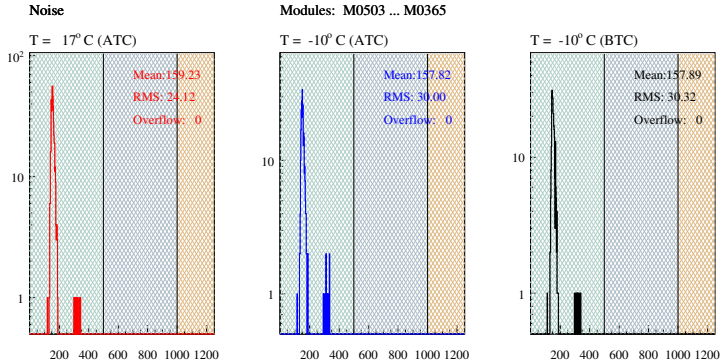
Current recalculation to $T = 17^{\circ}\text{C}$

Cross check of recalculated values with measured values



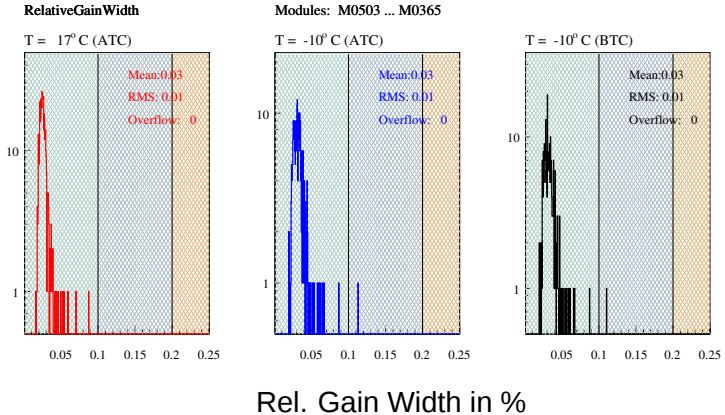
Noise

MeanNoise of chips



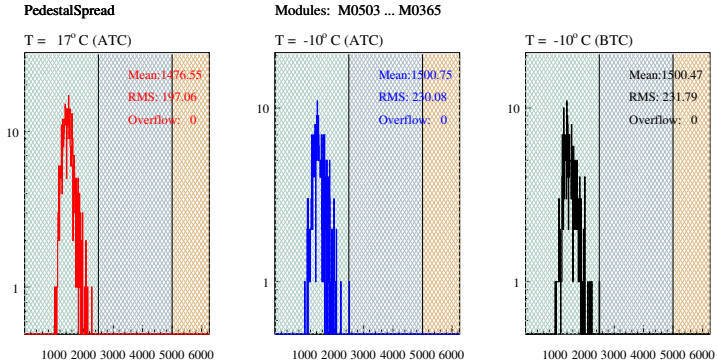
Relative Gain Width

RelativeGainWidth of chips



Pedestal Spread

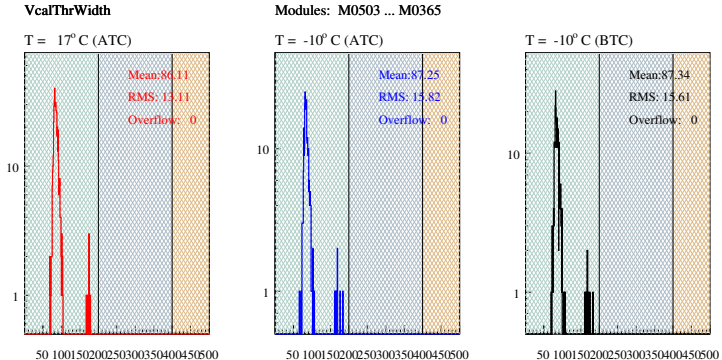
PedestalSpread of chips



Pedestal Spread in e^-

Vcal Threshold Width

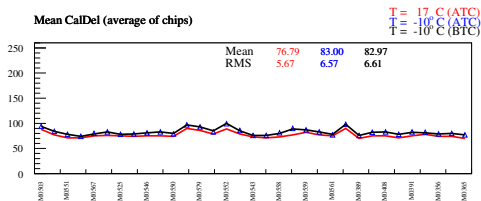
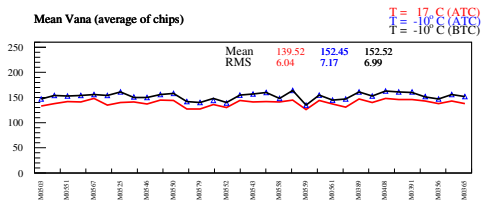
VcalThresholdWidth of chips



Vcal Thr. Width in e^-

Operational parameters I

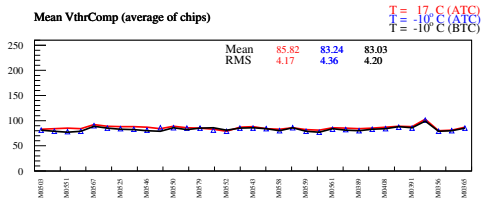
Mean DACs I



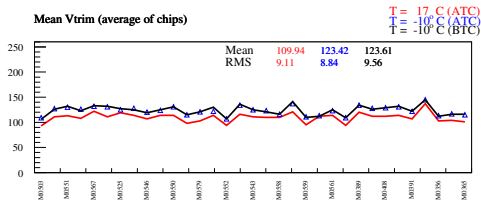
Operational parameters II

Mean DACs II

Mean VthrComp (average of chips)



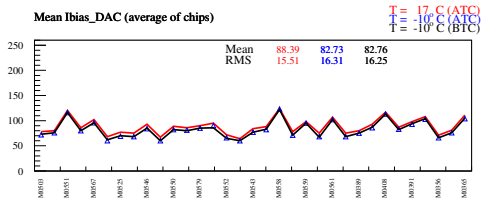
Mean Vtrim (average of chips)



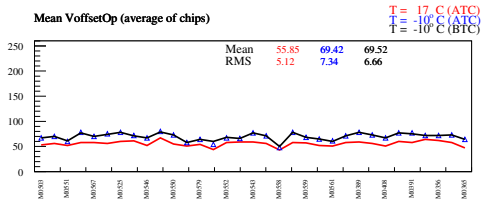
Operational parameters III

Mean DACs III

Mean Ibias_DAC (average of chips)



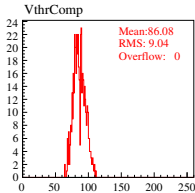
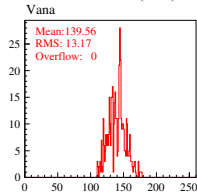
Mean VoffsetOp (average of chips)



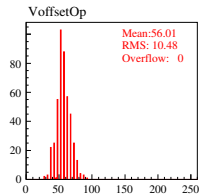
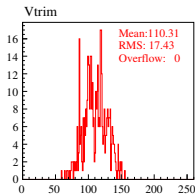
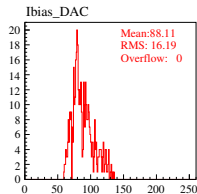
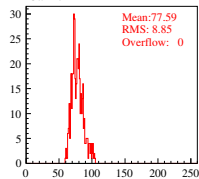
Operational parameters at $T = +17^{\circ}\text{C}$ (ATC)

DAC distribution (of chips)

DACs at $T = 17^{\circ}\text{C}$ (ATC)



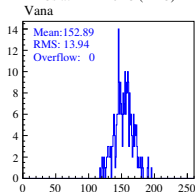
Modules: M0503 ... M0365
CalDel



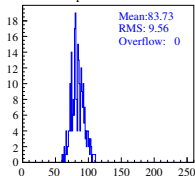
Operational parameters at $T = -10^{\circ}\text{C}$ (ATC)

DAC distribution (of chips)

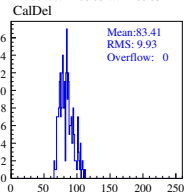
DACs at $T = -10^{\circ}\text{C}$ (ATC)



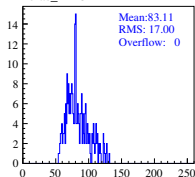
VthrComp



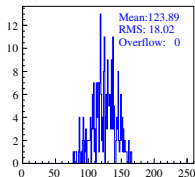
Modules: M0503 ... M0365



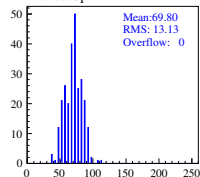
Ibias_DAC



Vtrim



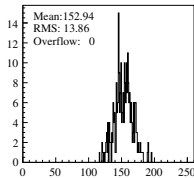
VoffsetOp



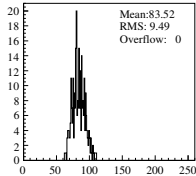
Operational parameters at $T = +17^{\circ}\text{C}$ (BTC)

DAC distribution (of chips)

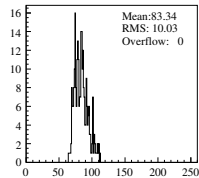
DACs at $T = -10^{\circ}\text{C}$ (BTC)
Vana



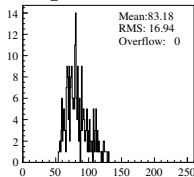
VthrComp



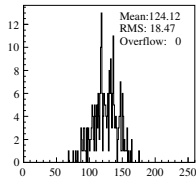
Modules: M0503 ... M0365
CalDel



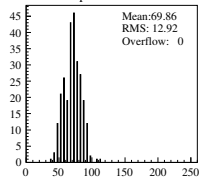
Ibias_DAC



Vtrim

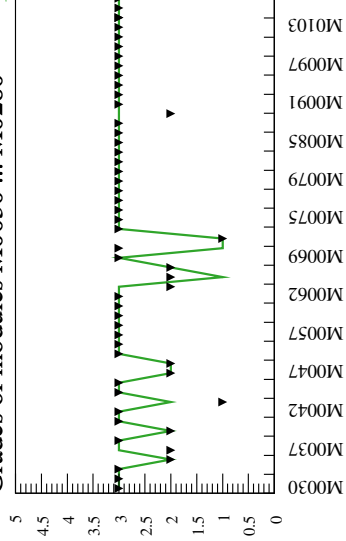


VoffsetOp



Retest Grades

Grades of modules M0030 ... M0280

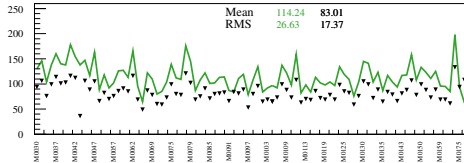


Operational parameters

Mean DACs I

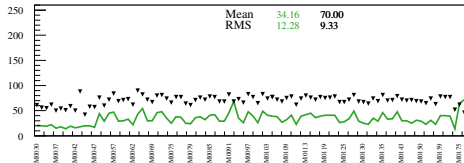
Mean Ibias_DAC (average of chips)

T = -10° C (ATC)
T = -10° C (ATC retest)



Mean VoffsetOp (average of chips)

T = -10° C (ATC)
T = -10° C (ATC retest)

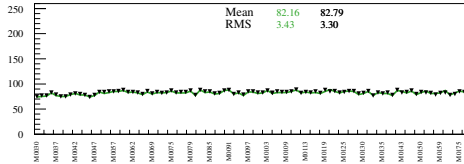


Operational parameters

Mean DACs II

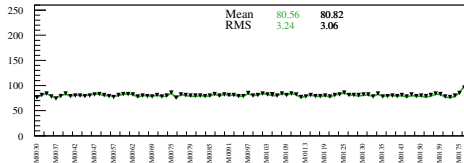
Mean VthrComp (average of chips)

T = -10. C (ATC)
T = -10° C (ATC retest)



Mean CalDel (average of chips)

T = -10. C (ATC)
T = -10° C (ATC retest)

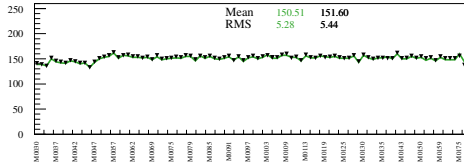


Operational parameters

Mean DACs III

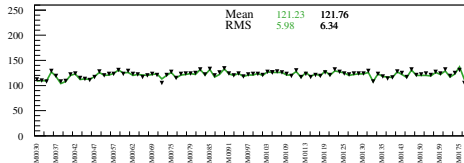
Mean Vana (average of chips)

T = -10° C (ATC)
T = -10° C (ATC retest)



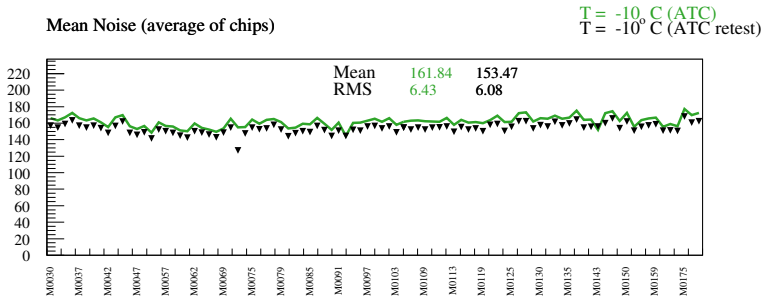
Mean Vtrim (average of chips)

T = -10° C (ATC)
T = -10° C (ATC retest)



Performance parameters

Mean **Noise** [e^-] vs. Module Nr.

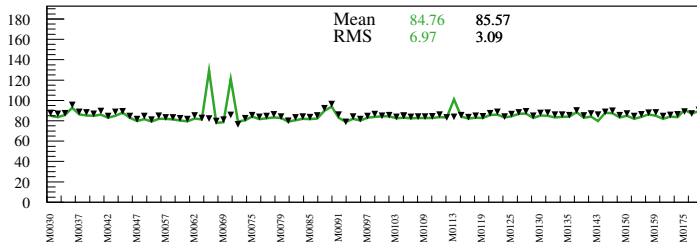


Performance parameters

Mean **VcalThresholdWidth** [e^-] vs. Module Nr.

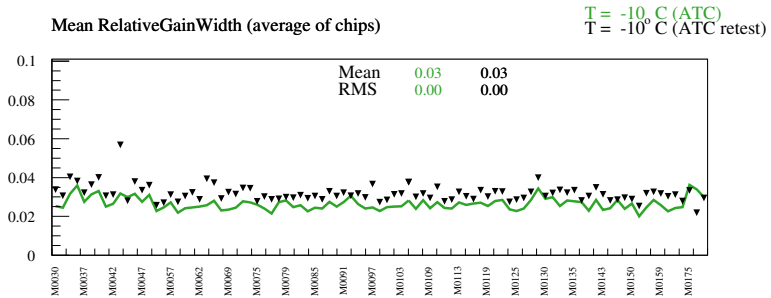
Mean VcalThrWidth (average of chips)

$T = -10^\circ\text{C}$ (ATC)
 $T = -10^\circ\text{C}$ (ATC retest)



Performance parameters

Mean **RelativeGainWidth** [%] vs. Module Nr.



Performance parameters

Mean **PedestalSpread** in [e^-] vs. Module Nr.

Mean PedestalSpread (average of chips)

$T = -10^\circ \text{C}$ (ATC)
 $T = -10^\circ \text{C}$ (ATC retest)

