

BPIX Module Testing Status - Week 1

12th January 2007

Production overview

Production Status: 342 modules produced (331 / 11)

- 237/46 graded as A/B → 83%
- 59 graded as C → 17%

Module Testing Report of Week 1:

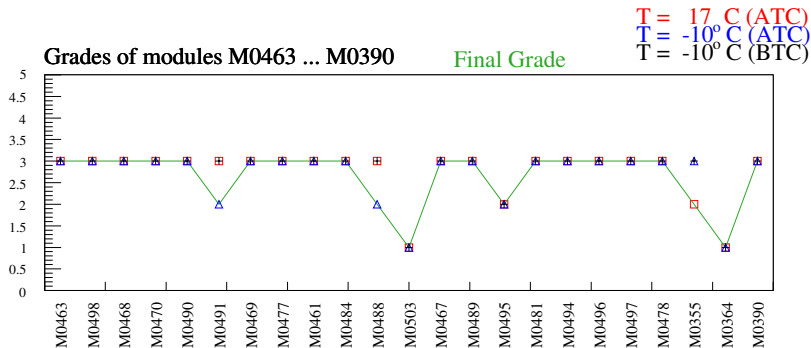
- 20/3 modules fully tested and therm. cycled (1 retested)

	Modules			Half-Modules		
Grade	A	B	C	A	B	C
T = -10° C, BTC*	18	1	1	2	0	1
T = -10° C, ATC	16	3	1	2	0	1
T = $+17^{\circ}$ C, ATC	18	1	1	1	1	1
Final Grade	16	3	1	1	1	1

- 15 were retested with new DAC settings (nothing changed)

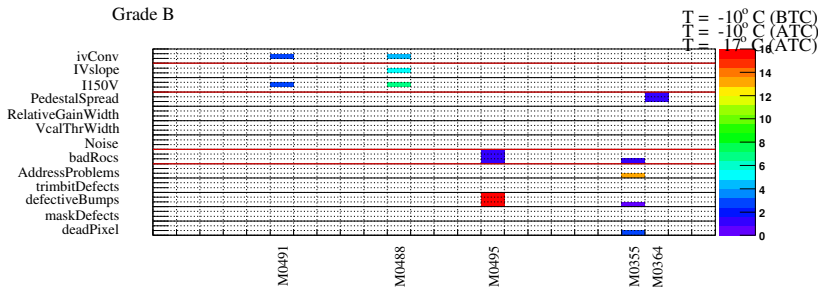
*without IV-criteria

Production summary

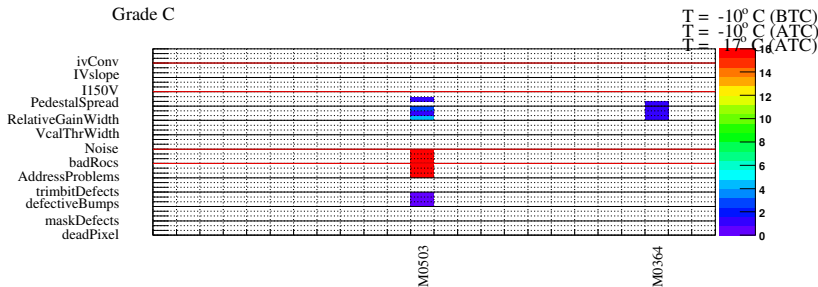


Module Failures Overview

Grade B



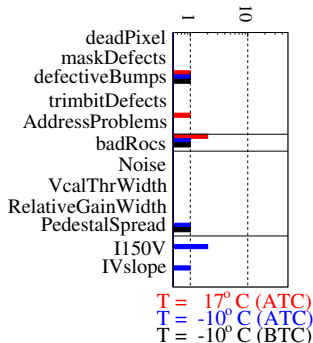
Grade C



Production quality

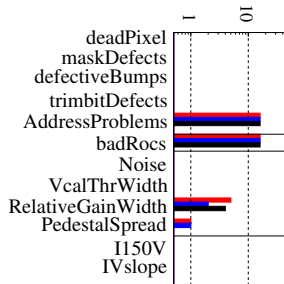
Chip Failures

Grade B
Grade B



Grade

Grade C



← Pixel defects

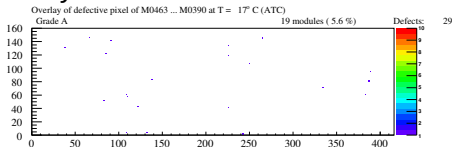
← Chip performance

← Module IV

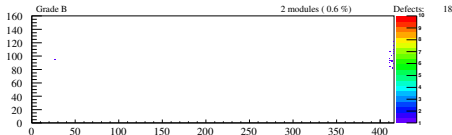
Defective pixel $T = 17^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = +17^{\circ}\text{C}$ (ATC)

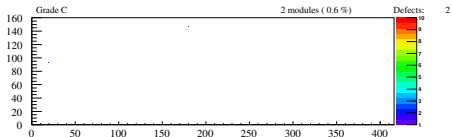
Grade A
(19 modules)



Grade B
(2 modules)



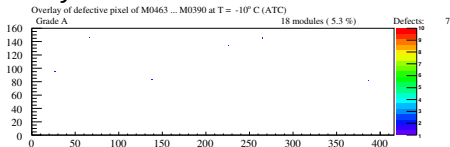
Grade C
(2 modules)



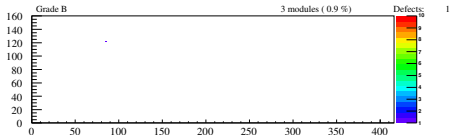
Defective pixel $T = -10^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (ATC)

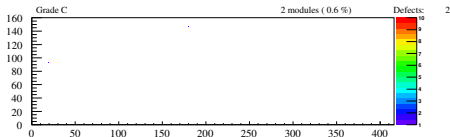
Grade A
(18 modules)



Grade B
(3 modules)



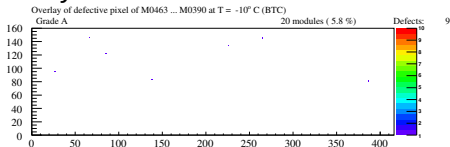
Grade C
(2 modules)



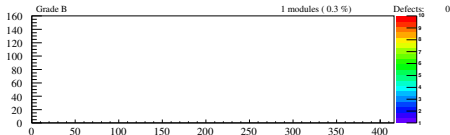
Defective pixel $T = -10^{\circ}\text{C}$ (BTC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (BTC)

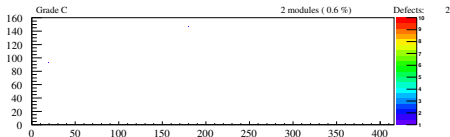
Grade A
(20 modules)



Grade B
(1 modules)



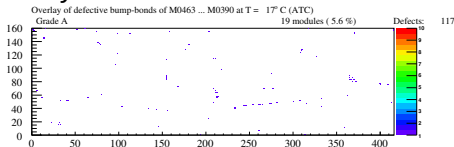
Grade C
(2 modules)



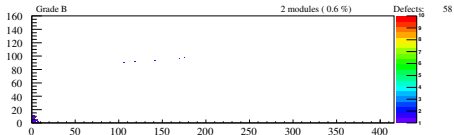
Defective bump-bonds $T = 17^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = +17^{\circ}\text{C}$ (ATC)

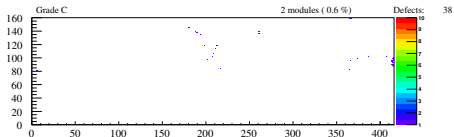
Grade A
(19 modules)



Grade B
(2 modules)



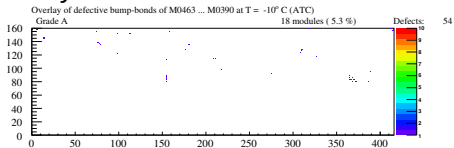
Grade C
(2 modules)



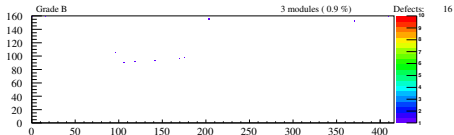
Defective bump-bonds $T = -10^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (ATC)

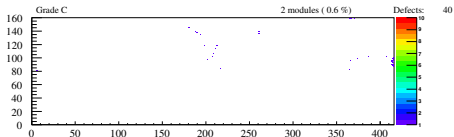
Grade A
(18 modules)



Grade B
(3 modules)



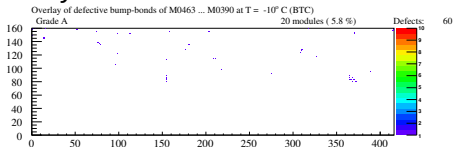
Grade C
(2 modules)



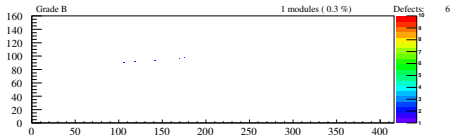
Defective bump-bonds $T = -10^{\circ}\text{C}$ (BTC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (BTC)

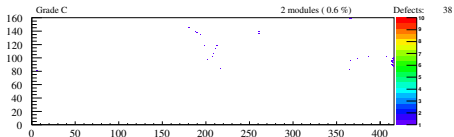
Grade A
(20 modules)



Grade B
(1 modules)

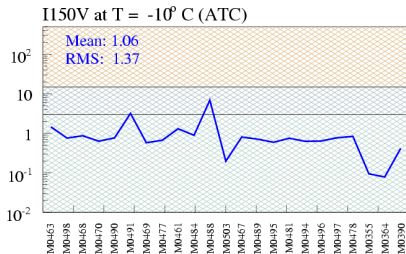


Grade C
(2 modules)

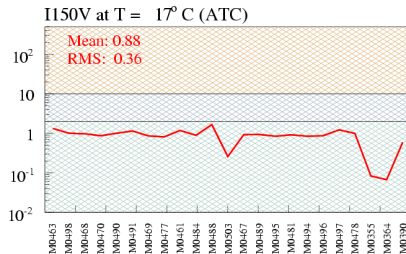


Current at 150 V

Current at 150 V (in μA) at $T = 17^\circ\text{C}$ and $T = -10^\circ\text{C}$



recalculated

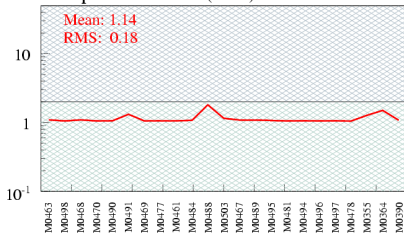


measured

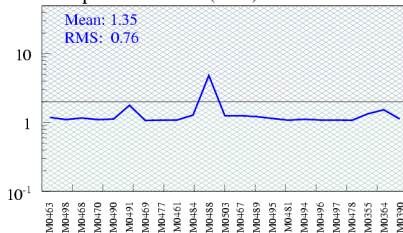
Slope of IV-Curve

Slope of IV-Curve at $T = 17^{\circ}\text{C}$ and $T = -10^{\circ}\text{C}$

IVslope at $T = 17^{\circ}\text{C}$ (ATC)

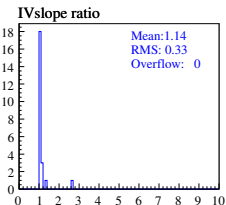
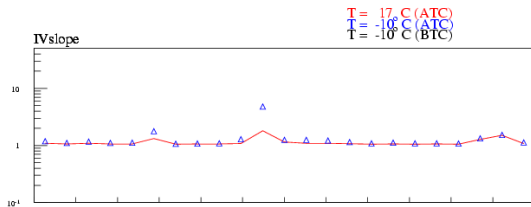
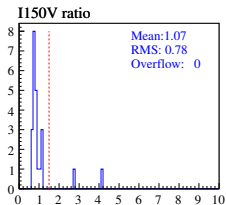
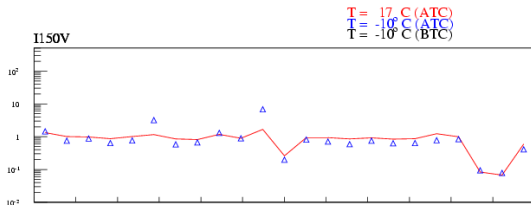


IVslope at $T = -10^{\circ}\text{C}$ (ATC)

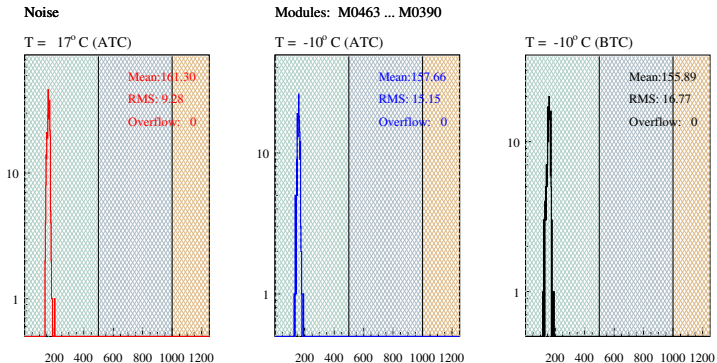


Current recalculation to $T = 17^{\circ}\text{C}$

Cross check of recalculated values with measured values

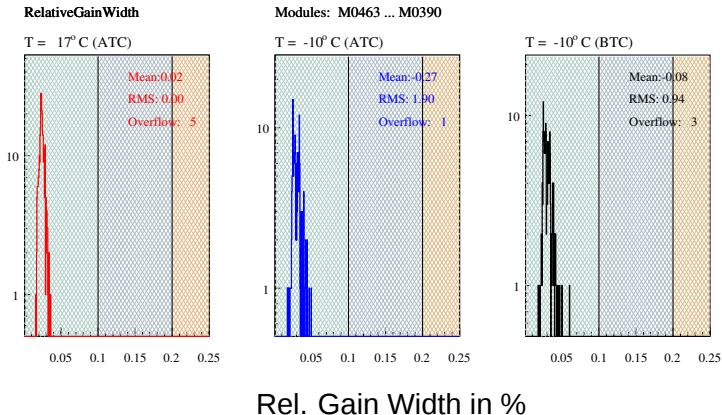


MeanNoise of chips

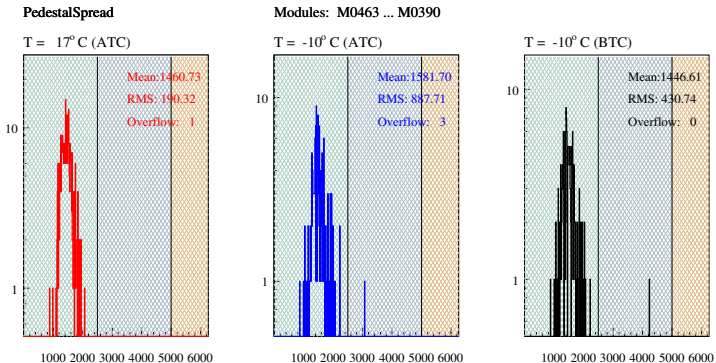


Noise in e^-

RelativeGainWidth of chips



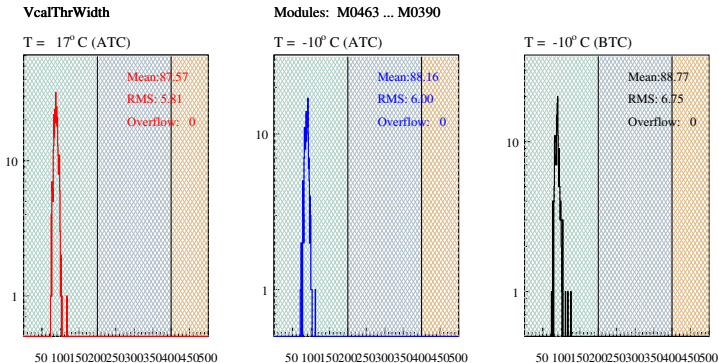
PedestalSpread of chips



Pedestal Spread in e^-

Vcal Threshold Width

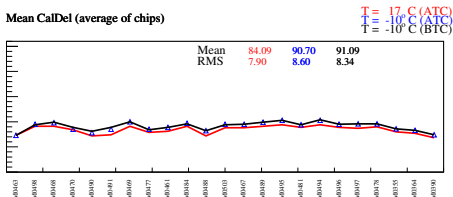
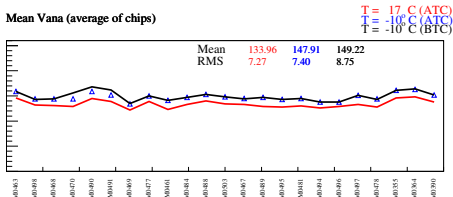
VcalThresholdWidth of chips



Vcal Thr. Width in e^-

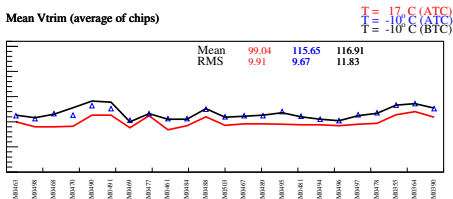
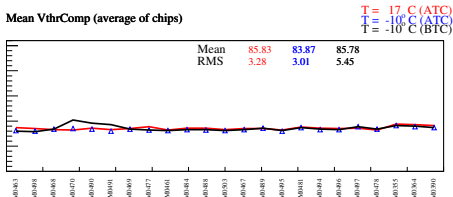
Operational parameters I

Mean DACs I



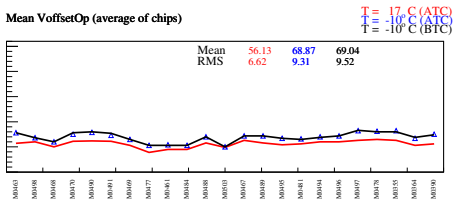
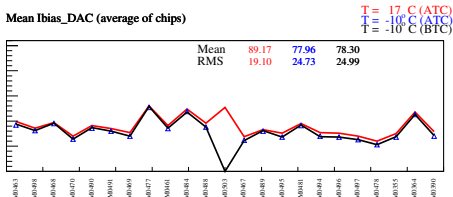
Operational parameters II

Mean DACs II



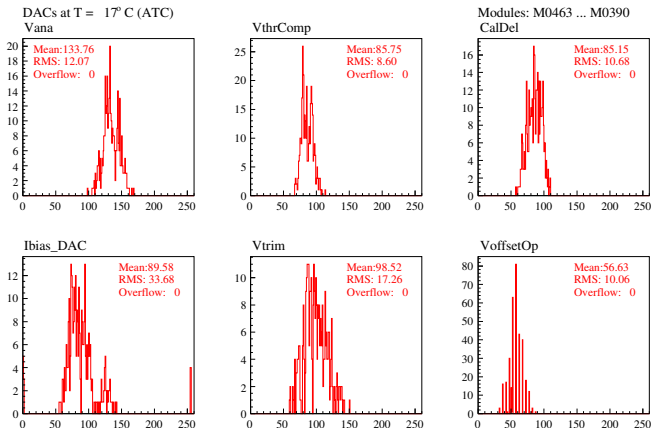
Operational parameters III

Mean DACs III



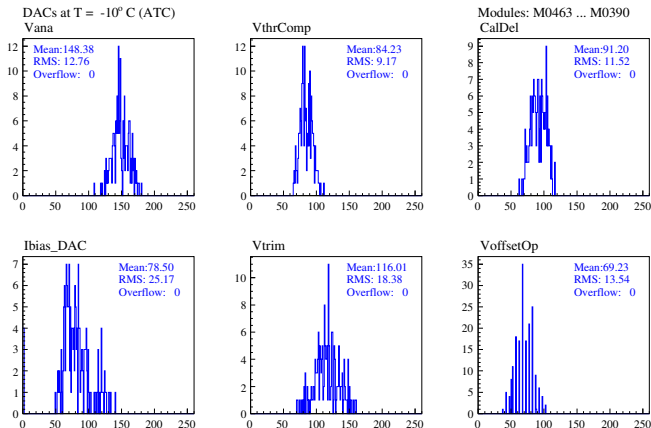
Operational parameters at $T = +17^{\circ}\text{C}$ (ATC)

DAC distribution (of chips)



Operational parameters at $T = -10^{\circ}\text{C}$ (ATC)

DAC distribution (of chips)

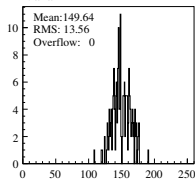


Operational parameters at $T = +17^{\circ}\text{C}$ (BTC)

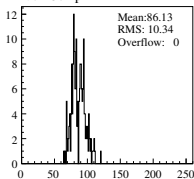
DAC distribution (of chips)

DACs at $T = -10^{\circ}\text{C}$ (BTC)

Vana

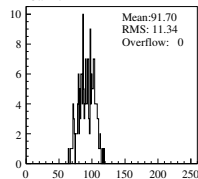


VthrComp

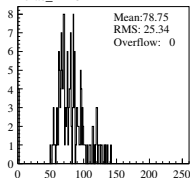


Modules: M0463 ... M0390

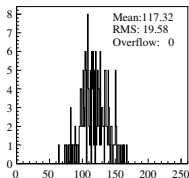
CalDel



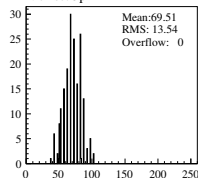
Ibias_DAC



Vtrim



VoffsetOp

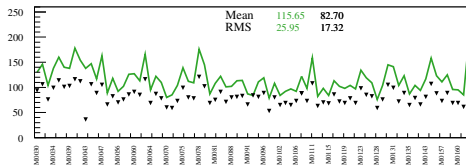


Operational parameters

Mean DACs I

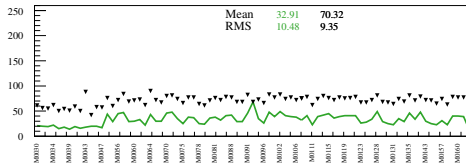
Mean Ibias_DAC (average of chips)

T = -10. C (ATC)
T = -10° C (ATC retest)



Mean VoffsetOp (average of chips)

T = -10. C (ATC)
T = -10° C (ATC retest)

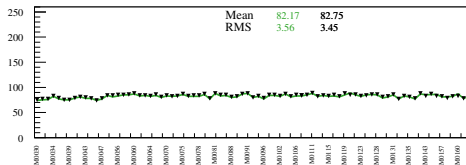


Operational parameters

Mean DACs II

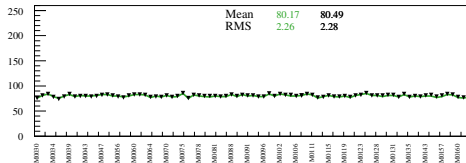
Mean VthrComp (average of chips)

T = -10°C (ATC)
T = -10°C (ATC retest)



Mean CalDel (average of chips)

T = -10°C (ATC)
T = -10°C (ATC retest)

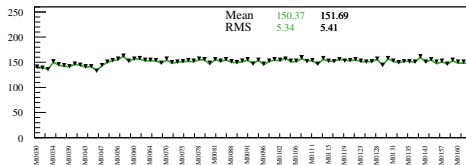


Operational parameters

Mean DACs III

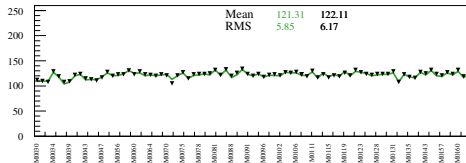
Mean Vana (average of chips)

T = -10° C (ATC)
T = -10° C (ATC retest)



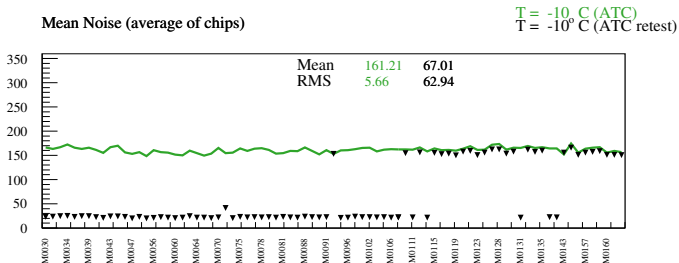
Mean Vtrim (average of chips)

T = -10° C (ATC)
T = -10° C (ATC retest)



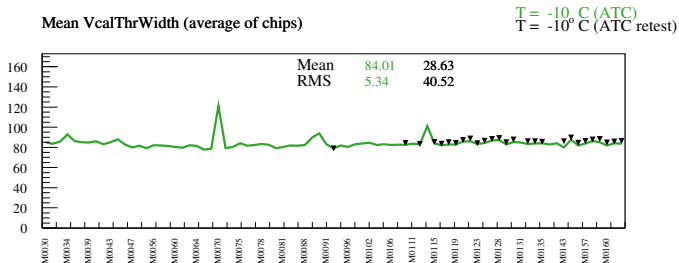
Performance parameters

Mean **Noise** [e^-] vs. Module Nr.



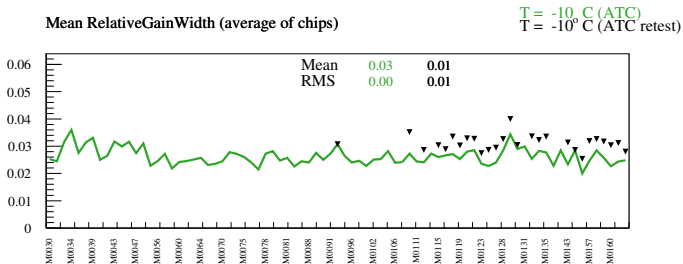
Performance parameters

Mean **VcalThresholdWidth** [e^-] vs. Module Nr.



Performance parameters

Mean **RelativeGainWidth** [%] vs. Module Nr.



Performance parameters

Mean PedestalSpread in $[e^-]$ vs. Module Nr.

