

BPIX Module Testing Status - Week 24 (2006)

26th September 2008

Production overview

Production Status: 5 modules produced (5 / 0)

- 0/0 graded as A/B → 0% || 0/0 → %
- 5 graded as C → 100% || 0 → %

Module Testing Report of Week 24 (2006):

- 2/— modules fully tested and therm. cycled (0 retested)

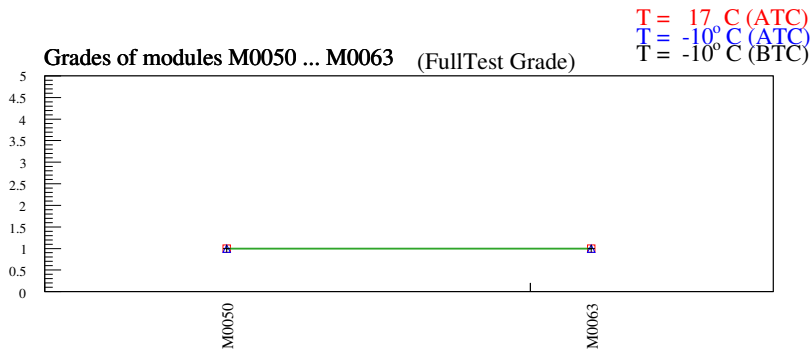
	Modules			Half-Modules		
Grade	A	B	C	A	B	C
T = -10° C, BTC*	0	0	2	—	—	—
T = -10° C, ATC	0	0	2	—	—	—
T = +17° C, ATC	0	0	2	—	—	—
Final Grade	0	0	2	—	—	—

- 12 were retested with new DAC settings (2 change)

- M0064: A -> B -> overall grades + M0070: C -> A -> overall grades

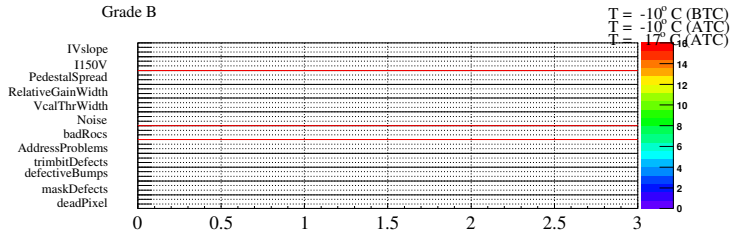
*without IV-criteria

Production summary

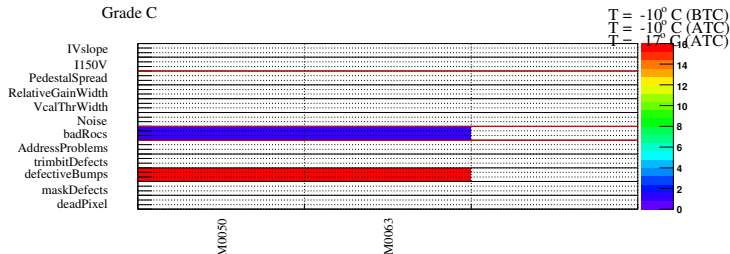


Module Failures Overview

Grade B



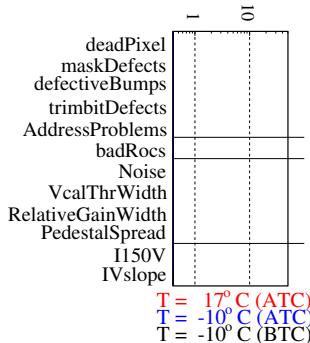
Grade C



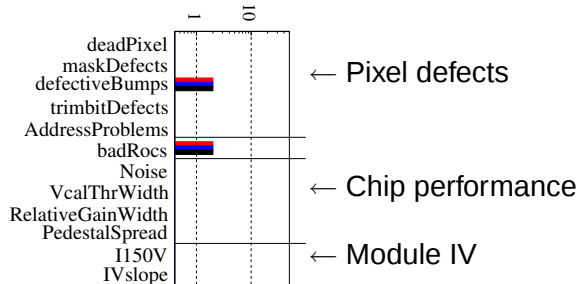
Production quality

Chip Failures

Grade B
Grade B



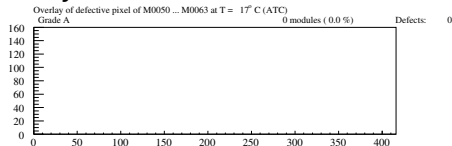
Grade C
Grade C



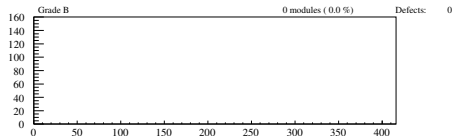
Defective pixel $T = 17^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = +17^{\circ}\text{C}$ (ATC)

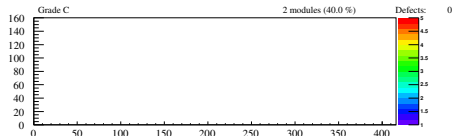
Grade A
(0 modules)



Grade B
(0 modules)



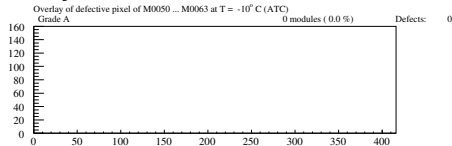
Grade C
(2 modules)



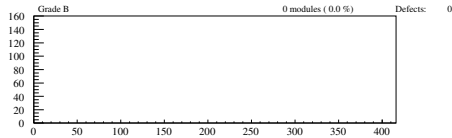
Defective pixel $T = -10^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (ATC)

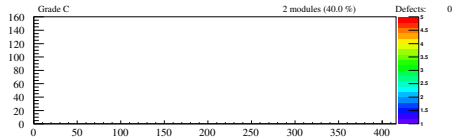
Grade A
(0 modules)



Grade B
(0 modules)



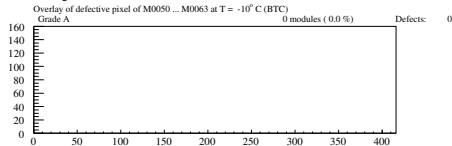
Grade C
(2 modules)



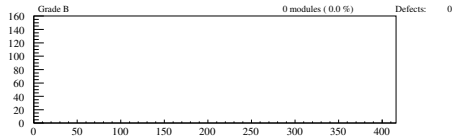
Defective pixel $T = -10^{\circ}\text{C}$ (BTC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (BTC)

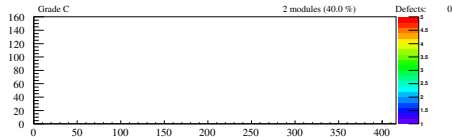
Grade A
(0 modules)



Grade B
(0 modules)



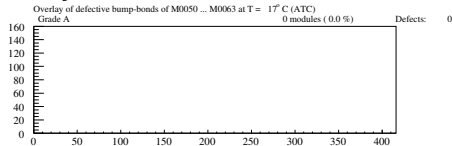
Grade C
(2 modules)



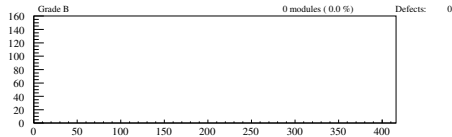
Defective bump-bonds $T = 17^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = +17^{\circ}\text{C}$ (ATC)

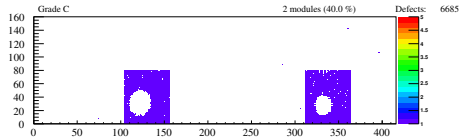
Grade A
(0 modules)



Grade B
(0 modules)



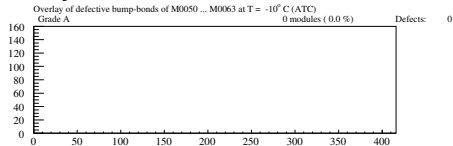
Grade C
(2 modules)



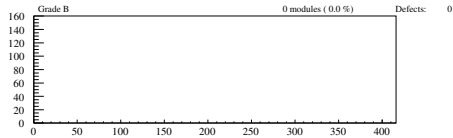
Defective bump-bonds $T = -10^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (ATC)

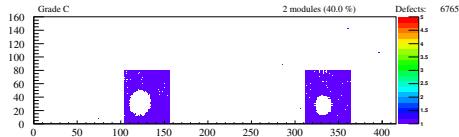
Grade A
(0 modules)



Grade B
(0 modules)



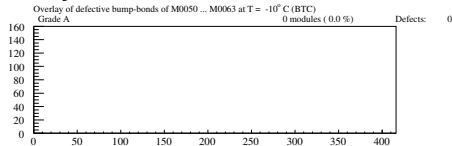
Grade C
(2 modules)



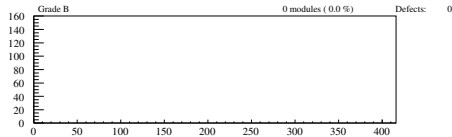
Defective bump-bonds $T = -10^{\circ}\text{C}$ (BTC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (BTC)

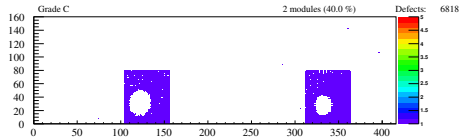
Grade A
(0 modules)



Grade B
(0 modules)



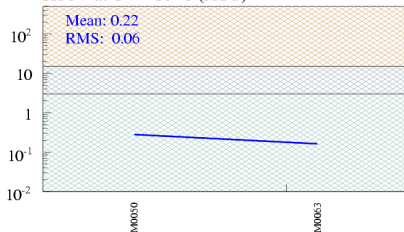
Grade C
(2 modules)



Current at 150 V

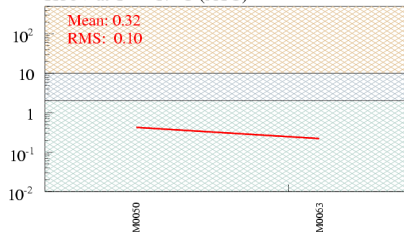
Current at 150 V (in μA) at $T = 17^\circ\text{C}$ and $T = -10^\circ\text{C}$

I150V at T = -10°C (ATC)



recalculated

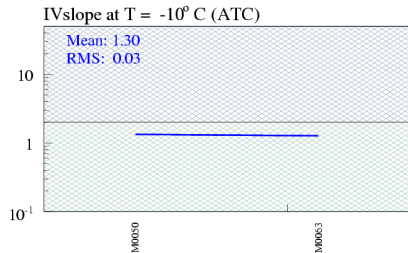
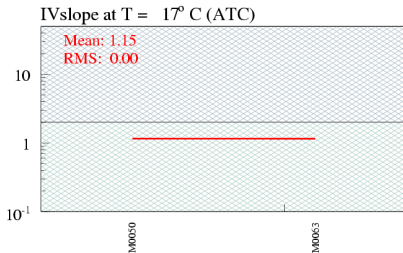
I150V at T = 17°C (ATC)



measured

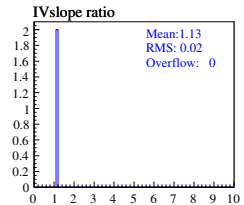
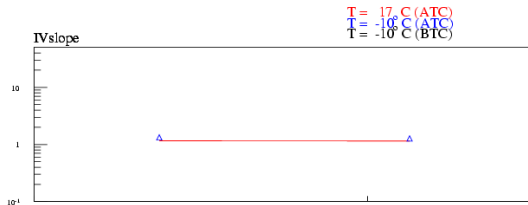
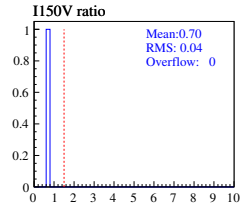
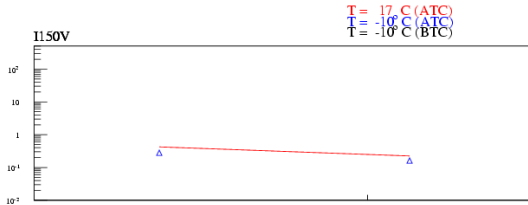
Slope of IV-Curve

Slope of IV-Curve at $T = 17^{\circ}\text{C}$ and $T = -10^{\circ}\text{C}$



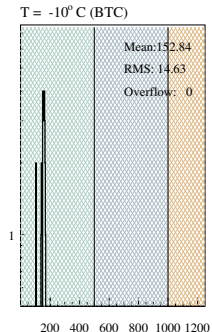
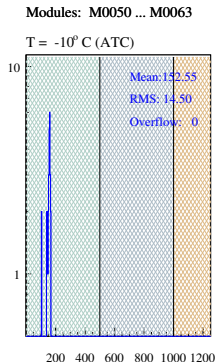
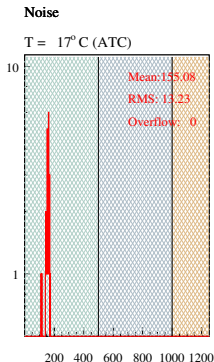
Current recalculation to $T = 17^{\circ}\text{C}$

Cross check of recalculated values with measured values



Noise

MeanNoise of chips



Noise in e^-

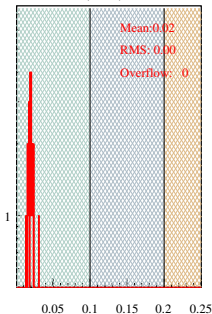
Relative Gain Width

RelativeGainWidth of chips

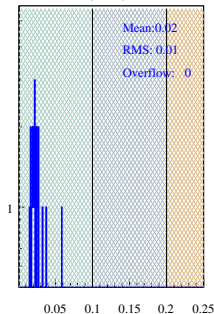
RelativeGainWidth

Modules: M0050 ... M0063

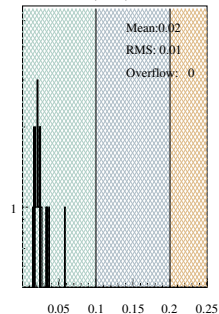
T = 17° C (ATC)



T = -10° C (ATC)



T = -10° C (BTC)



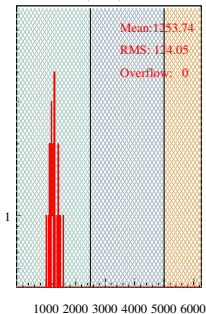
Rel. Gain Width in %

Pedestal Spread

PedestalSpread of chips

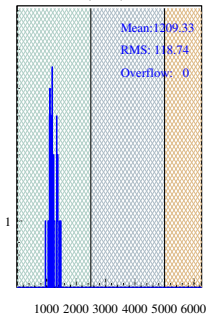
PedestalSpread

T = 17° C (ATC)

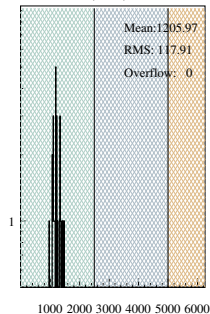


Modules: M0050 ... M0063

T = -10° C (ATC)



T = -10° C (BTC)



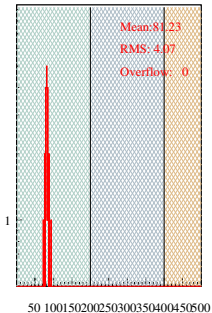
Pedestal Spread in e^-

Vcal Threshold Width

VcalThresholdWidth of chips

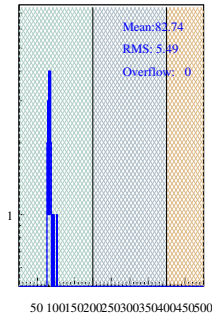
VcalThrWidth

T = 17° C (ATC)

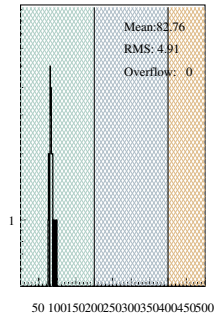


Modules: M0050 ... M0063

T = -10° C (ATC)



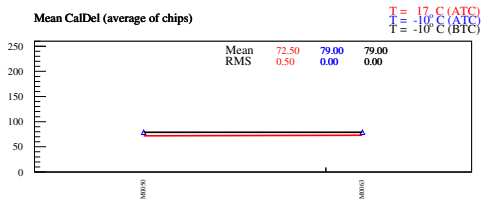
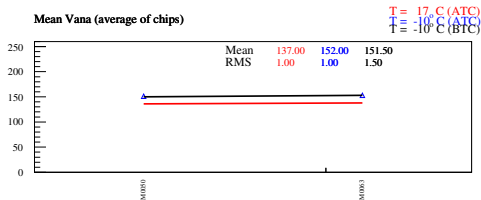
T = -10° C (BTC)



Vcal Thr. Width in e^-

Operational parameters I

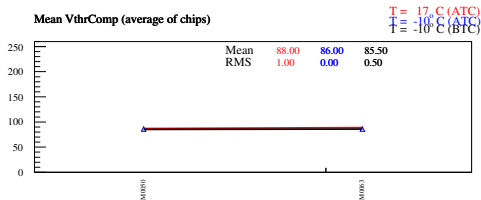
Mean DACs I



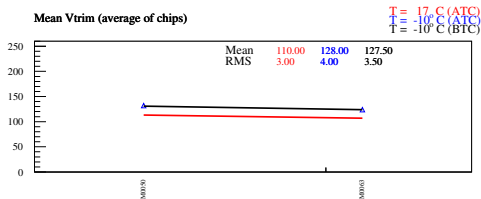
Operational parameters II

Mean DACs II

Mean VthrComp (average of chips)



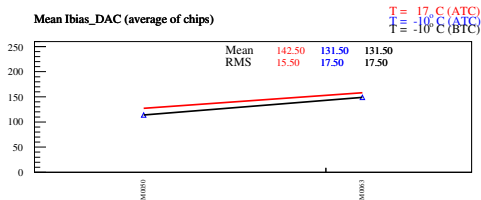
Mean Vtrim (average of chips)



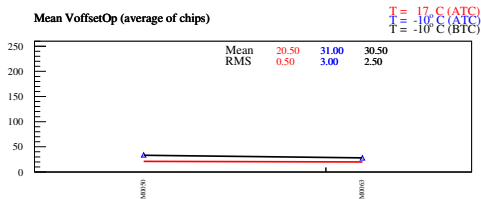
Operational parameters III

Mean DACs III

Mean Ibias_DAC (average of chips)

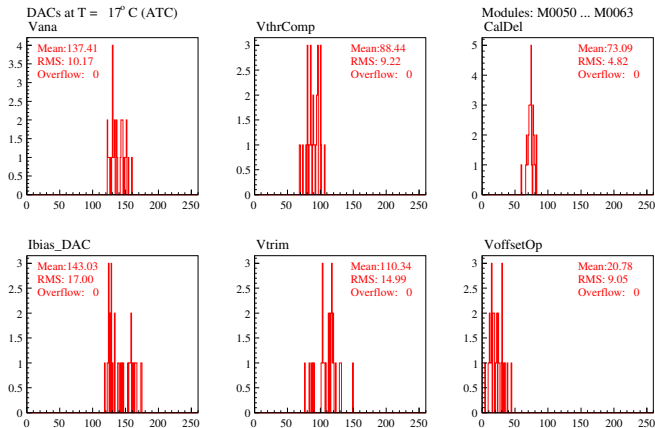


Mean VoffsetOp (average of chips)



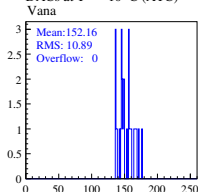
Operational parameters at $T = +17^{\circ}\text{C}$ (ATC)

DAC distribution (of chips)

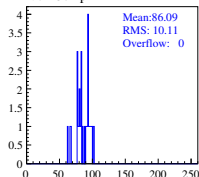


Operational parameters at $T = -10^{\circ}\text{C}$ (ATC)

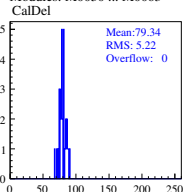
DAC distribution (of chips)

DACs at $T = -10^{\circ}\text{C}$ (ATC)

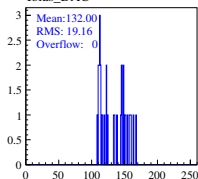
VthrComp



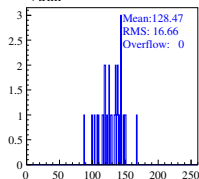
Modules: M0050 ... M0063



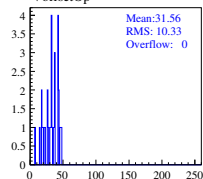
Ibias_DAC



Vtrim

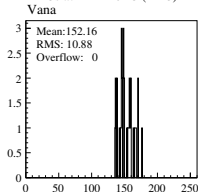


VoffsetOp

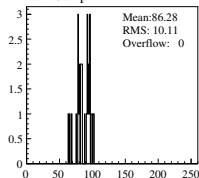


Operational parameters at $T = +17^{\circ}\text{C}$ (BTC)

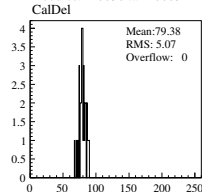
DAC distribution (of chips)

DACs at $T = -10^{\circ}\text{C}$ (BTC)

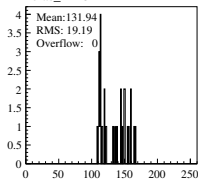
VthrComp



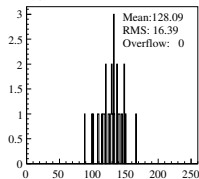
Modules: M0050 ... M0063



Ibias_DAC



Vtrim



VoffsetOp

