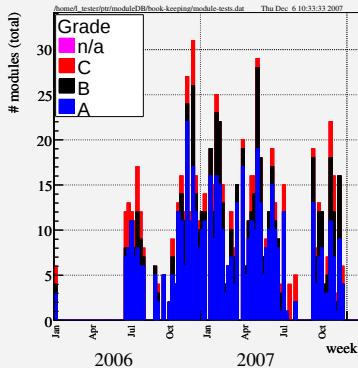


BPIX Module Testing Status - 2007

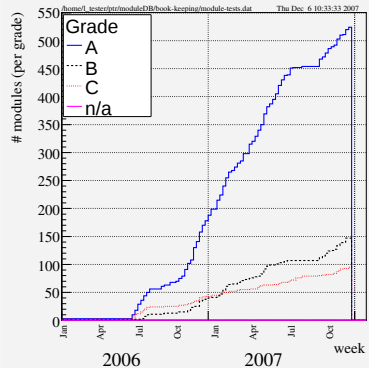
6th December 2007

Production Overview

Tested Modules in 2006/2007 (incl. half-modules)



Tested Modules in 2006/2007 (incl. half-modules)



Production overview

Production Status: 883 modules produced (762 full/ 121 half)

- 523/145 graded as A/B → 88% || 87/23 → 91%
- 94 graded as C → 12% || 11 → 9%

Module Testing Report of 2007:

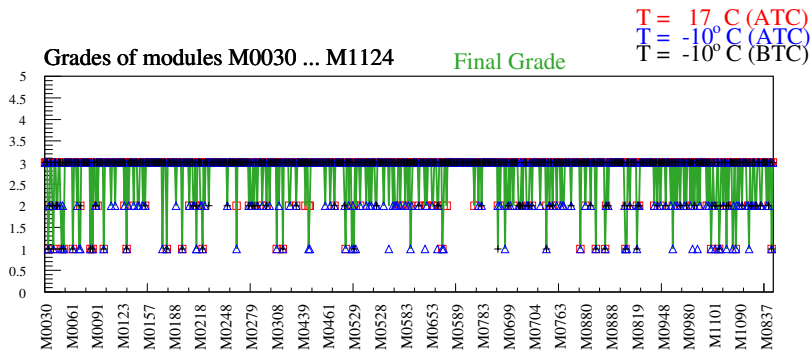
- 708 modules fully tested and therm. cycled (62 retested)

	Modules (708)			Halfmodules (119)		
Grade	A	B	C	A	B	C
T = -10° C, BTC*	626	60	22	108	5	8
T = -10° C, ATC	535	122	51	94	18	9
T = +17° C, ATC	605	79	24	98	13	10
Final Grade	523	143	42	87	23	9

- 90 were retested with new DAC settings (7 change)

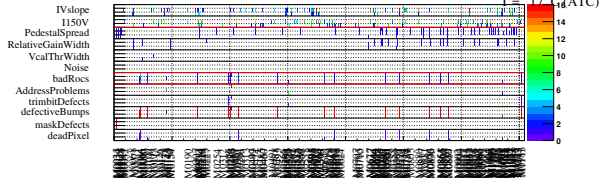
+ M0037: B -> A -> overall grades + M0043: C -> B -> overall grades + M0064: B -> A -> overall grades -
M0070: A -> C -> overall grades - M0143: A -> B -> overall grades + M0067: B -> A -> overall grades -
M0145: A -> B -> overall grades

Production summary

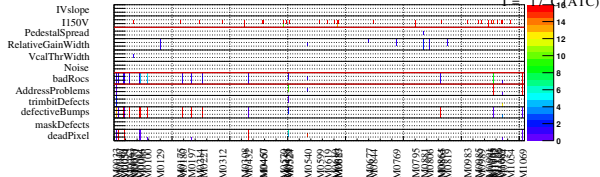


Module Failures Overview

Grade B



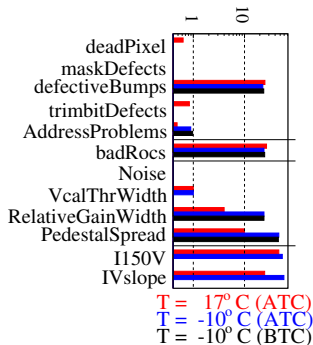
Grade C



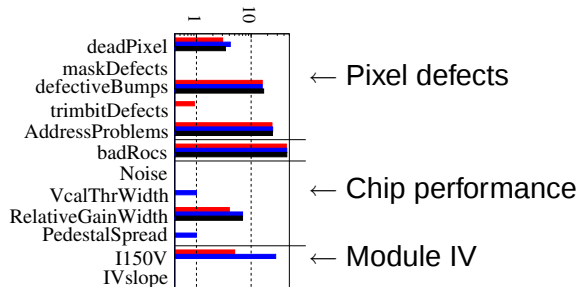
Production quality

Chip Failures

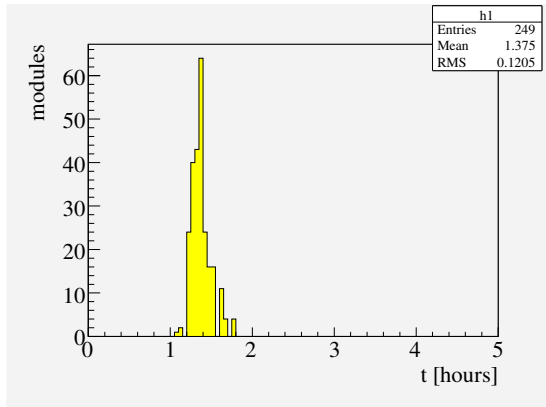
Grade B
Grade B



Grade C
Grade C



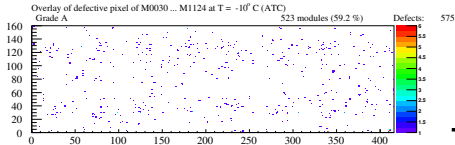
Test duration



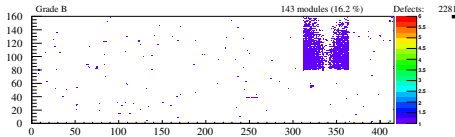
Dead pixel

Overlay of modules tested at $T = -10^{\circ}\text{C}$ (ATC)

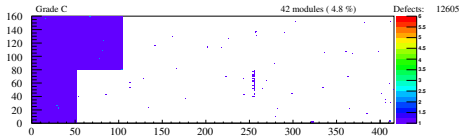
Final Grade A
(523 modules)



Final Grade B
(143 modules)



Final Grade C
(42 modules)



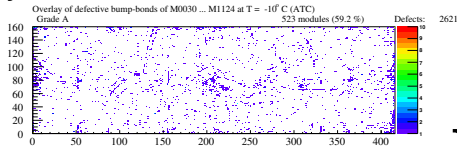
} 44.3 Mio. Pixel

2.8 Mio. Pixel

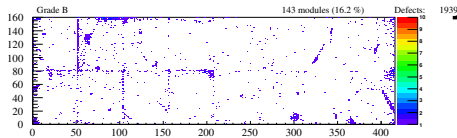
Defective bump-bonds

Overlay of modules tested at $T = -10^{\circ}\text{C}$ (ATC)

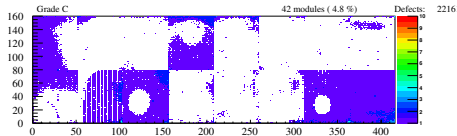
Final Grade A
(523 modules)



Final Grade B
(143 modules)



Final Grade C
(42 modules)

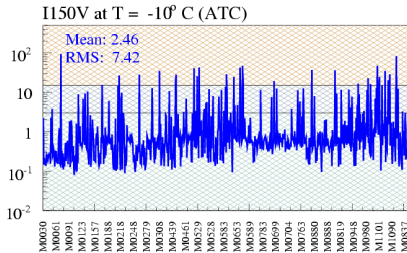


} 44.3 Mio. Pixel

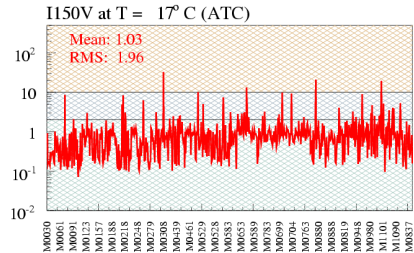
2.8 Mio. Pixel

Current at 150 V

Current at 150 V (in μA) at $T = 17^\circ\text{C}$ and $T = -10^\circ\text{C}$



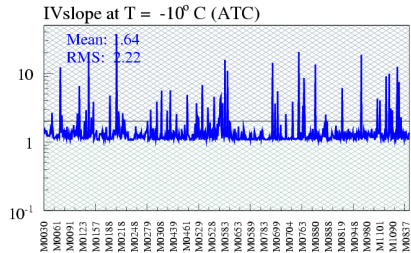
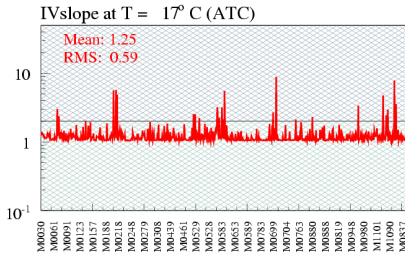
recalculated



measured

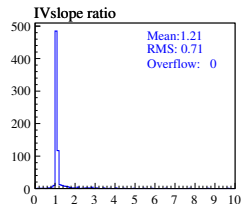
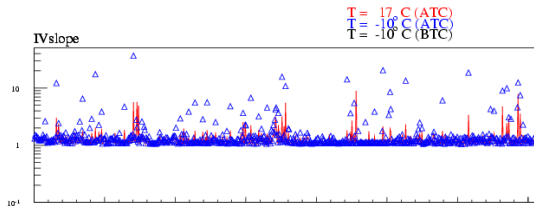
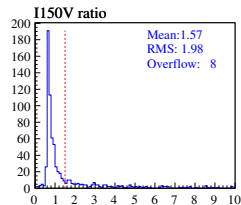
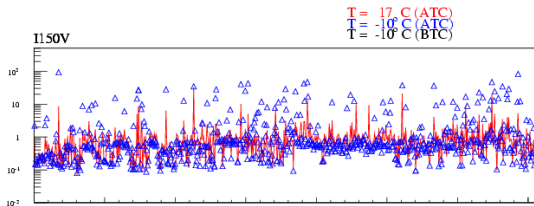
Slope of IV-Curve

Slope of IV-Curve at $T = 17^{\circ}\text{C}$ and $T = -10^{\circ}\text{C}$



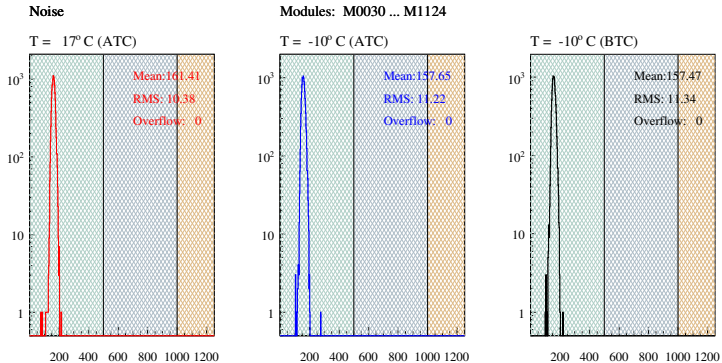
Current recalculation to $T = 17^{\circ}\text{C}$

Cross check of recalculated values with measured values



Noise

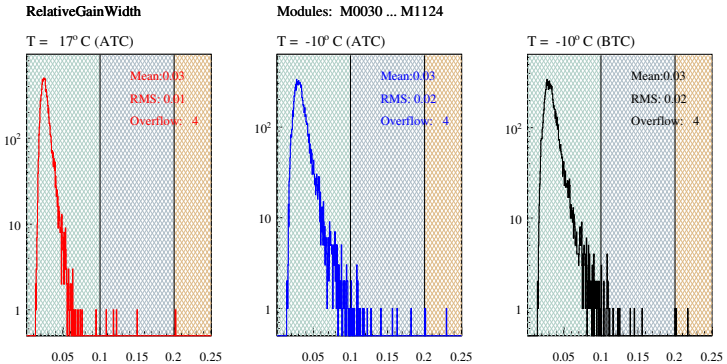
MeanNoise of chips



Noise in e^-

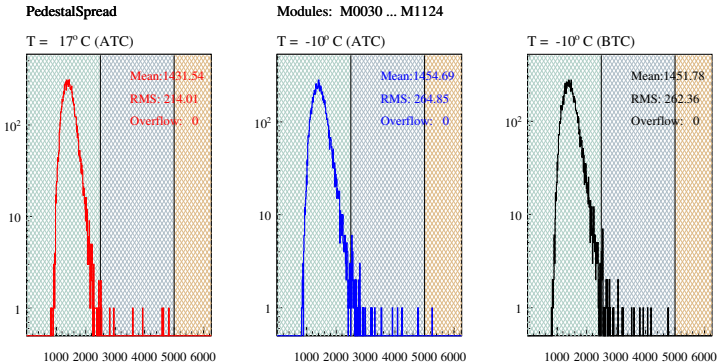
Relative Gain Width

RelativeGainWidth of chips



Pedestal Spread

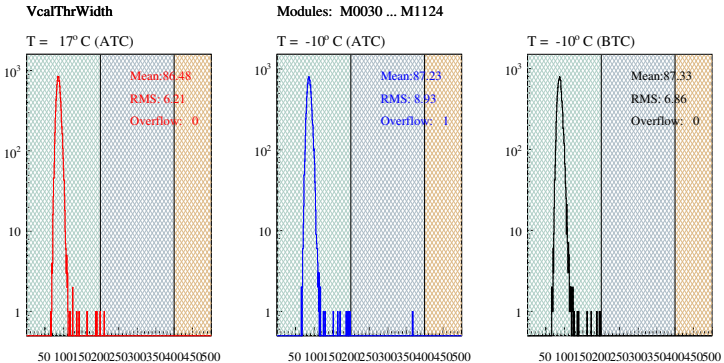
PedestalSpread of chips



Pedestal Spread in e^-

Vcal Threshold Width

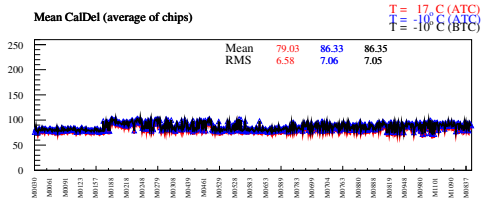
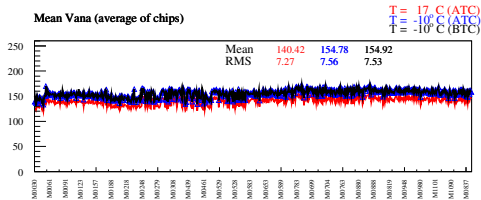
VcalThresholdWidth of chips



Vcal Thr. Width in e^-

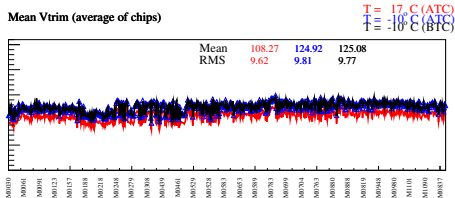
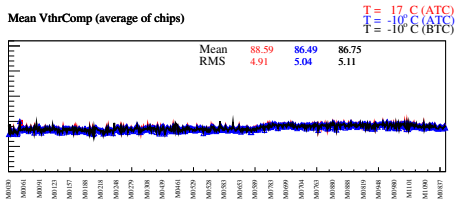
Operational parameters I

Mean DACs I



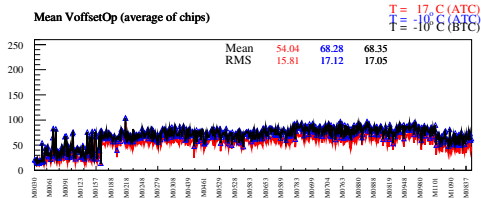
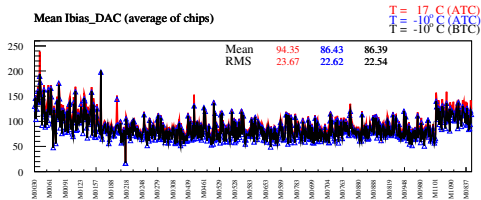
Operational parameters II

Mean DACs II



Operational parameters III

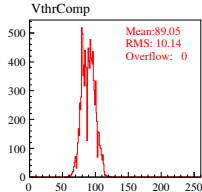
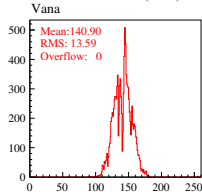
Mean DACs III



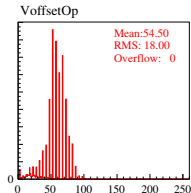
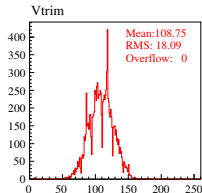
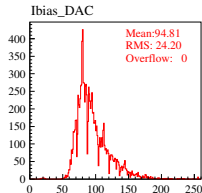
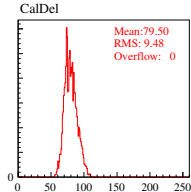
Operational parameters at $T = +17^{\circ}\text{C}$ (ATC)

DAC distribution (of chips)

DACs at $T = 17^{\circ}\text{C}$ (ATC)



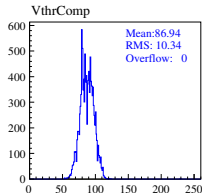
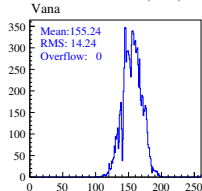
Modules: M0030 ... M1124



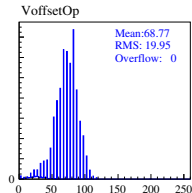
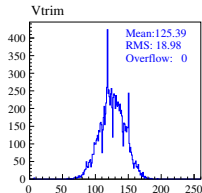
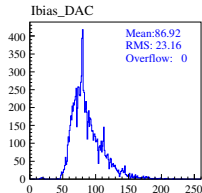
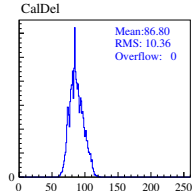
Operational parameters at $T = -10^{\circ}\text{C}$ (ATC)

DAC distribution (of chips)

DACs at $T = -10^{\circ}\text{C}$ (ATC)



Modules: M0030 ... M1124

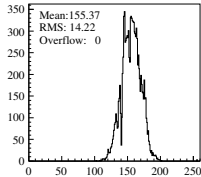


Operational parameters at $T = +17^{\circ}\text{C}$ (BTC)

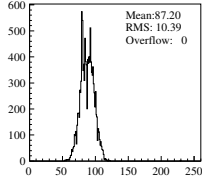
DAC distribution (of chips)

DACs at $T = -10^{\circ}\text{C}$ (BTC)

Vana

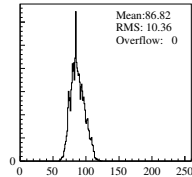


VthrComp

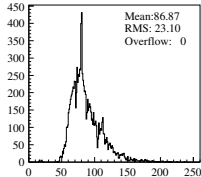


Modules: M0030 ... M1124

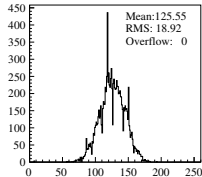
CalDel



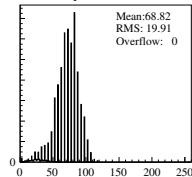
Ibias_DAC



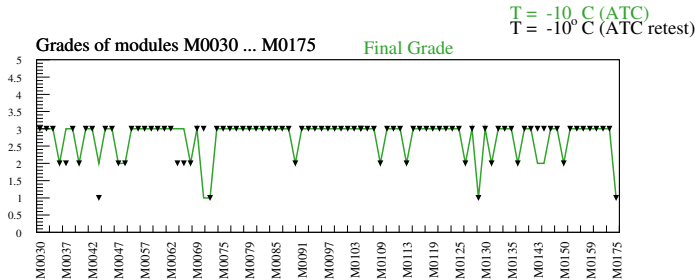
Vtrim



VoffsetOp



Retest Grades

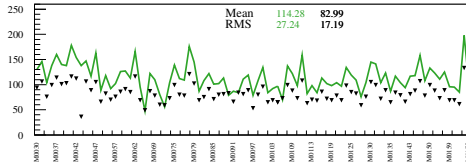


Operational parameters

Mean DACs I

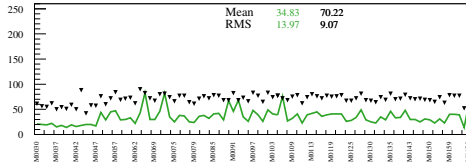
Mean Ibias_DAC (average of chips)

$T = -10^{\circ}\text{C (ATC)}$
 $T = -10^{\circ}\text{C (ATC retest)}$



Mean VoffsetOp (average of chips)

$T = -10^{\circ}\text{C (ATC)}$
 $T = -10^{\circ}\text{C (ATC retest)}$

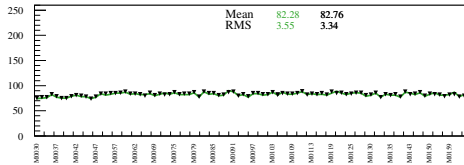


Operational parameters

Mean DACs II

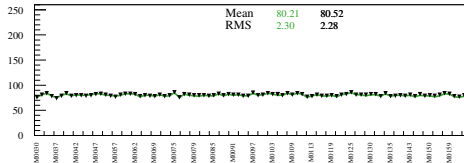
Mean VthrComp (average of chips)

$T = -10^{\circ}\text{C (ATC)}$
 $T = -10^{\circ}\text{C (ATC retest)}$



Mean CalDel (average of chips)

$T = -10^{\circ}\text{C (ATC)}$
 $T = -10^{\circ}\text{C (ATC retest)}$

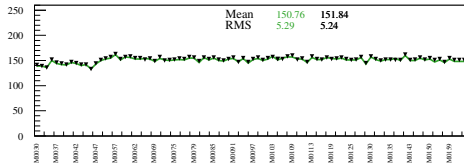


Operational parameters

Mean DACs III

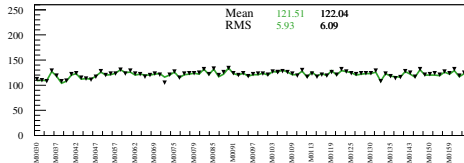
Mean Vana (average of chips)

$T = -10^{\circ}\text{C (ATC)}$
 $T = -10^{\circ}\text{C (ATC retest)}$



Mean Vtrim (average of chips)

$T = -10^{\circ}\text{C (ATC)}$
 $T = -10^{\circ}\text{C (ATC retest)}$

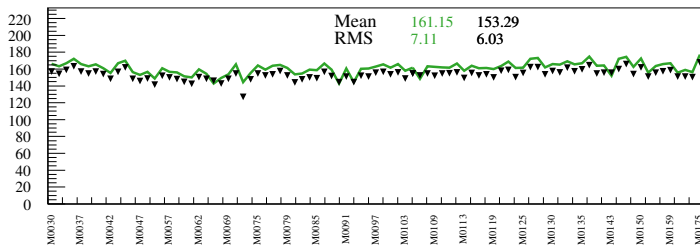


Performance parameters

Mean Noise [e^-] vs. Module Nr.

Mean Noise (average of chips)

$T = -10^\circ \text{C}$ (ATC)
 $T = -10^\circ \text{C}$ (ATC retest)

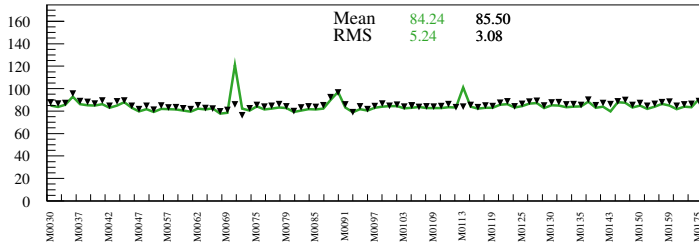


Performance parameters

Mean **VcalThresholdWidth** [e^-] vs. Module Nr.

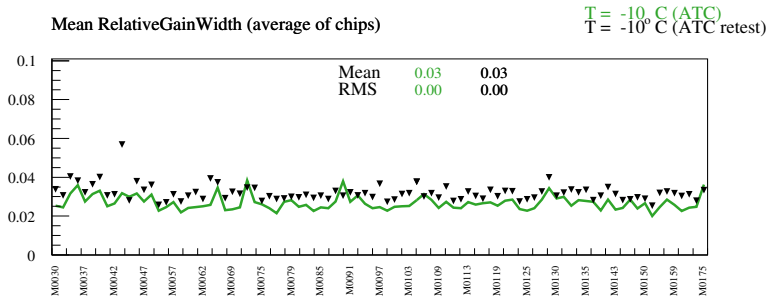
Mean VcalThrWidth (average of chips)

$T = -10^\circ \text{C}$ (ATC)
 $T = -10^\circ \text{C}$ (ATC retest)



Performance parameters

Mean **RelativeGainWidth** [%] vs. Module Nr.



Performance parameters

Mean **PedestalSpread** in [e^-] vs. Module Nr.

Mean PedestalSpread (average of chips)

T = -10° C (ATC)
T = -10° C (ATC retest)

