

BPIX Module Testing Status - Week 9

5th March 2007

Production overview

Production Status: 474 modules produced (421 / 53)

- 291/65 graded as A/B → 85% || 40/9 → 92%
- 65 graded as C → 15% || 4 → 8%

Module Testing Report of Week 9:

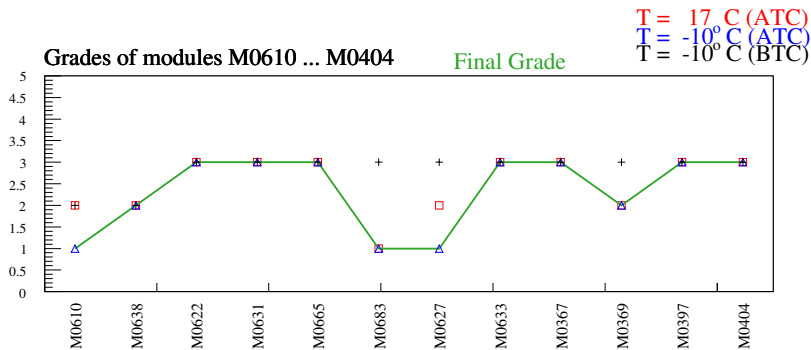
- 8/4 modules fully tested and therm. cycled (0 retested)

	Modules			Half-Modules		
Grade	A	B	C	A	B	C
T = -10° C, BTC*	6	2	0	4	0	0
T = -10° C, ATC	4	1	3	3	1	0
T = +17° C, ATC	4	3	1	3	1	0
Final Grade	4	1	3	3	1	0

- 2 were retested with new DAC settings (nothing changed)

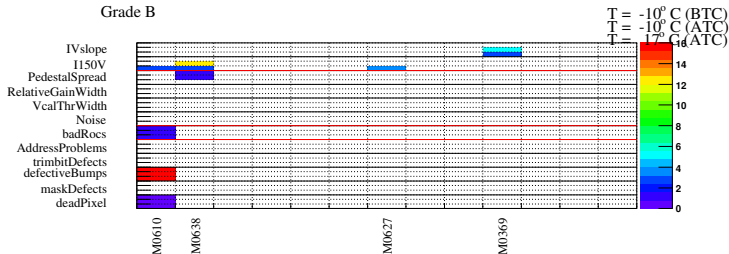
*without IV-criteria

Production summary

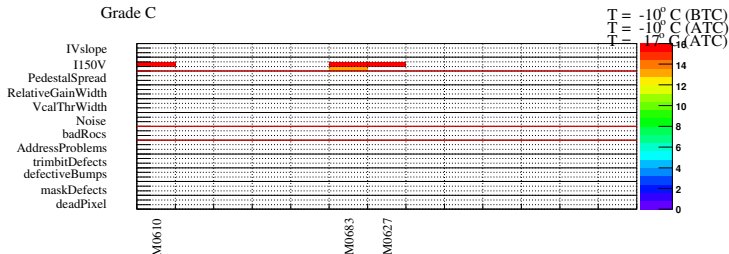


Module Failures Overview

Grade B



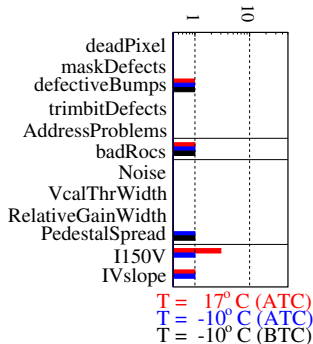
Grade C



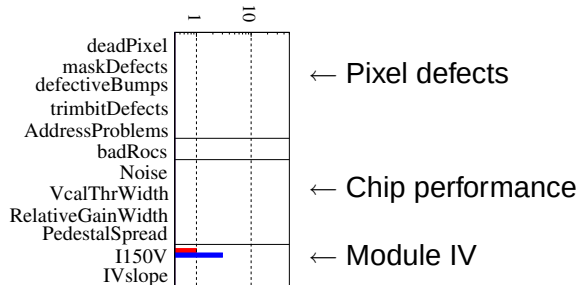
Production quality

Chip Failures

Grade B
Grade B



Grade C
Grade C



← Pixel defects

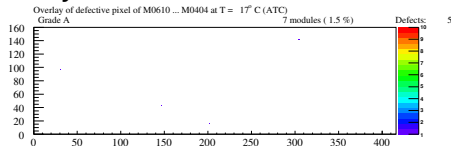
← Chip performance

← Module IV

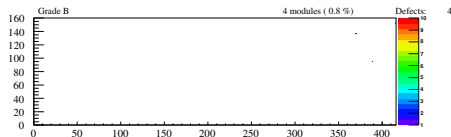
Defective pixel $T = 17^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = +17^{\circ}\text{C}$ (ATC)

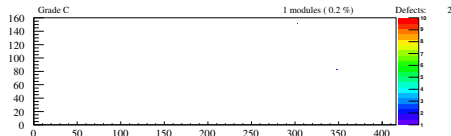
Grade A
(7 modules)



Grade B
(4 modules)



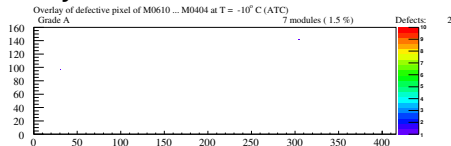
Grade C
(1 modules)



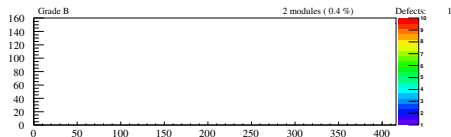
Defective pixel $T = -10^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (ATC)

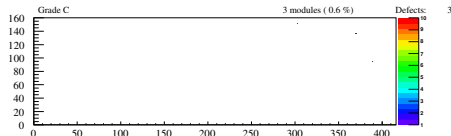
Grade A
(7 modules)



Grade B
(2 modules)



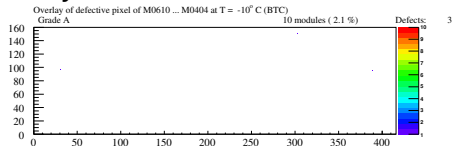
Grade C
(3 modules)



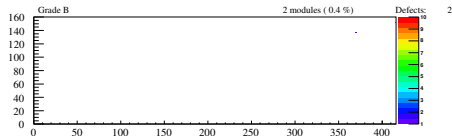
Defective pixel $T = -10^0\text{C}$ (BTC)

Overlay of all fully tested modules at $T = -10^0\text{C}$ (BTC)

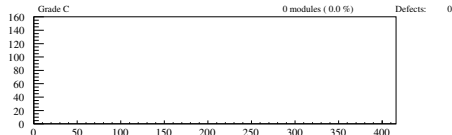
Grade A
(10 modules)



Grade B
(2 modules)



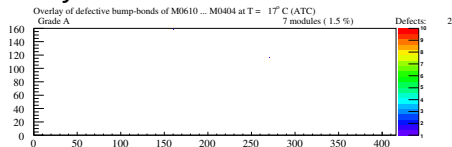
Grade C
(0 modules)



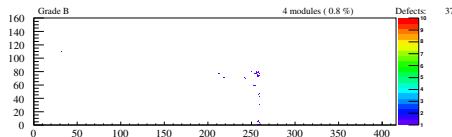
Defective bump-bonds $T = 17^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = +17^{\circ}\text{C}$ (ATC)

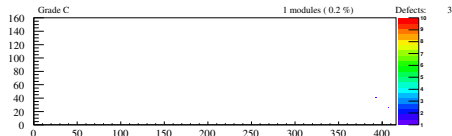
Grade A
(7 modules)



Grade B
(4 modules)



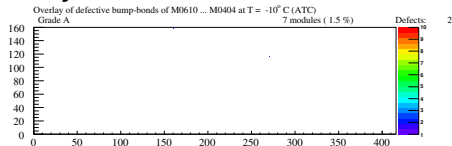
Grade C
(1 modules)



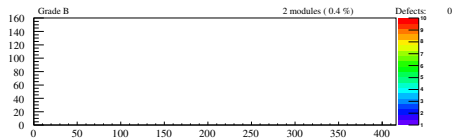
Defective bump-bonds $T = -10^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (ATC)

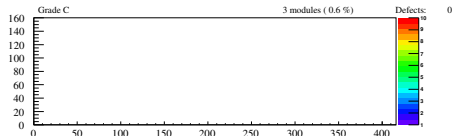
Grade A
(7 modules)



Grade B
(2 modules)



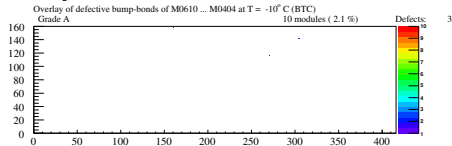
Grade C
(3 modules)



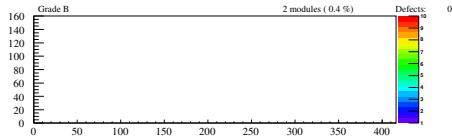
Defective bump-bonds $T = -10^{\circ}\text{C}$ (BTC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (BTC)

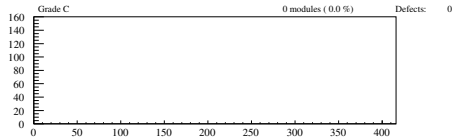
Grade A
(10 modules)



Grade B
(2 modules)



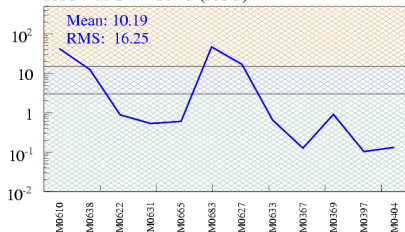
Grade C
(0 modules)



Current at 150 V

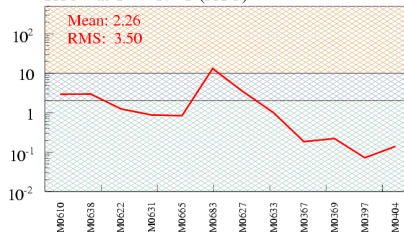
Current at 150 V (in μA) at $T = 17^\circ\text{C}$ and $T = -10^\circ\text{C}$

I150V at $T = -10^\circ\text{C}$ (ATC)



recalculated

I150V at $T = 17^\circ\text{C}$ (ATC)

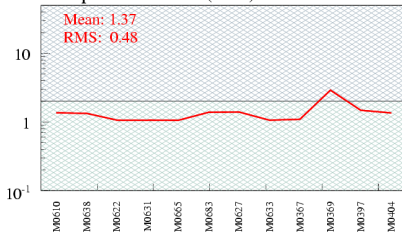


measured

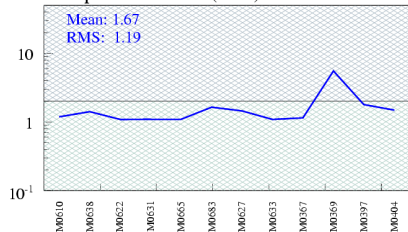
Slope of IV-Curve

Slope of IV-Curve at $T = 17^{\circ}\text{C}$ and $T = -10^{\circ}\text{C}$

IVslope at $T = 17^{\circ}\text{C}$ (ATC)

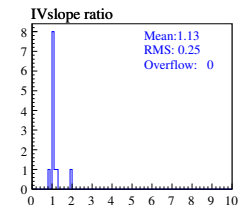
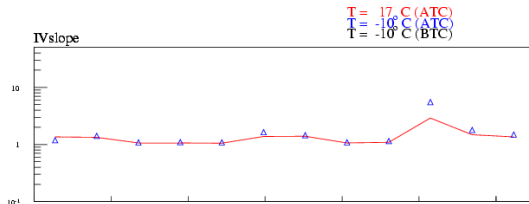
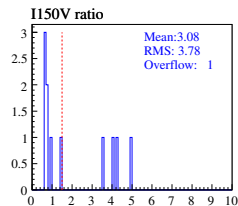
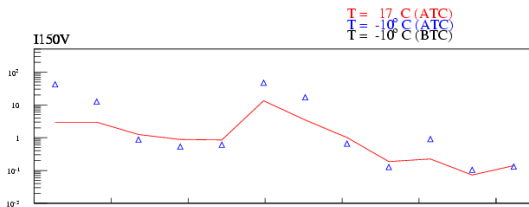


IVslope at $T = -10^{\circ}\text{C}$ (ATC)



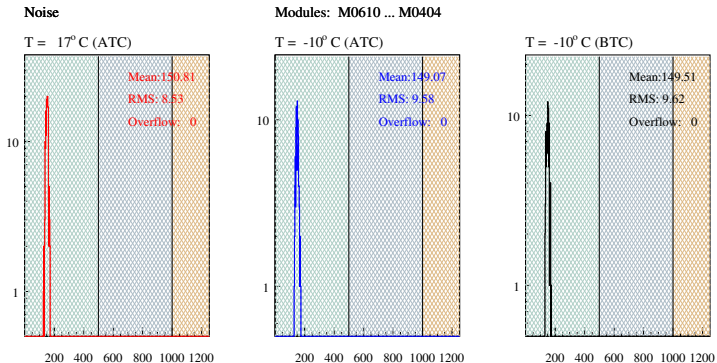
Current recalculation to $T = 17^{\circ}\text{C}$

Cross check of recalculated values with measured values



Noise

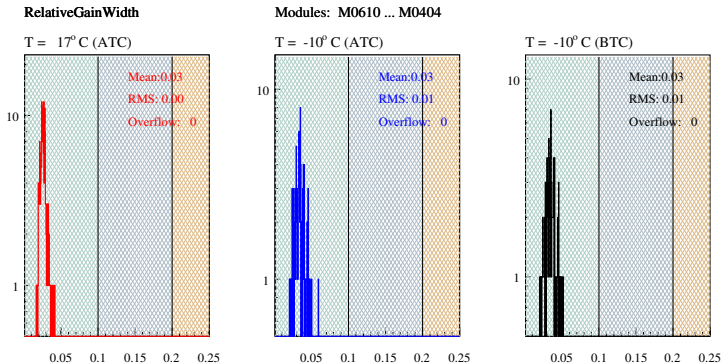
MeanNoise of chips



Noise in e^-

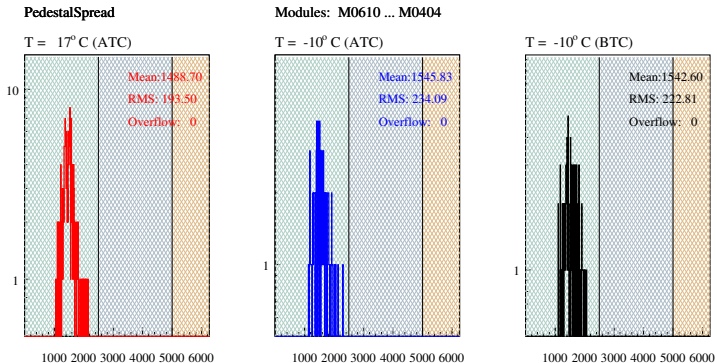
Relative Gain Width

RelativeGainWidth of chips



Pedestal Spread

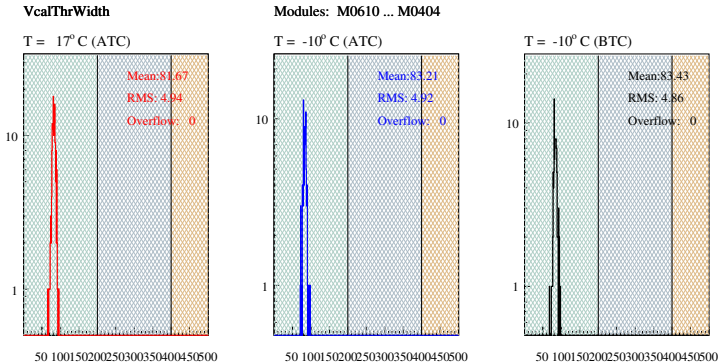
PedestalSpread of chips



Pedestal Spread in e^-

Vcal Threshold Width

VcalThresholdWidth of chips

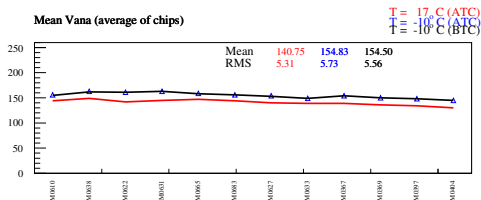


Vcal Thr. Width in e^-

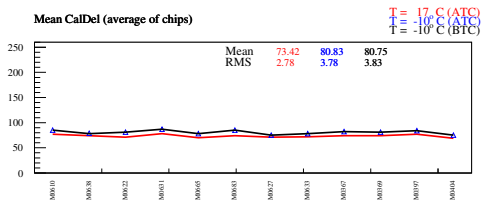
Operational parameters I

Mean DACs I

Mean Vana (average of chips)



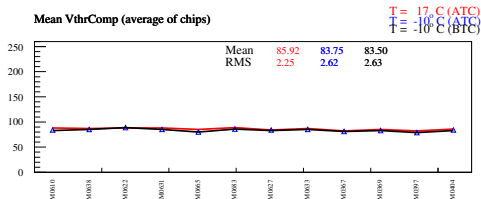
Mean CalDel (average of chips)



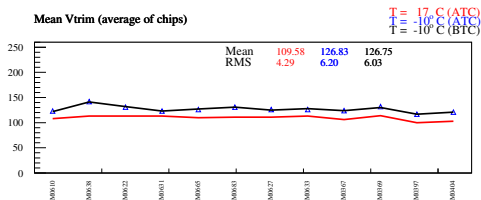
Operational parameters II

Mean DACs II

Mean VthrComp (average of chips)



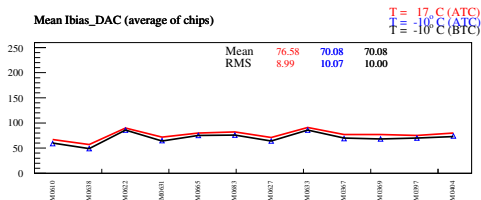
Mean Vtrim (average of chips)



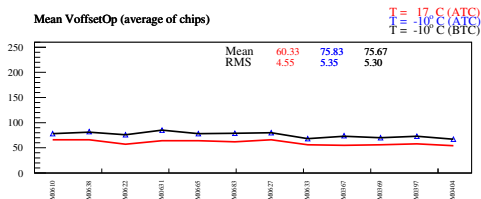
Operational parameters III

Mean DACs III

Mean Ibias_DAC (average of chips)

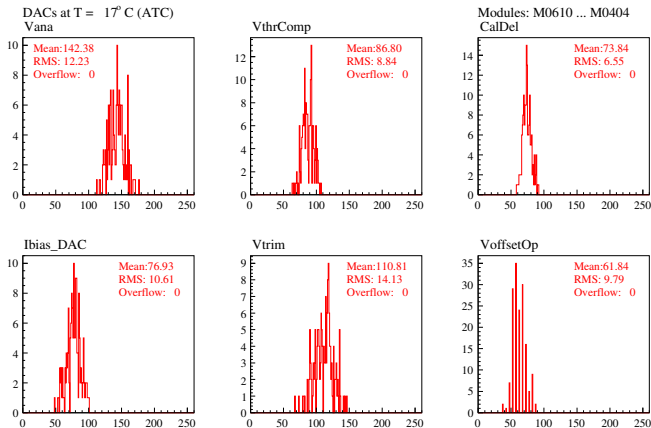


Mean VoffsetOp (average of chips)



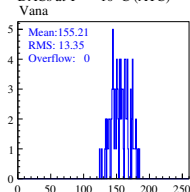
Operational parameters at $T = +17^{\circ}\text{C}$ (ATC)

DAC distribution (of chips)

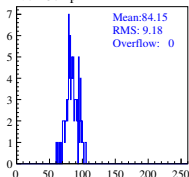


Operational parameters at $T = -10^{\circ}\text{C}$ (ATC)

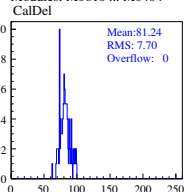
DAC distribution (of chips)

DACs at $T = -10^{\circ}\text{C}$ (ATC)

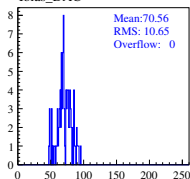
VthrComp



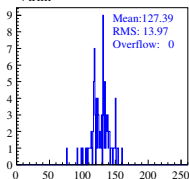
Modules: M0610 ... M0404



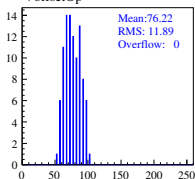
Ibias_DAC



Vtrim



VoffsetOp

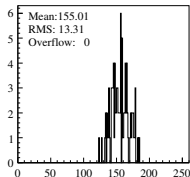


Operational parameters at $T = +17^{\circ}\text{C}$ (BTC)

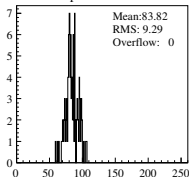
DAC distribution (of chips)

DACs at $T = -10^{\circ}\text{C}$ (BTC)

Vana

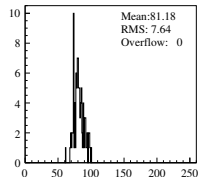


VthrComp

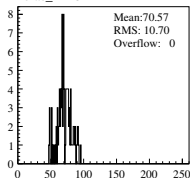


Modules: M0610 ... M0404

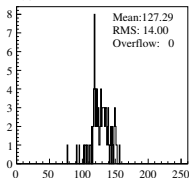
CalDel



Ibias_DAC



Vtrim



VoffsetOp

