BPIX Module Testing Status - Week 8

28th February 2007

Production overview

Production Status: 464 modules produced (415 / 49)

- 287/65 graded as A/B → 85% || 37/8 → 92%
- 63 graded as C → 15% || 4 → 8%

Module Testing Report of Week 8:

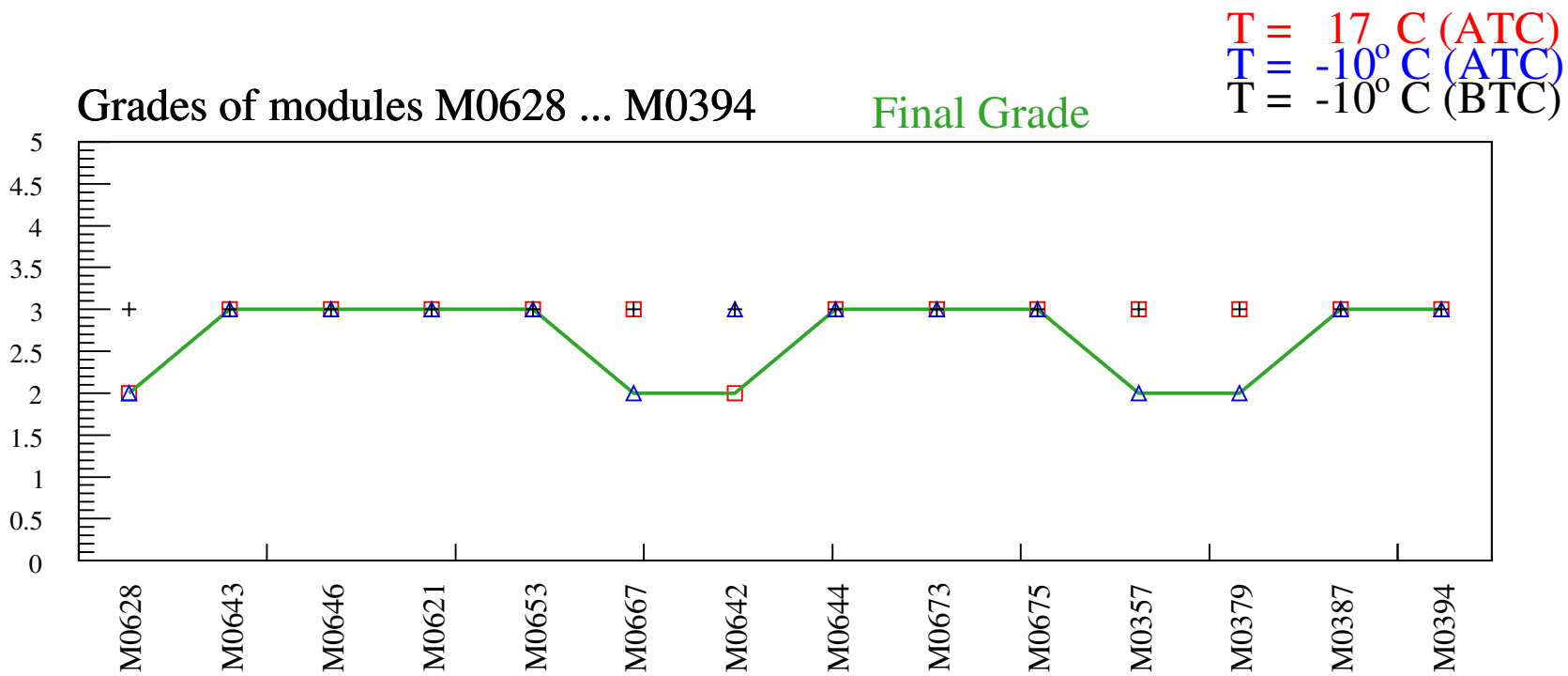
- 10/4 modules fully tested and therm. cycled (2 retested)

	Modules			*Half-Modules*		
Grade	**A**	**B**	**C**	**A**	**B**	**C**
T = -10^o C, BTC*	10	0	0	4	0	0
T = -10^o C, ATC	8	2	0	2	2	0
T = $+17^o$ C, ATC	8	2	0	4	0	0
Final Grade	7	3	0	2	2	0

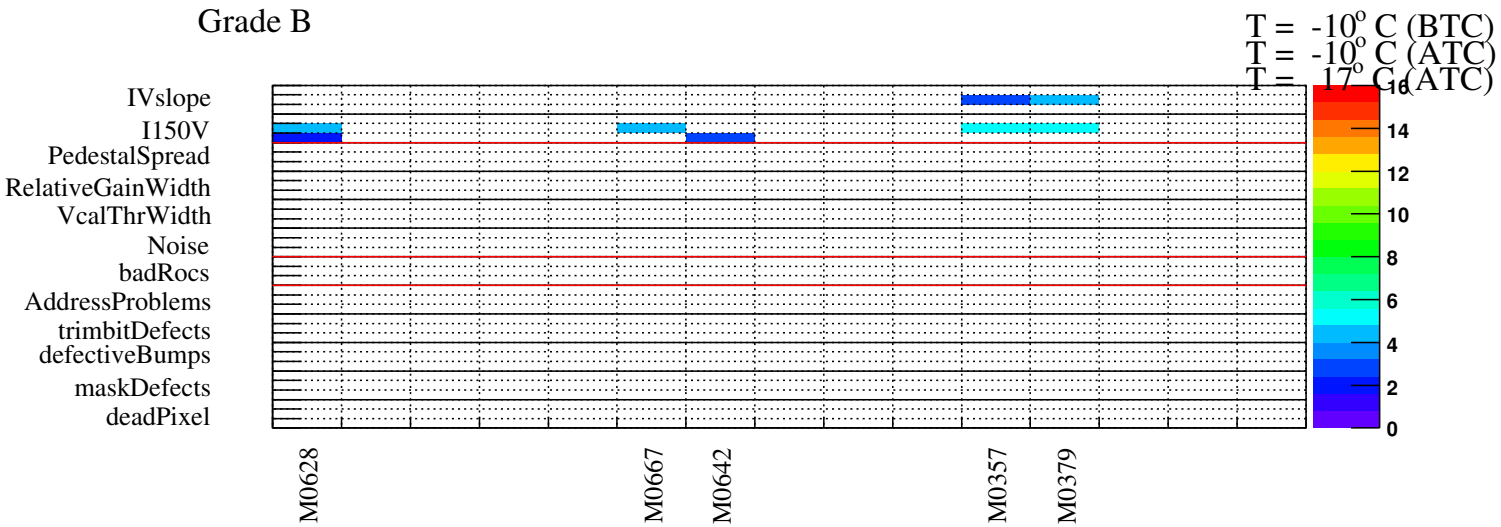
- 1 were retested with new DAC settings (nothing changed)

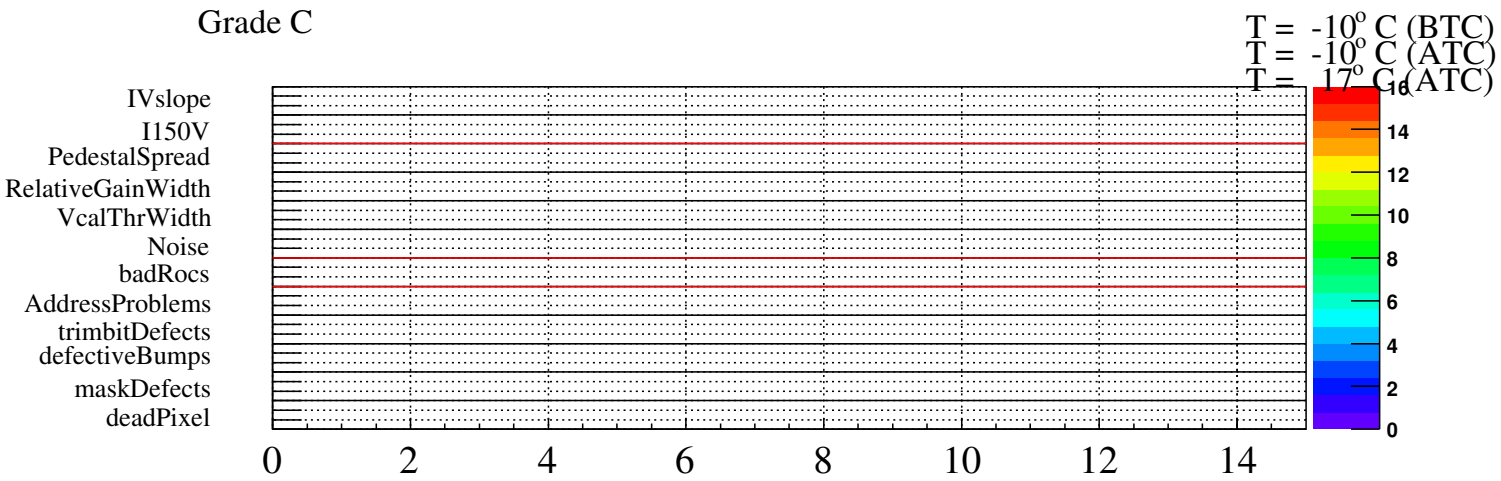
*without IV-criteria

Production summary



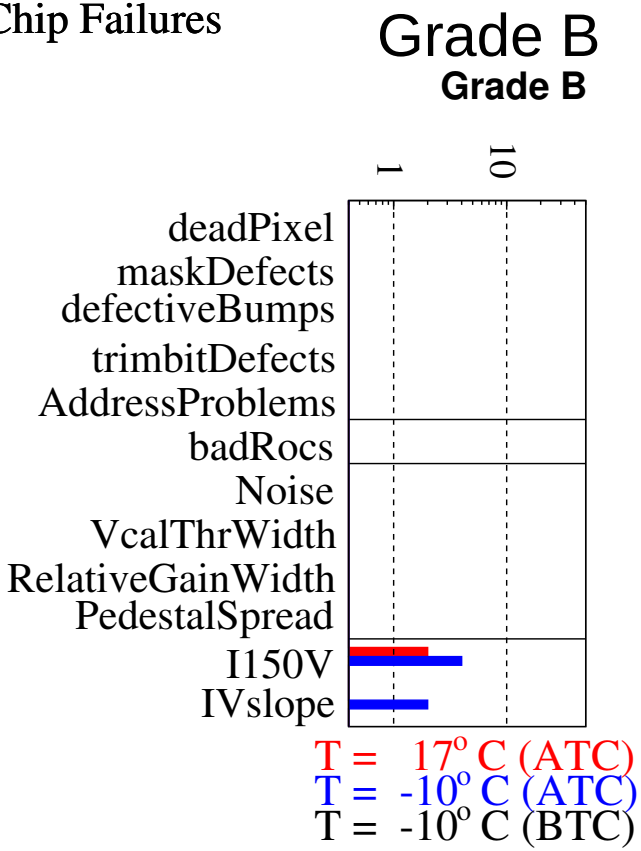
Module Failures Overview

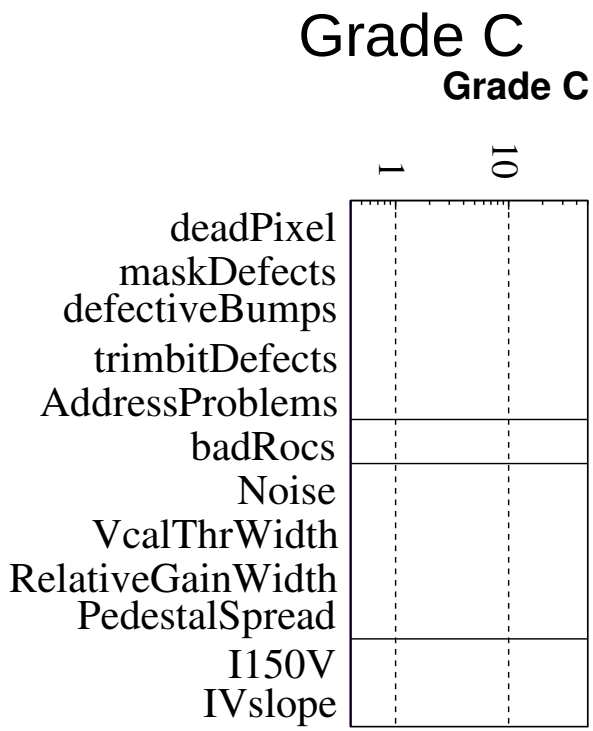




Production quality

Chip Failures





← Pixel defects

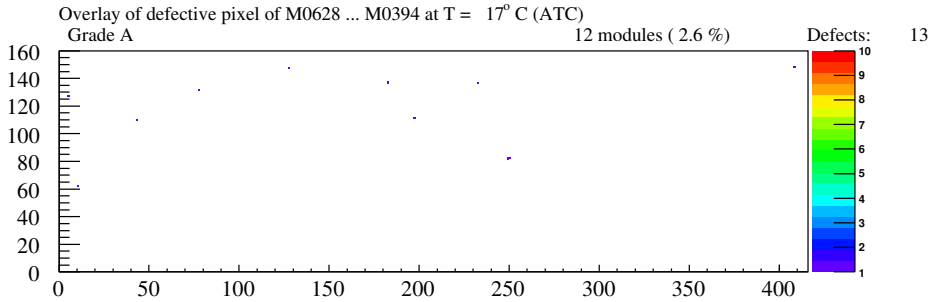
← Chip performance

← Module IV

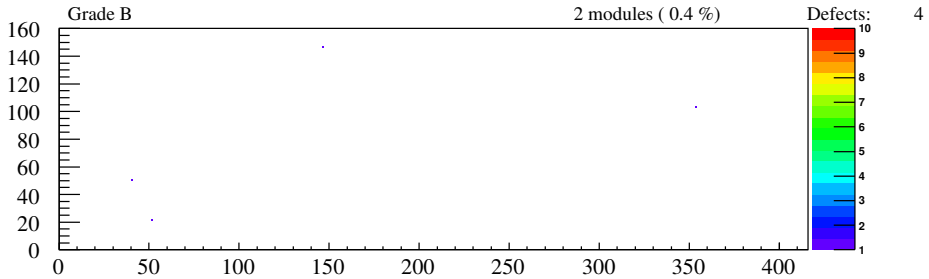
Defective pixel $T = 17^{o}C$ (ATC)

Overlay of all fully tested modules at T = $+17^{o}$ C (ATC)

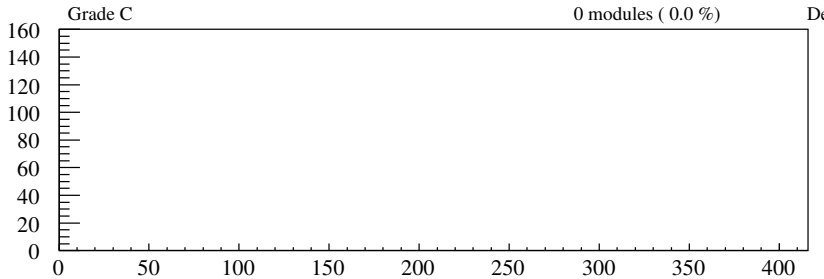
Grade A
(12 modules)



Grade B
(2 modules)



Grade C
(0 modules)



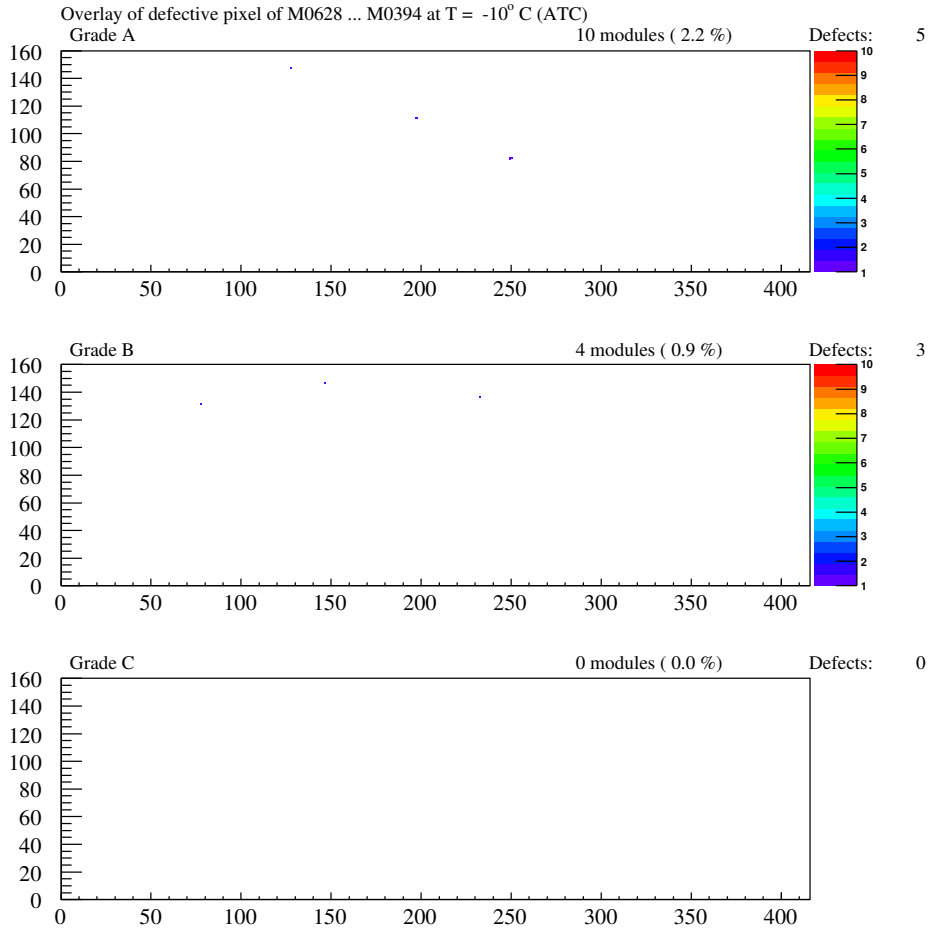
Defective pixel $T = -10^{o}C$ (ATC)

Overlay of all fully tested modules at T = -10^{o} C (ATC)

Grade A
(10 modules)

Grade B
(4 modules)

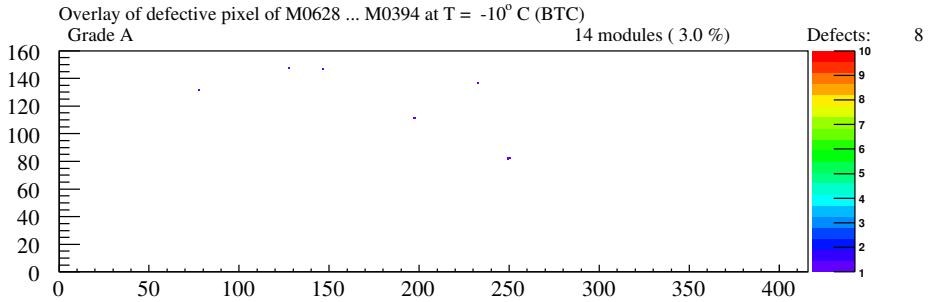
Grade C
(0 modules)



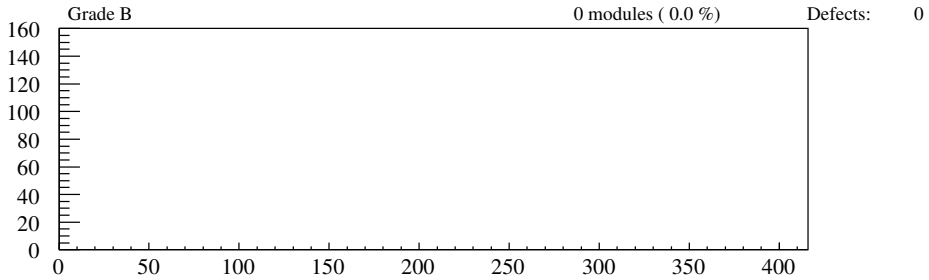
Defective pixel $T = -10^oC$ (BTC)

Overlay of all fully tested modules at T = -10^o C (BTC)

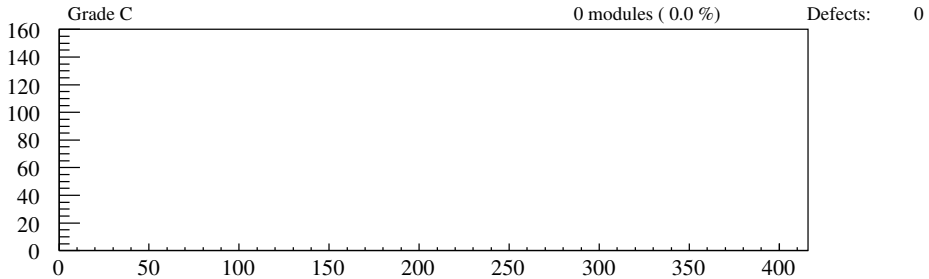
Grade A
(14 modules)



Grade B
(0 modules)



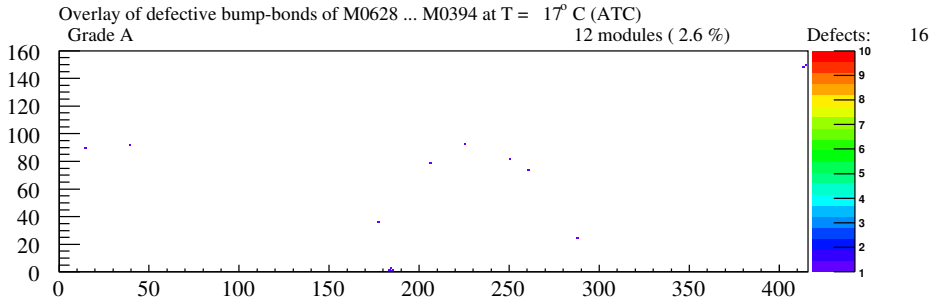
Grade C
(0 modules)



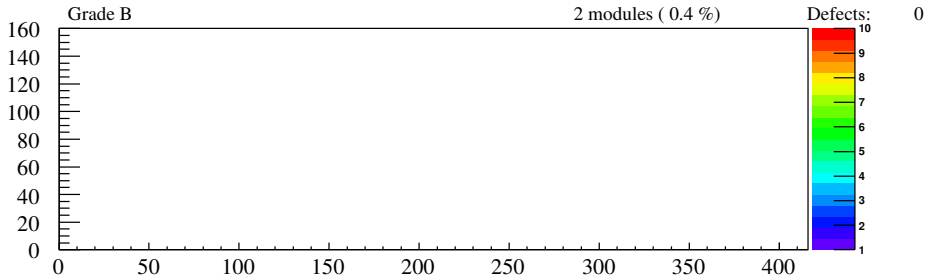
Defective bump-bonds $T = 17^{o}C$ (ATC)

Overlay of all fully tested modules at T = $+17^{o}$ C (ATC)

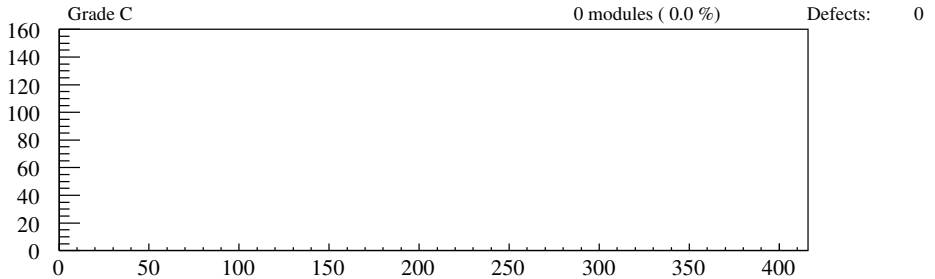
Grade A
(12 modules)



Grade B
(2 modules)



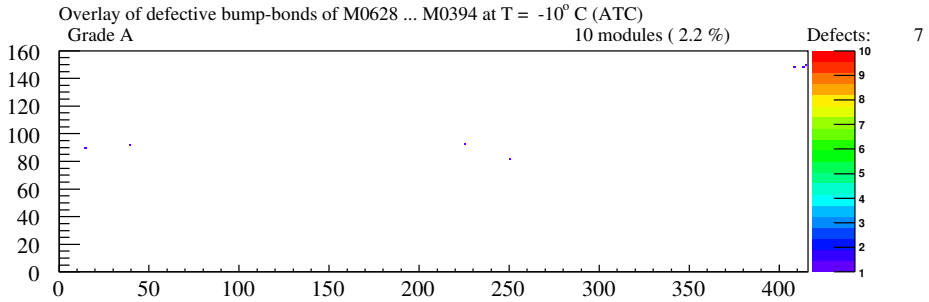
Grade C
(0 modules)



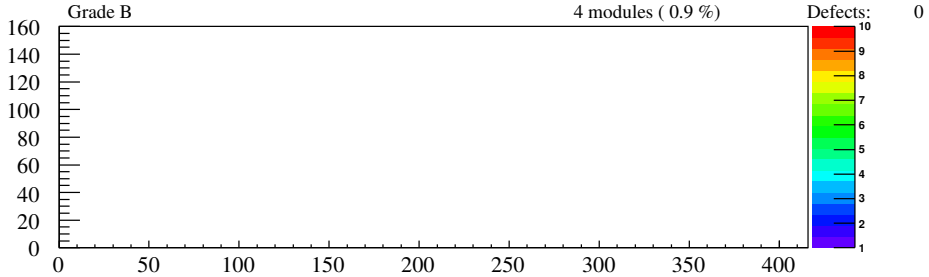
Defective bump-bonds $T = -10^{o}C$ (ATC)

Overlay of all fully tested modules at T = -10^{o} C (ATC)

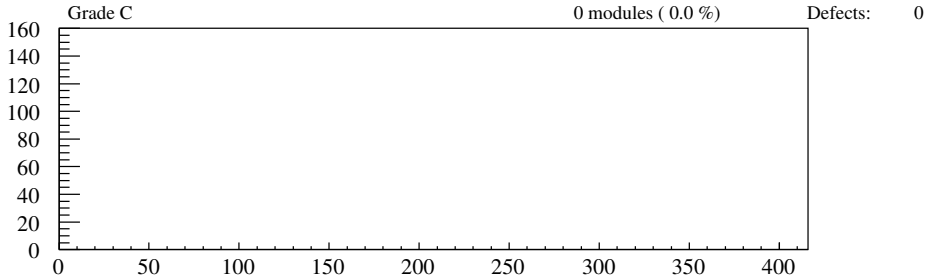
Grade A
(10 modules)



Grade B
(4 modules)



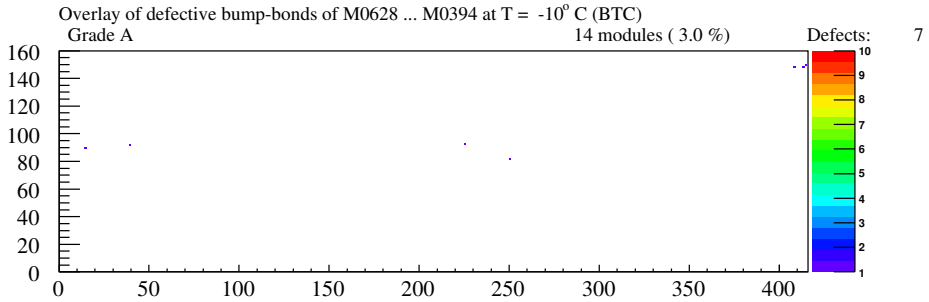
Grade C
(0 modules)



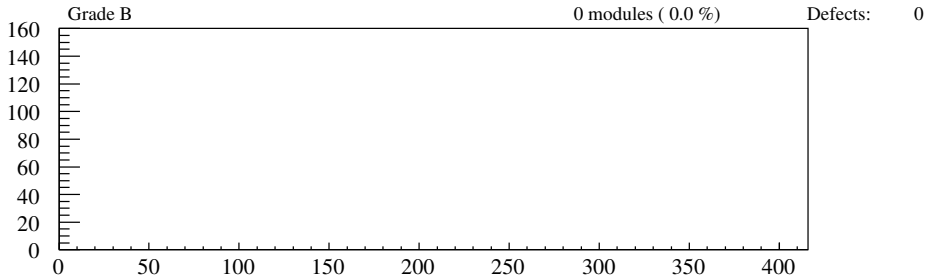
Defective bump-bonds $T = -10^{o}C$ (BTC)

Overlay of all fully tested modules at T = -10^{o} C (BTC)

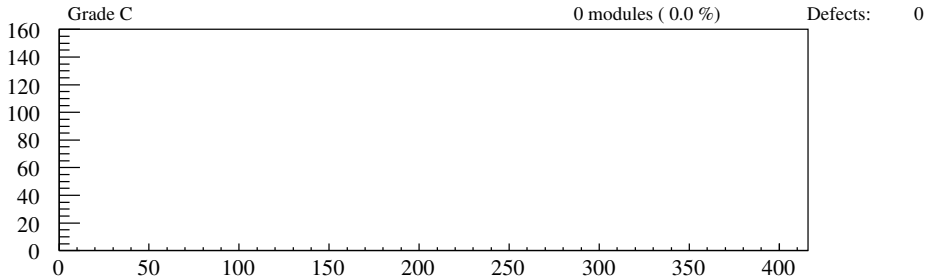
Grade A
(14 modules)



Grade B
(0 modules)

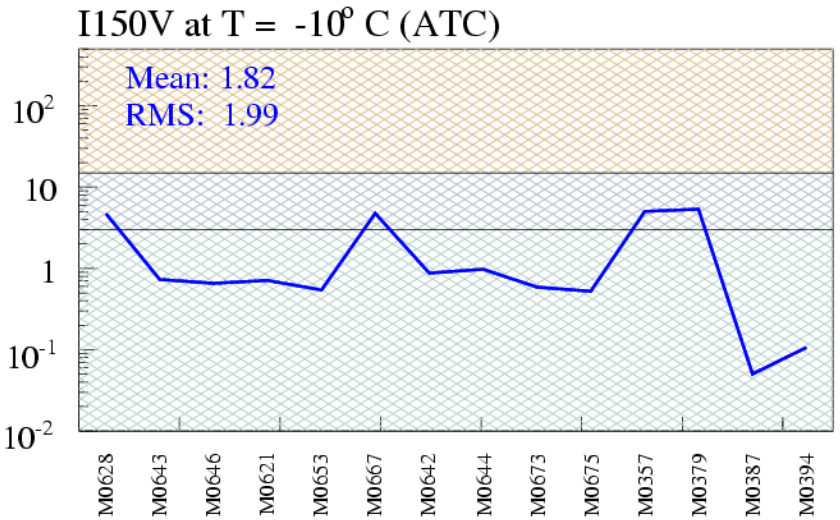


Grade C
(0 modules)

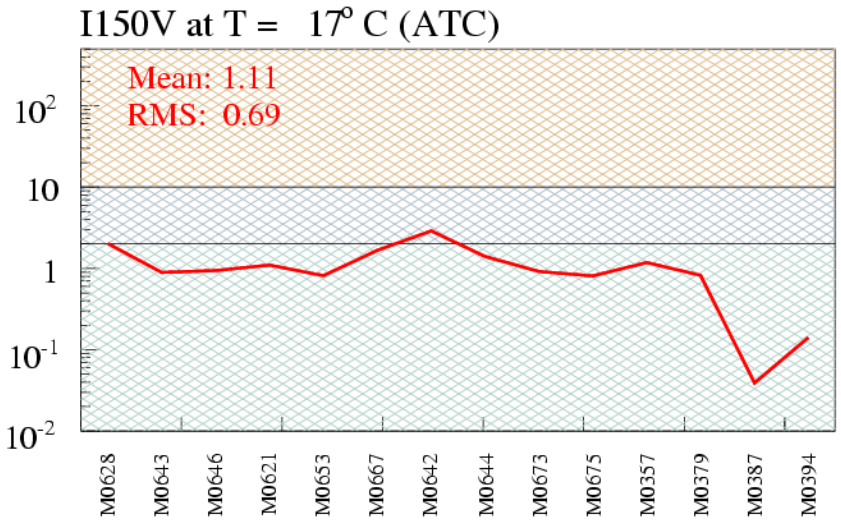


Current at 150 V

Current at 150 V (in μA) at $T = 17^oC$ and $T = -10^oC$



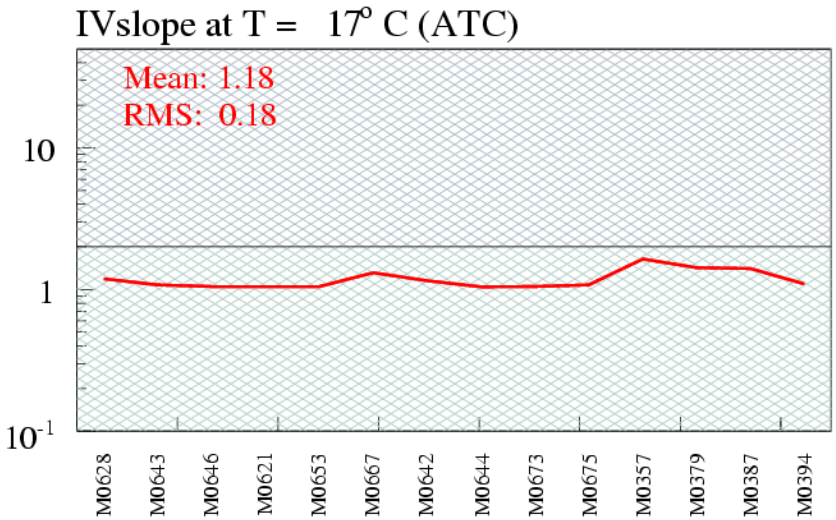
recalculated

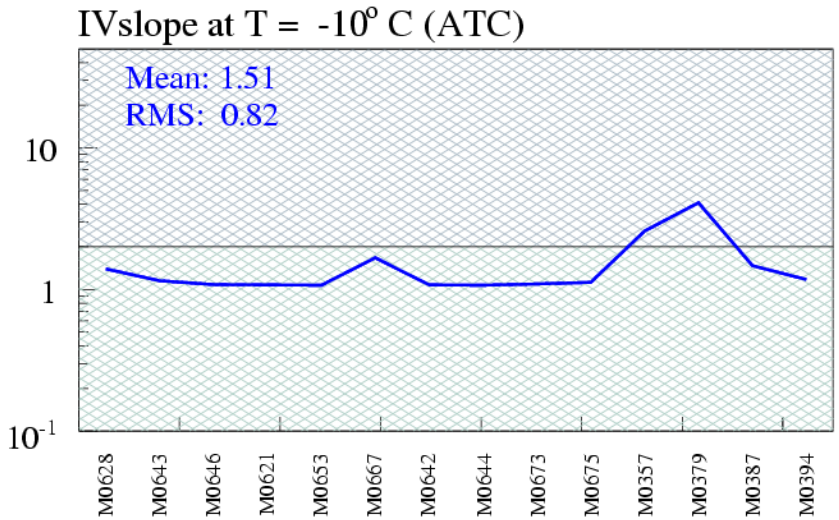


measured

Slope of IV-Curve

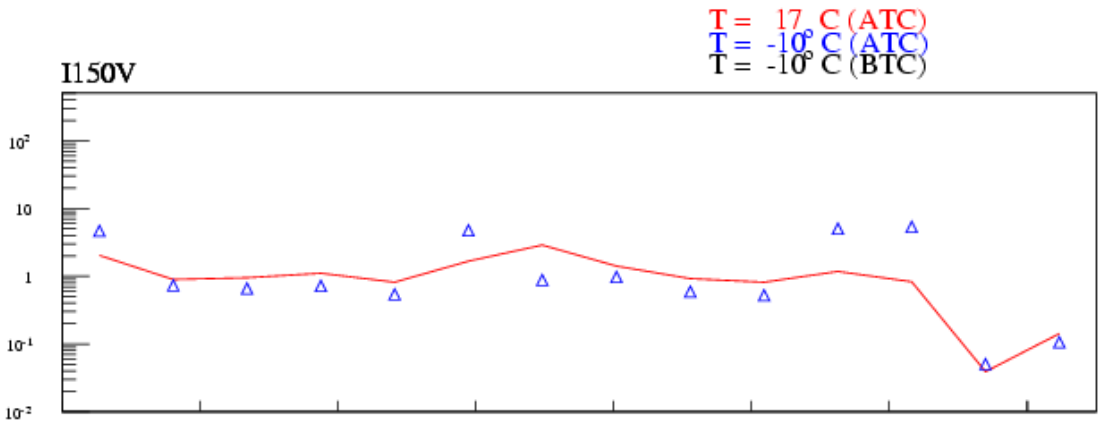
Slope of IV-Curveat $T = 17^oC$ and $T = -10^oC$

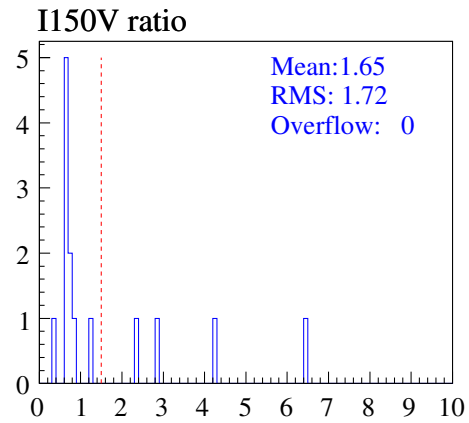


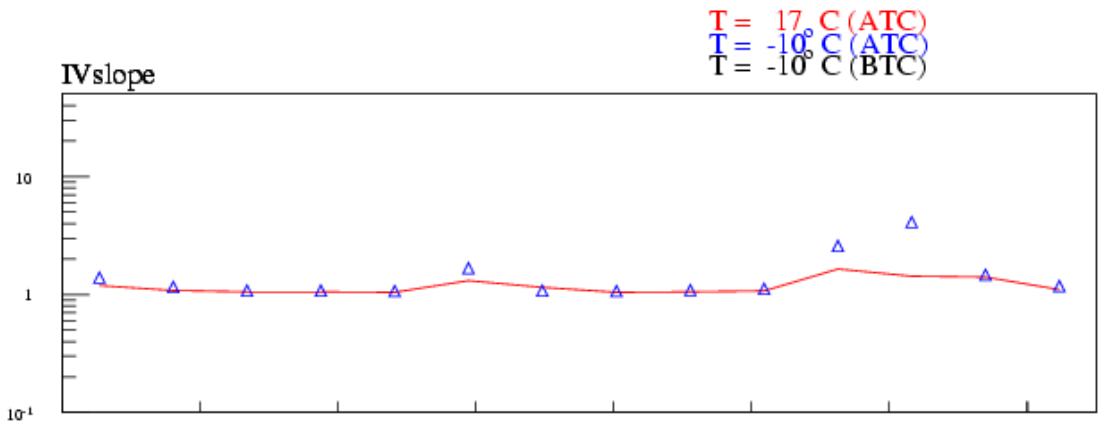


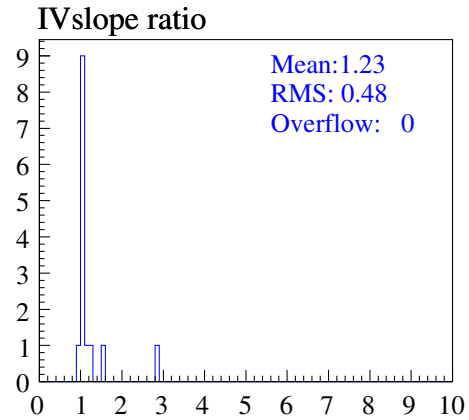
Current recalculation to $T = 17^oC$

Cross check of recalculated values with measured values



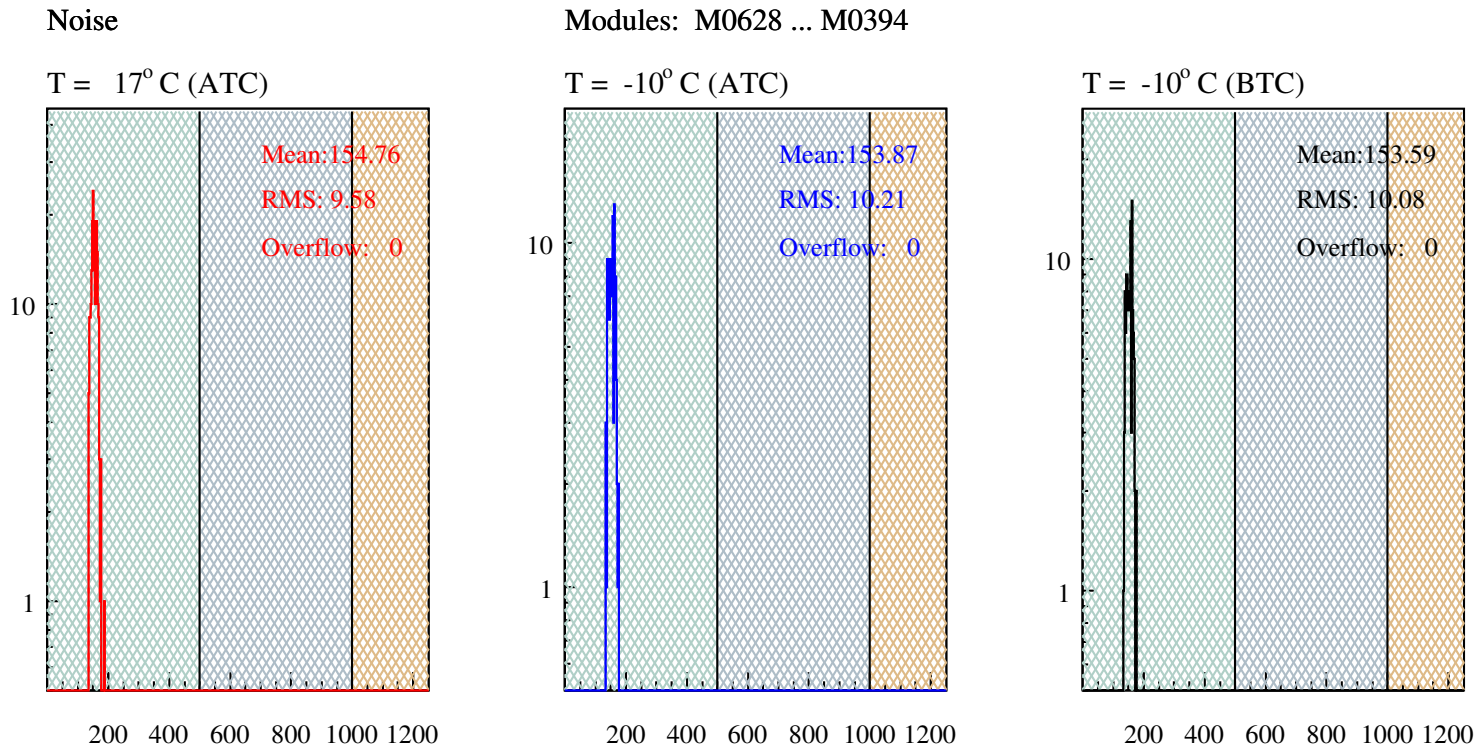






Noise

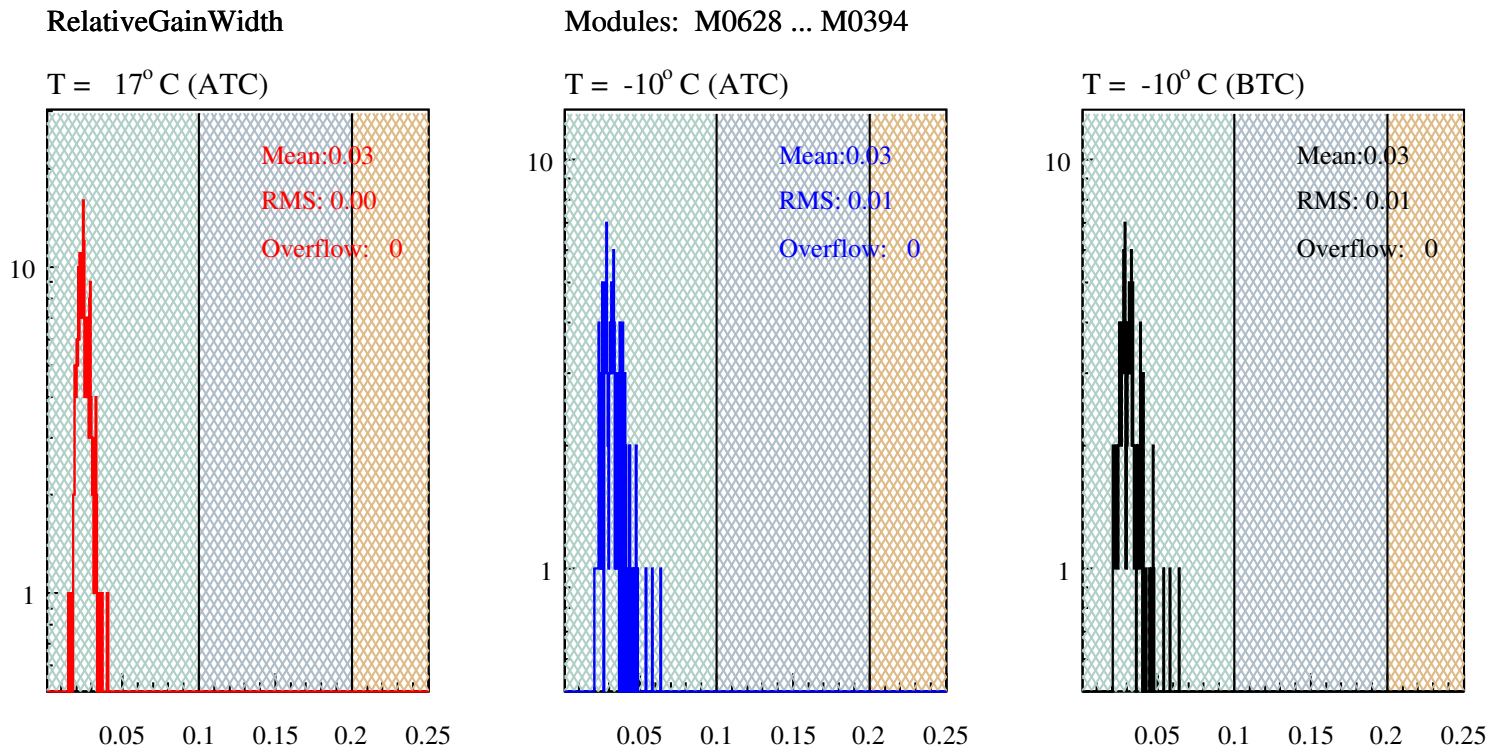
MeanNoise of chips



Noise in e^-

Relative Gain Width

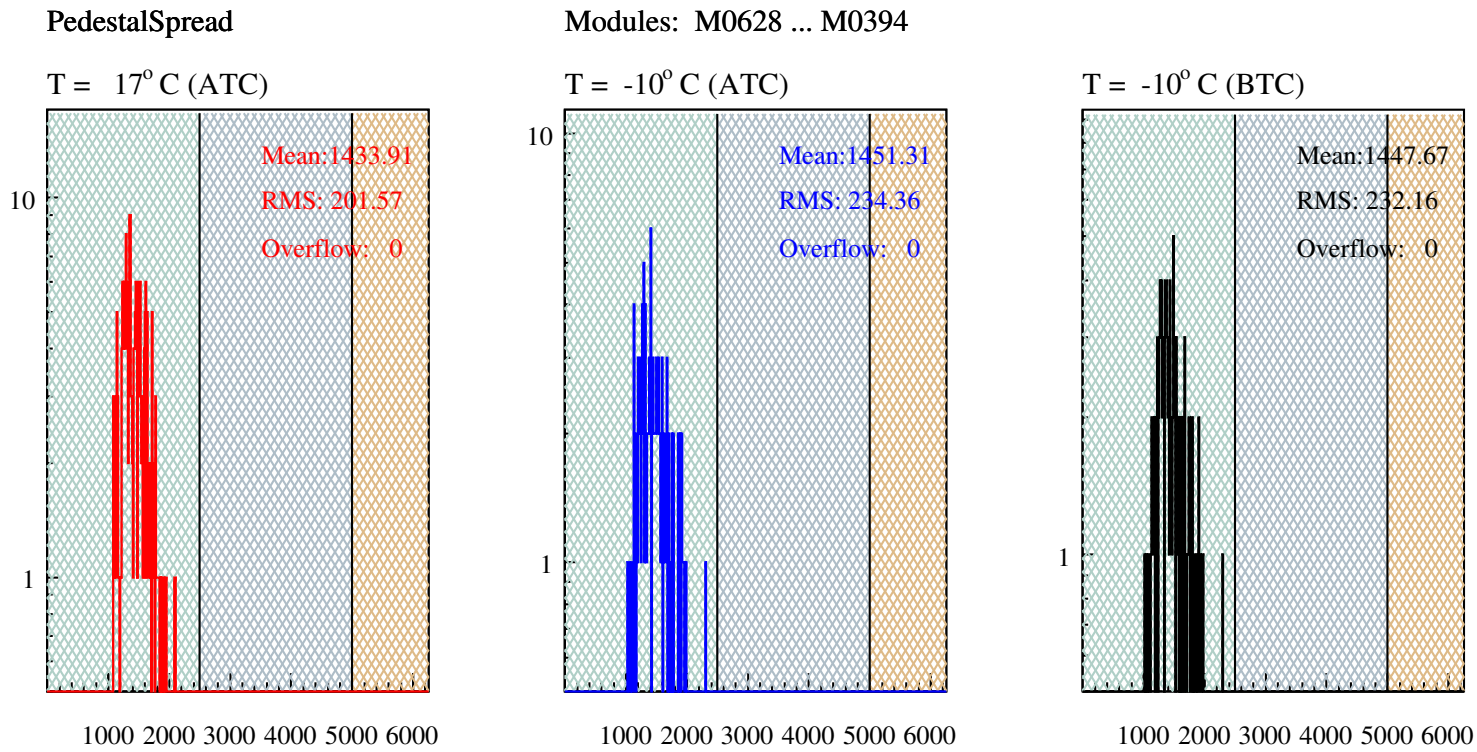
RelativeGainWidth of chips



Rel. Gain Width in %

Pedestal Spread

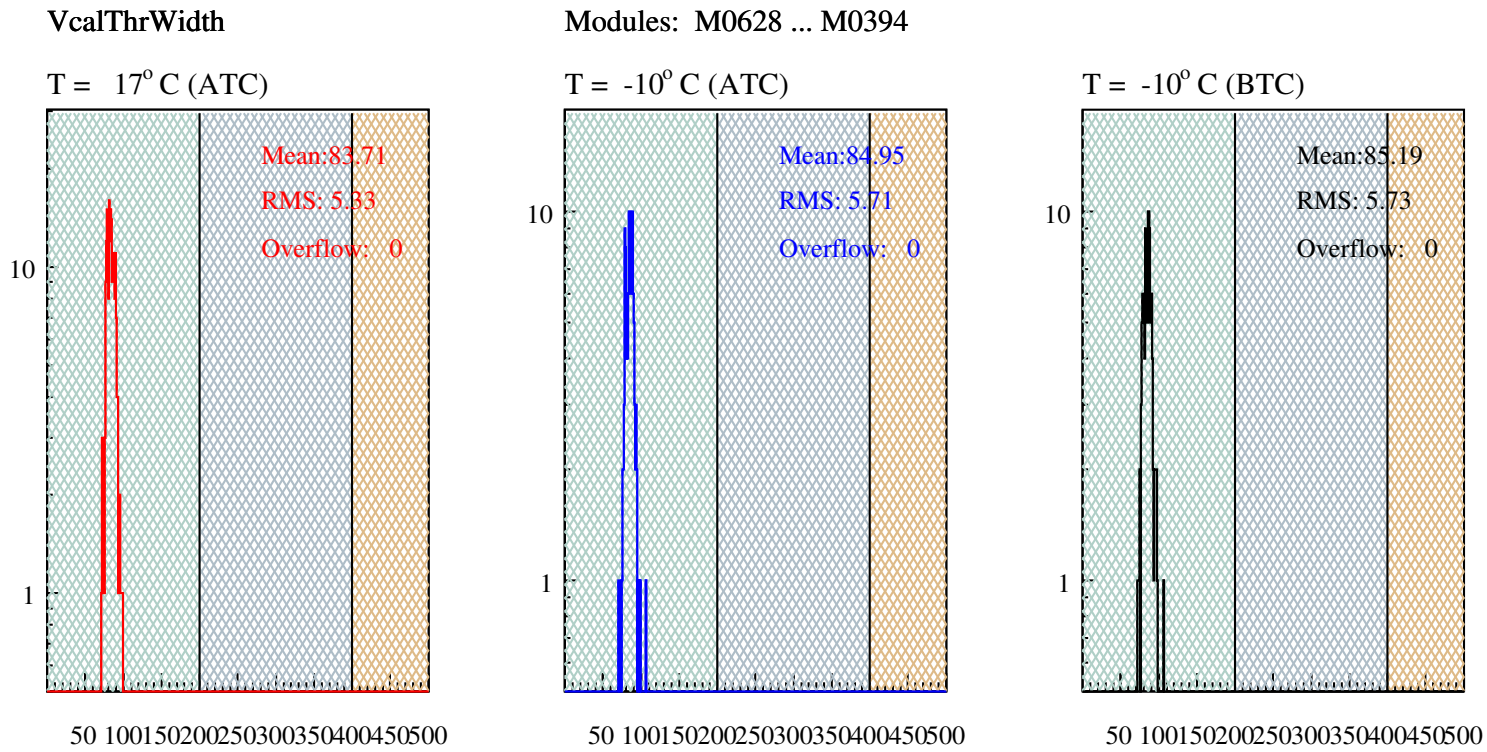
PedestalSpread of chips



Pedestal Spread in e^-

Vcal Threshold Width

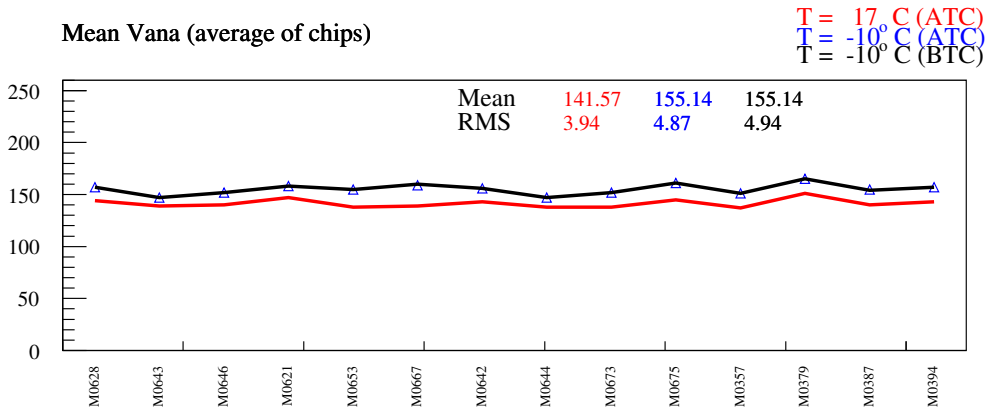
VcalThresholdWidth of chips

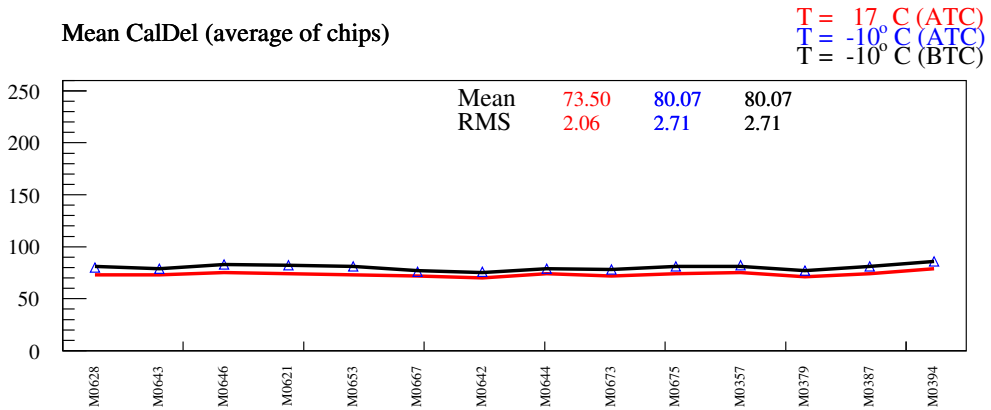


Vcal Thr. Width in e^-

Operational parameters I

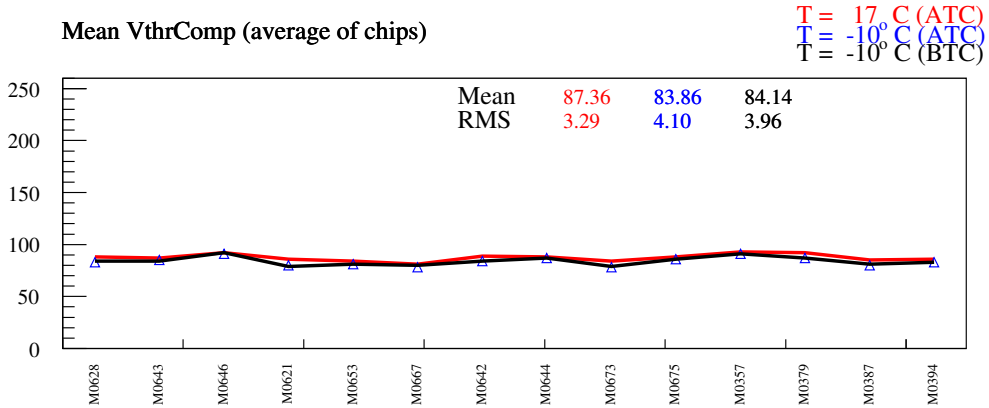
Mean DACs I

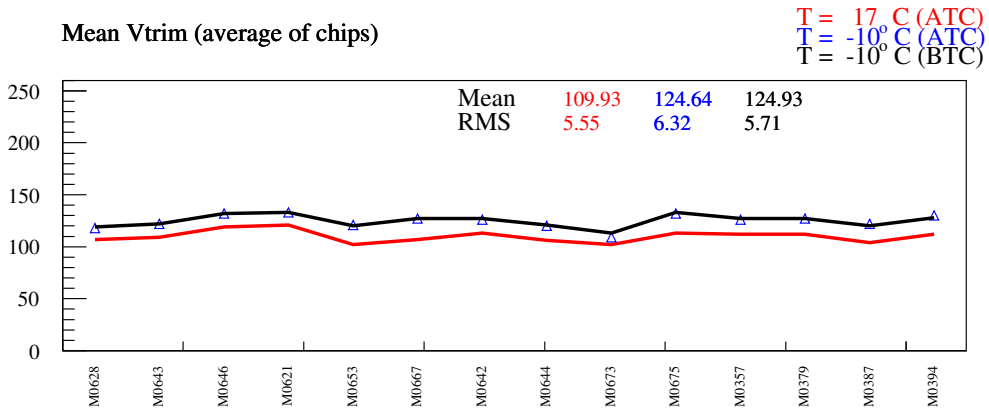




Operational parameters II

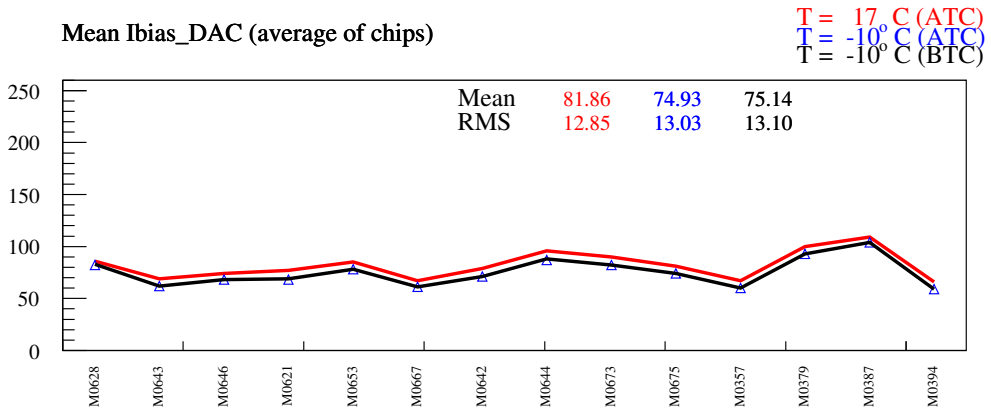
Mean DACs II

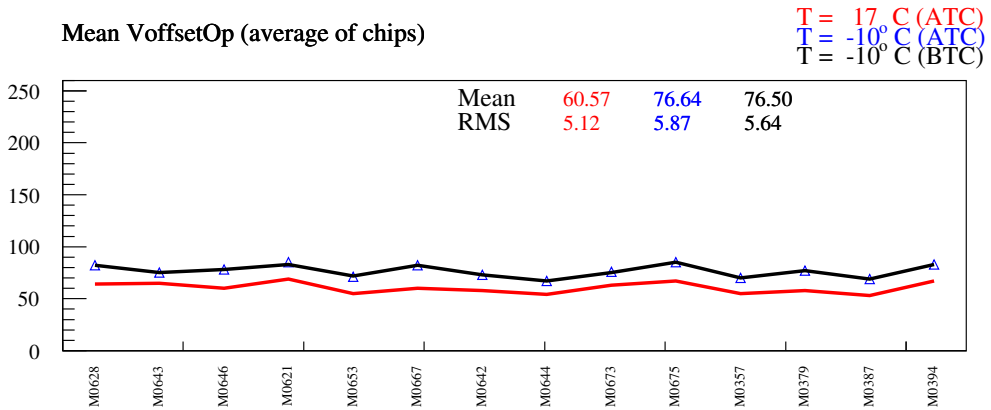




Operational parameters III

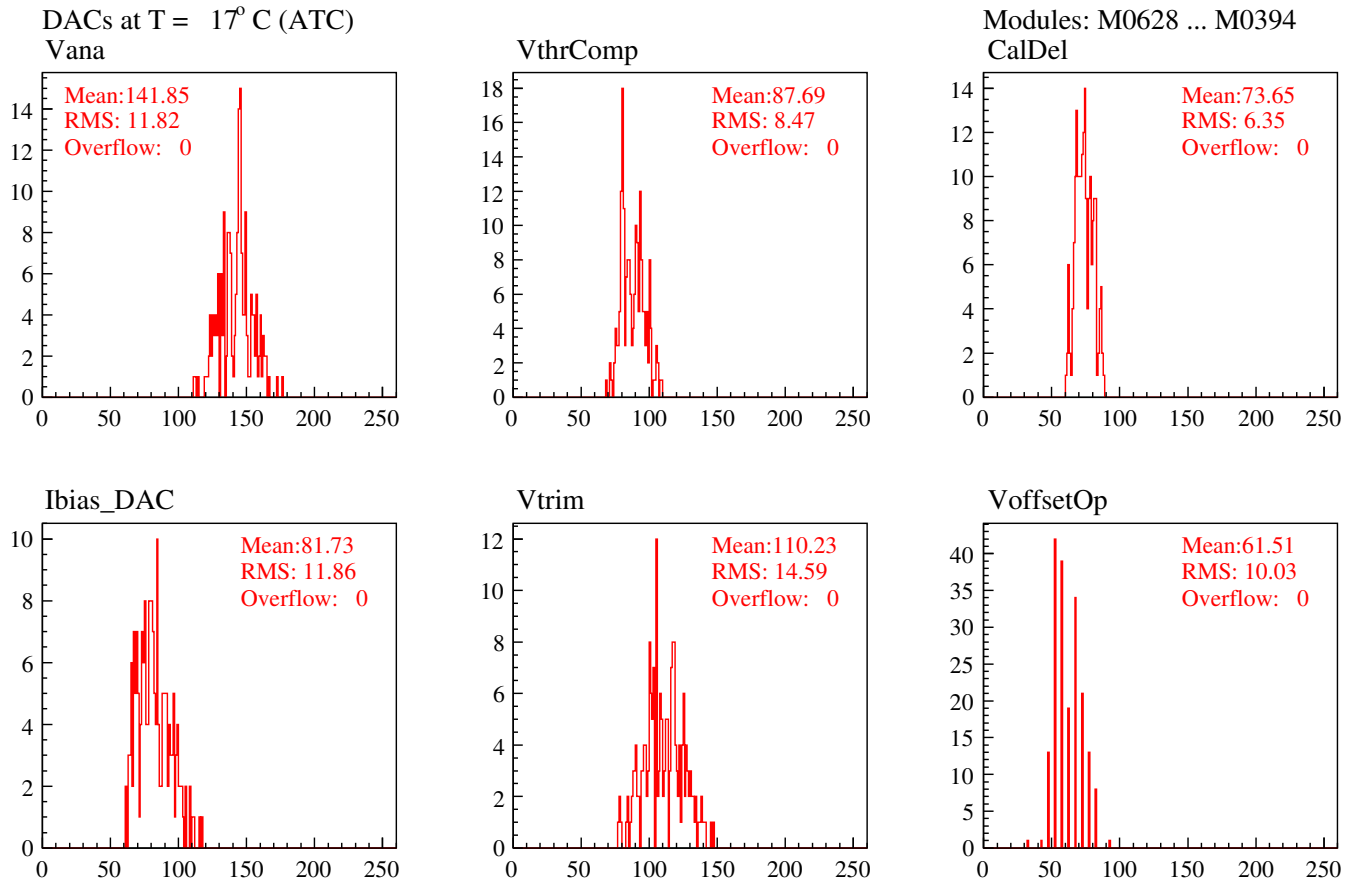
Mean DACs III





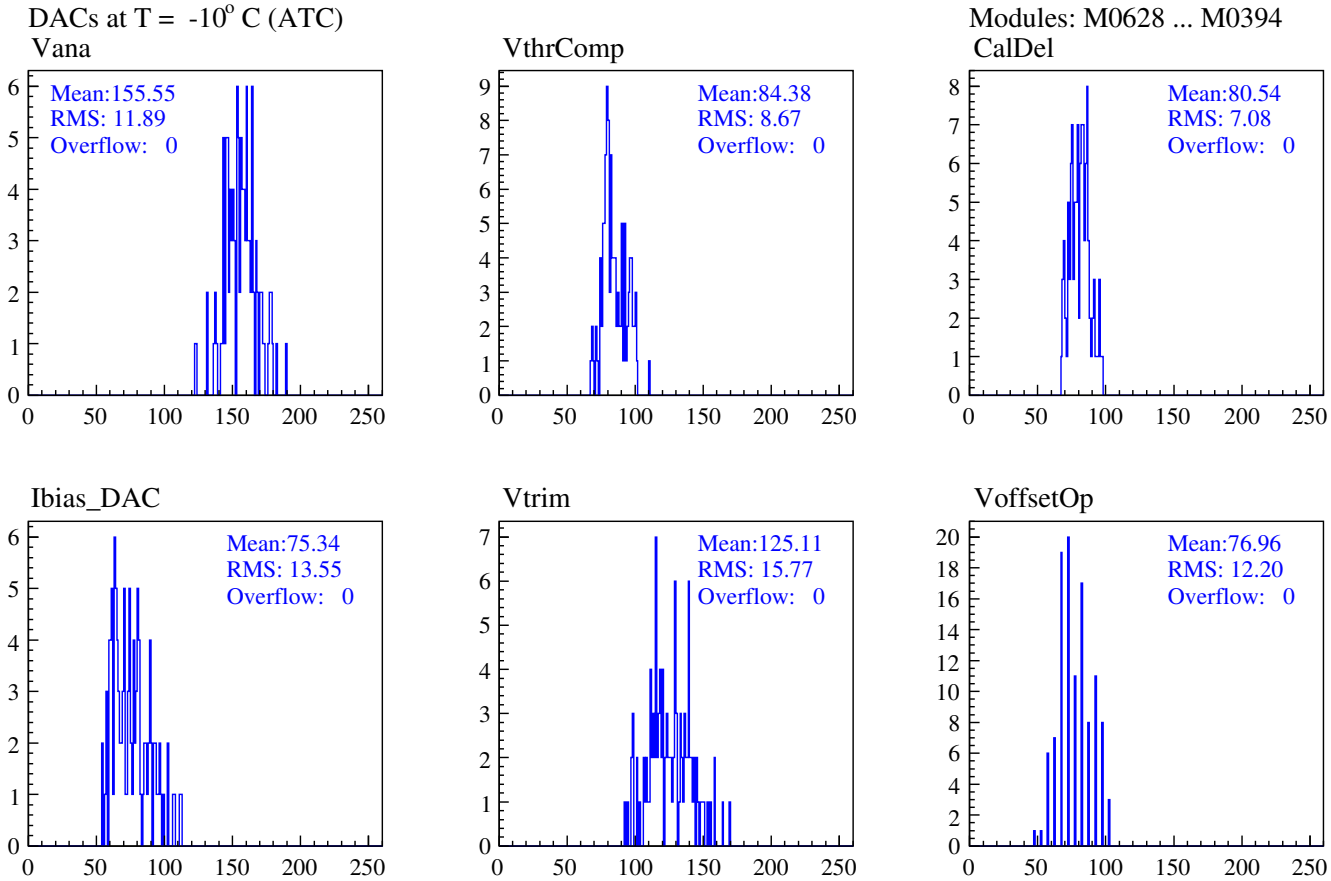
Operational parameters at $T = +17^{o}C$ (ATC)

DAC distribution (of chips)



Operational parameters at $T = -10^oC$ (ATC)

DAC distribution (of chips)



Operational parameters at $T = +17^{o}C$ (BTC)

DAC distribution (of chips)