

BPIX Module Testing Status - Week 49

10th January 2007

Production Status: 283 modules produced (275 / 8)

- 197/36 graded as A/B → 82%
- 50 graded as C → 18%

Module Testing Report of Week 49:

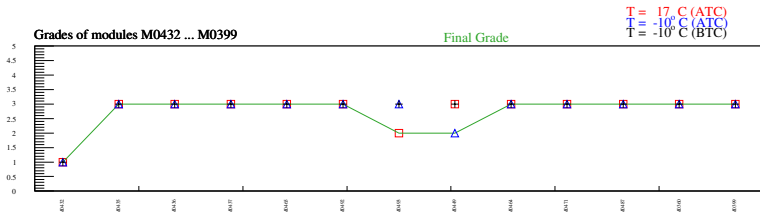
- 11/2 modules fully tested and therm. cycled (0 retested)

	Modules			Half-Modules		
Grade	A	B	C	A	B	C
T = -10° C, BTC*	10	0	1	2	0	0
T = -10° C, ATC	9	1	1	2	0	0
T = $+17^{\circ}$ C, ATC	9	1	1	2	0	0
Final Grade	8	2	1	2	0	0

- no retests with new DAC settings

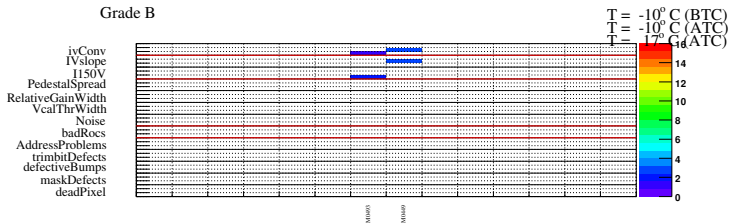
*without IV-criteria

Production summary

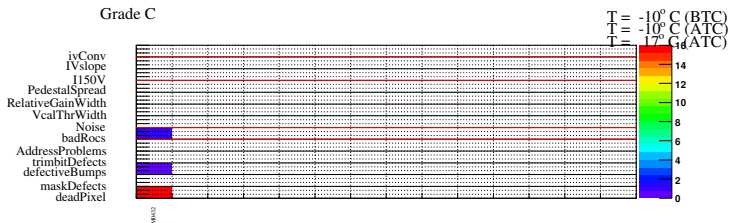


Module Failures Overview

Grade B

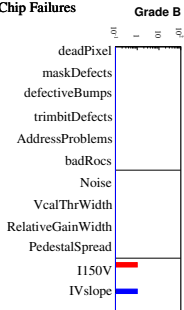


Grade C



Grade B

Chip Failures

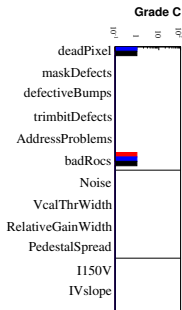


T = 17° C (ATC)

T = -10° C (ATC)

T = -10° C (BTC)

Grade C Failures



← Pixel defects

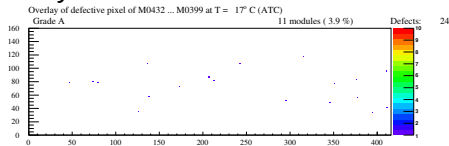
← Chip performance

← Module IV

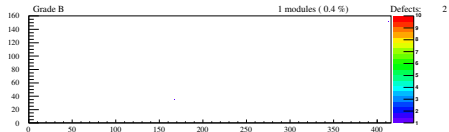
Defective pixel $T = 17^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = +17^{\circ}\text{C}$ (ATC)

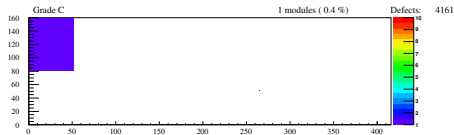
Grade A
(11 modules)



Grade B
(1 modules)



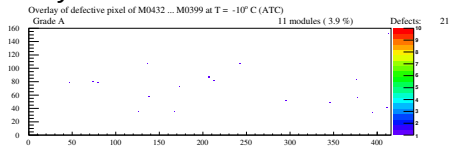
Grade C
(1 modules)



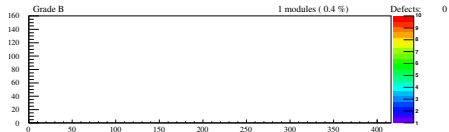
Defective pixel $T = -10^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (ATC)

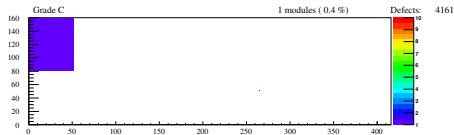
Grade A
(11 modules)



Grade B
(1 modules)



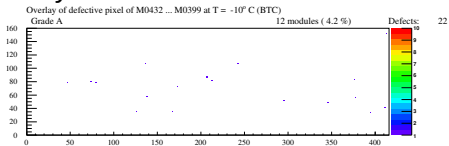
Grade C
(1 modules)



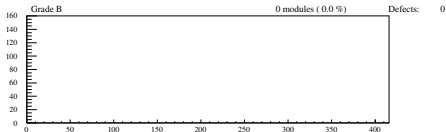
Defective pixel $T = -10^{\circ}\text{C}$ (BTC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (BTC)

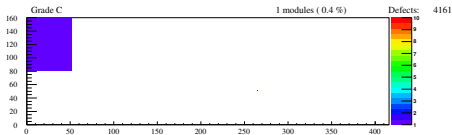
Grade A
(12 modules)



Grade B
(0 modules)



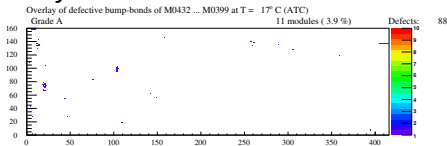
Grade C
(1 modules)



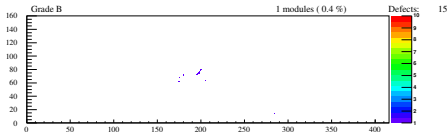
Defective bump-bonds $T = 17^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = +17^{\circ}\text{C}$ (ATC)

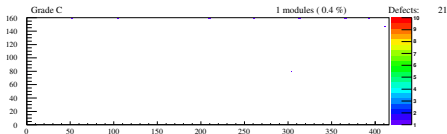
Grade A
(11 modules)



Grade B
(1 modules)



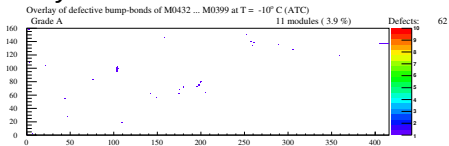
Grade C
(1 modules)



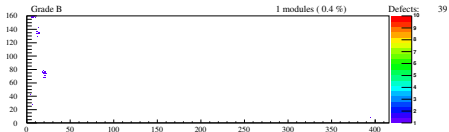
Defective bump-bonds $T = -10^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (ATC)

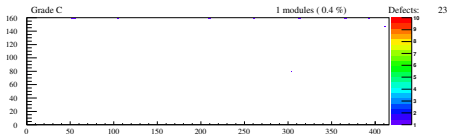
Grade A
(11 modules)



Grade B
(1 modules)



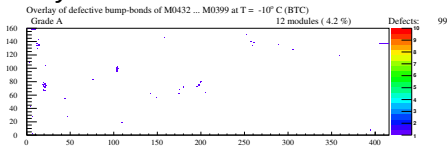
Grade C
(1 modules)



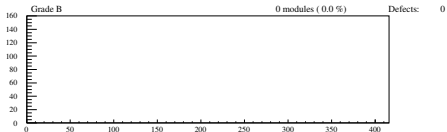
Defective bump-bonds $T = -10^{\circ}\text{C}$ (BTC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (BTC)

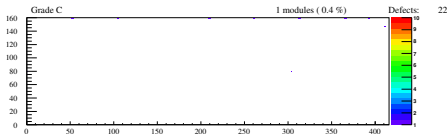
Grade A
(12 modules)



Grade B
(0 modules)



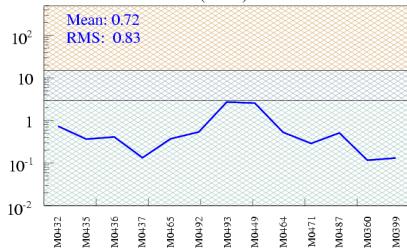
Grade C
(1 modules)



Current at 150 V

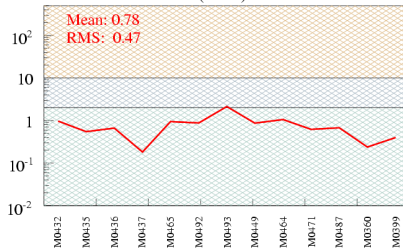
Current at 150 V (in μA) at $T = 17^\circ\text{C}$ and $T = -10^\circ\text{C}$

I150V at $T = -10^\circ\text{C}$ (ATC)



recalculated

I150V at $T = 17^\circ\text{C}$ (ATC)

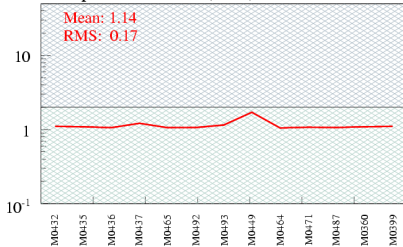


measured

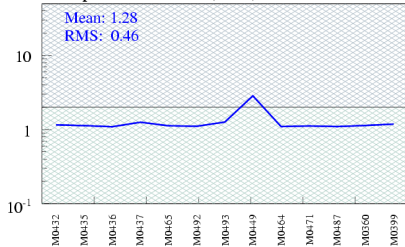
Slope of IV-Curve

Slope of IV-Curve at $T = 17^{\circ}\text{C}$ and $T = -10^{\circ}\text{C}$

IVslope at $T = 17^{\circ}\text{C}$ (ATC)

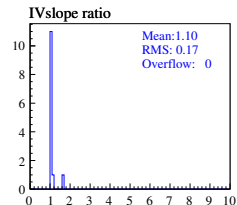
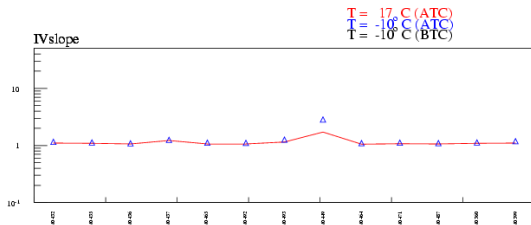
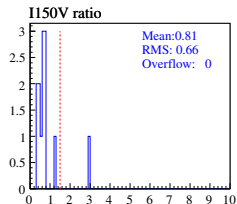
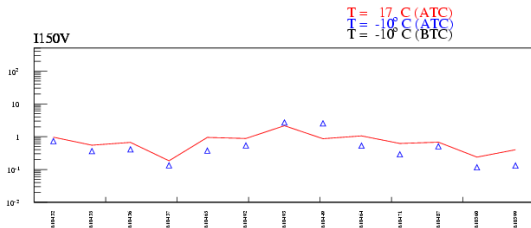


IVslope at $T = -10^{\circ}\text{C}$ (ATC)

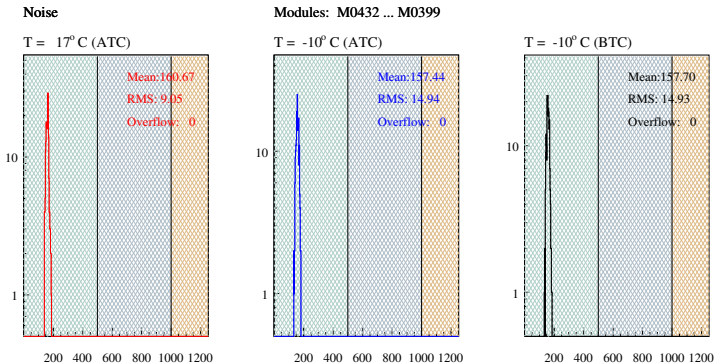


Current recalculation to $T = 17^{\circ}\text{C}$

Cross check of recalculated values with measured values

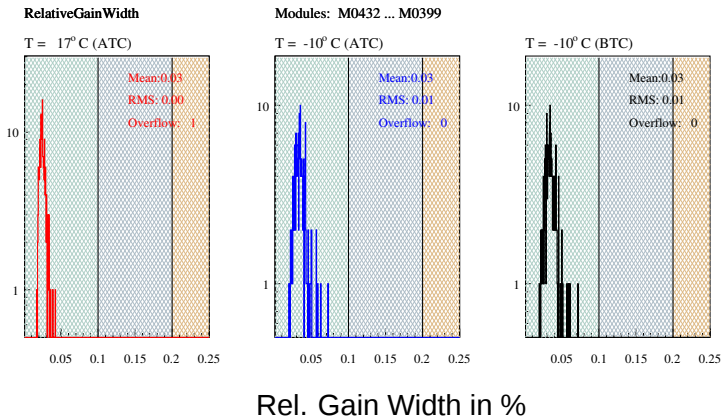


MeanNoise of chips

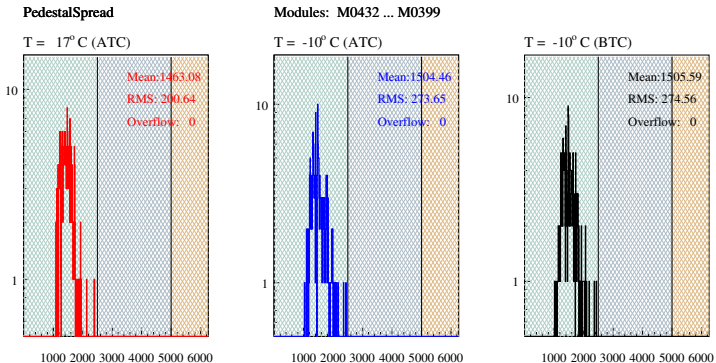


Noise in e^-

RelativeGainWidth of chips



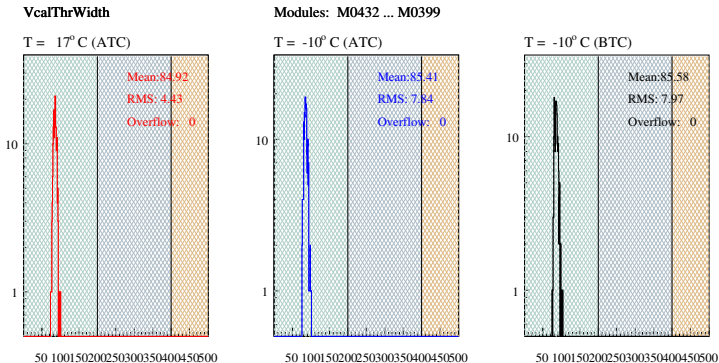
PedestalSpread of chips



Pedestal Spread in e^-

Vcal Threshold Width

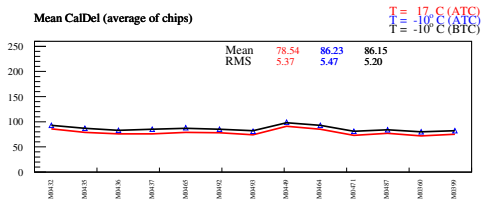
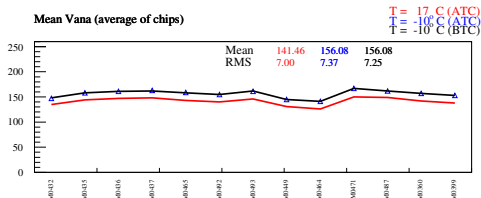
VcalThresholdWidth of chips



Vcal Thr. Width in e^-

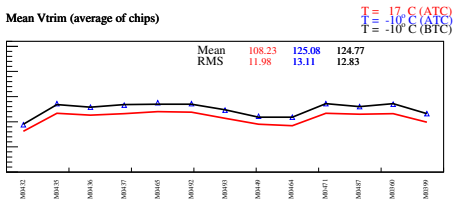
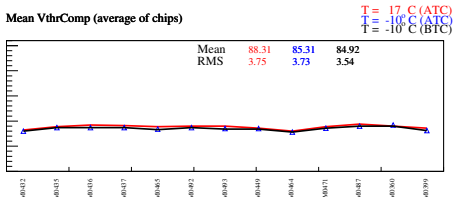
Operational parameters I

Mean DACs I



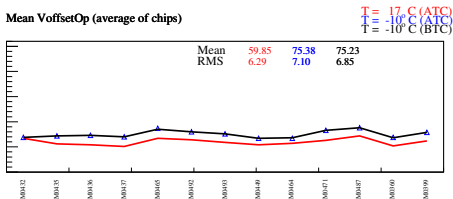
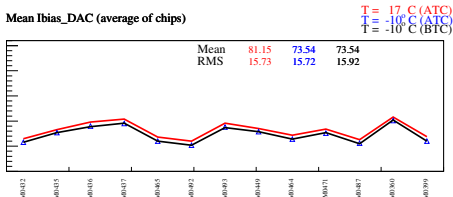
Operational parameters II

Mean DACs II



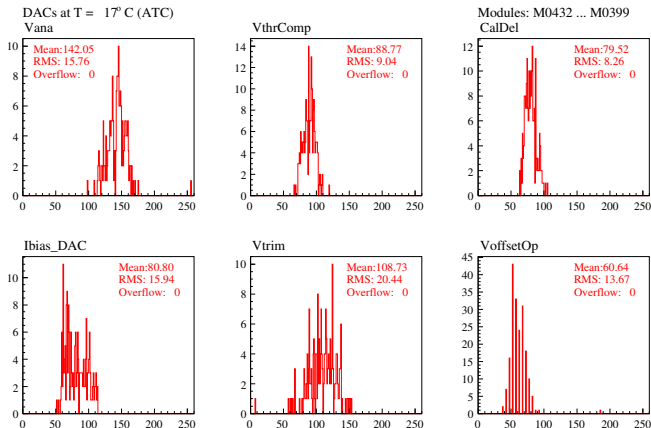
Operational parameters III

Mean DACs III



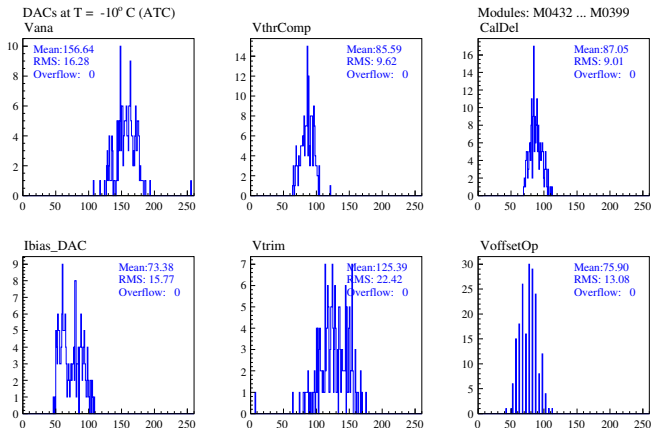
Operational parameters at $T = +17^{\circ}\text{C}$ (ATC)

DAC distribution (of chips)



Operational parameters at $T = -10^{\circ}\text{C}$ (ATC)

DAC distribution (of chips)

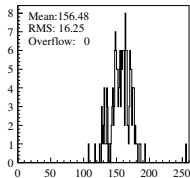


Operational parameters at $T = +17^{\circ}\text{C}$ (BTC)

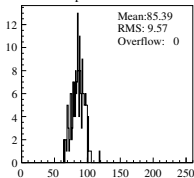
DAC distribution (of chips)

DACs at $T = -10^{\circ}\text{C}$ (BTC)

Vana

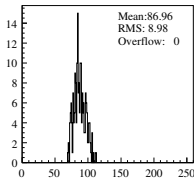


VthrComp

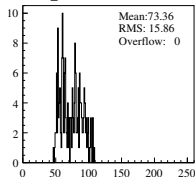


Modules: M0432 ... M0399

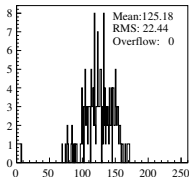
CalDel



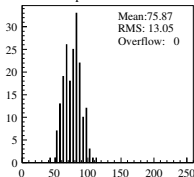
Ibias_DAC



Vtrim



VoffsetOp

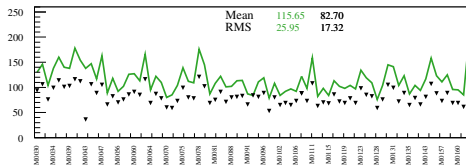


Operational parameters

Mean DACs I

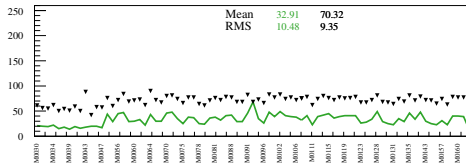
Mean Ibias_DAC (average of chips)

T = -10 C (ATC)
T = -10° C (ATC retest)



Mean VoffsetOp (average of chips)

T = -10 C (ATC)
T = -10° C (ATC retest)

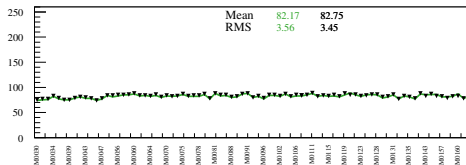


Operational parameters

Mean DACs II

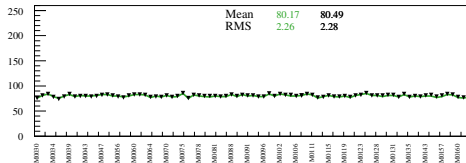
Mean VthrComp (average of chips)

T = -10. C (ATC)
T = -10° C (ATC retest)



Mean CalDel (average of chips)

T = -10. C (ATC)
T = -10° C (ATC retest)

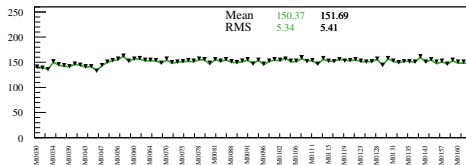


Operational parameters

Mean DACs III

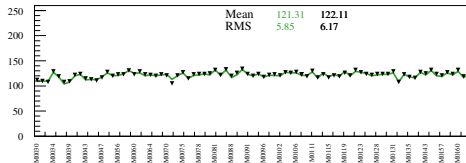
Mean Vana (average of chips)

T = -10° C (ATC)
T = -10° C (ATC retest)



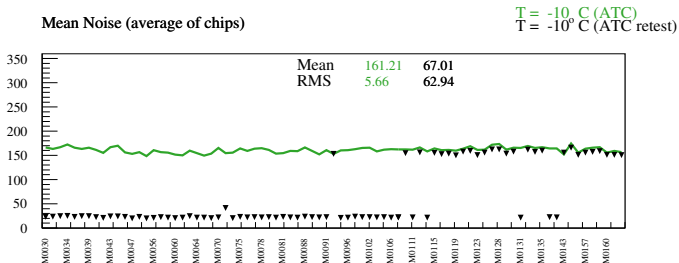
Mean Vtrim (average of chips)

T = -10° C (ATC)
T = -10° C (ATC retest)



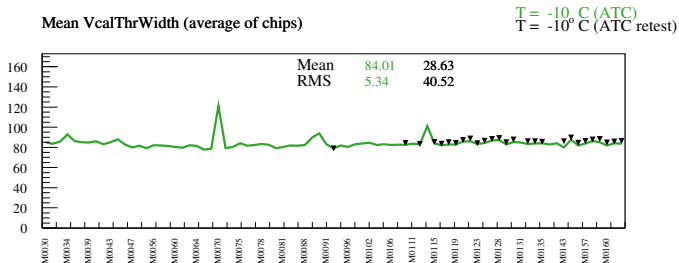
Performance parameters

Mean **Noise** [e^-] vs. Module Nr.



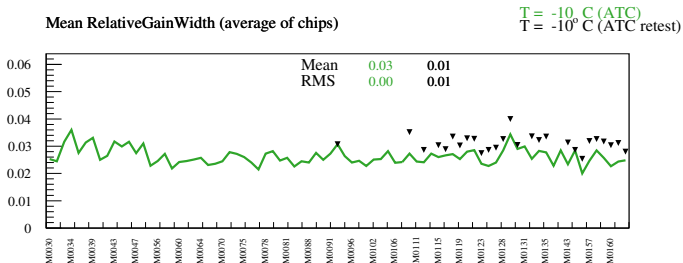
Performance parameters

Mean **VcalThresholdWidth** [e^-] vs. Module Nr.



Performance parameters

Mean **RelativeGainWidth** [%] vs. Module Nr.



Performance parameters

Mean **PedestalSpread** in $[e^-]$ vs. Module Nr.

