

BPIX Module Testing Status - Week 45

12th November 2007

Production overview

Production Status: 880 modules produced (757 full/ 123 half)

- 519/145 graded as A/B → 88% || 86/24 → 89%
- 93 graded as C → 12% || 13 → 11%

Module Testing Report of Week 45:

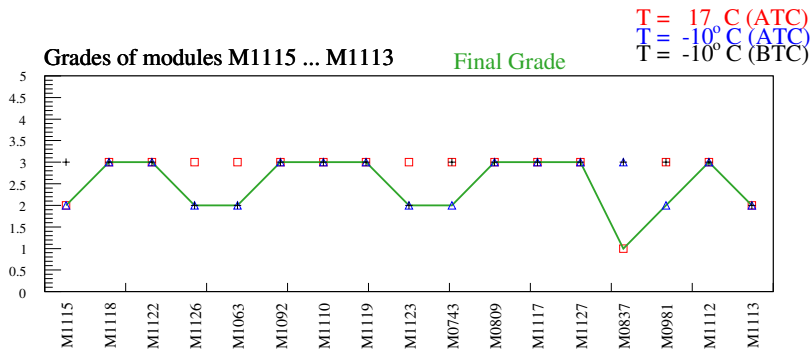
- 17 modules fully tested and therm. cycled (0 retested)

	Modules (17)			Halfmodules (–)		
Grade	A	B	C	A	B	C
T = –10° C, BTC*	13	4	0	–	–	–
T = –10° C, ATC	10	7	0	–	–	–
T = +17° C, ATC	14	2	1	–	–	–
Final Grade	9	7	1	–	–	–

- no retests with new DAC settings

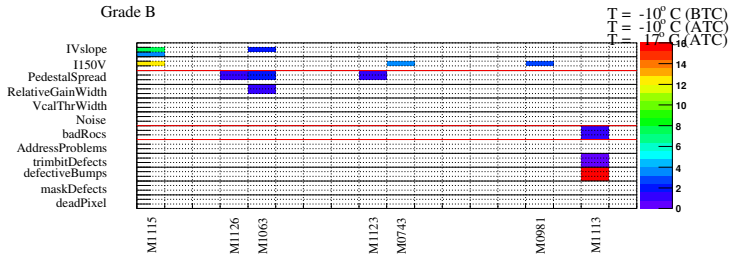
*without IV-criteria

Production summary

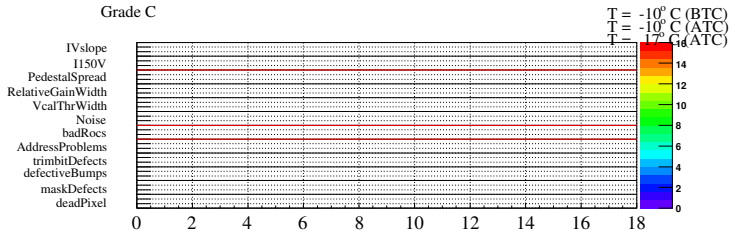


Module Failures Overview

Grade B



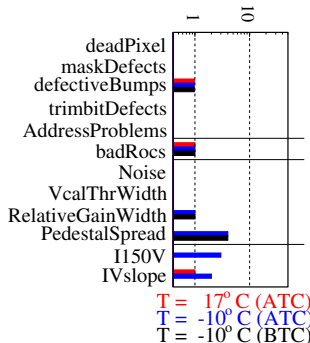
Grade C



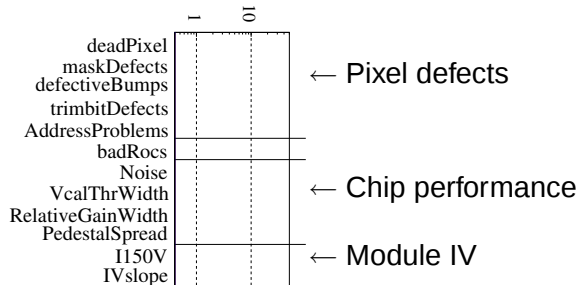
Production quality

Chip Failures

Grade B
Grade B



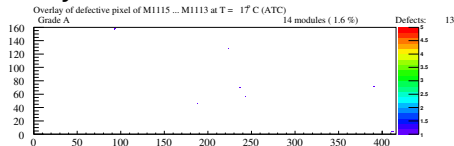
Grade C
Grade C



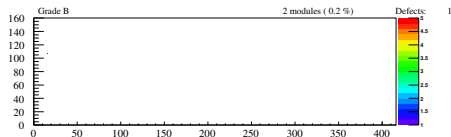
Defective pixel $T = 17^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = +17^{\circ}\text{C}$ (ATC)

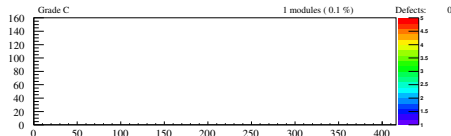
Grade A
(14 modules)



Grade B
(2 modules)



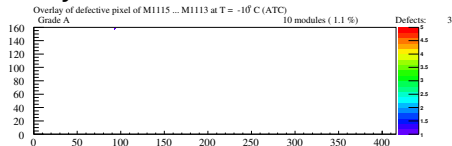
Grade C
(1 modules)



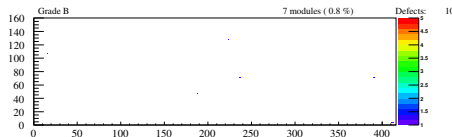
Defective pixel $T = -10^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (ATC)

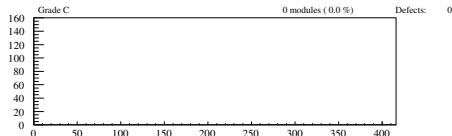
Grade A
(10 modules)



Grade B
(7 modules)



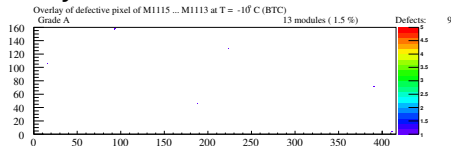
Grade C
(0 modules)



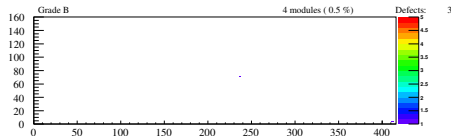
Defective pixel $T = -10^0\text{C}$ (BTC)

Overlay of all fully tested modules at $T = -10^0\text{C}$ (BTC)

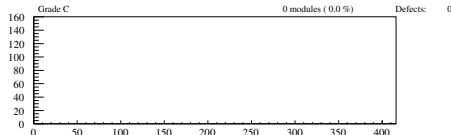
Grade A
(13 modules)



Grade B
(4 modules)



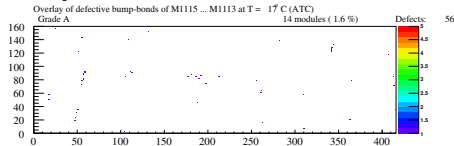
Grade C
(0 modules)



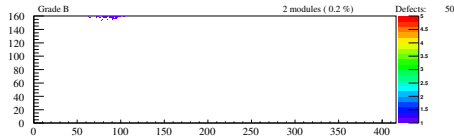
Defective bump-bonds $T = 17^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = +17^{\circ}\text{C}$ (ATC)

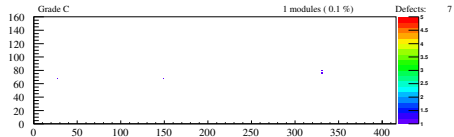
Grade A
(14 modules)



Grade B
(2 modules)



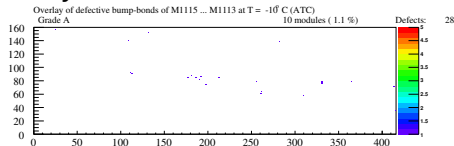
Grade C
(1 modules)



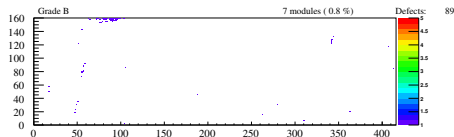
Defective bump-bonds $T = -10^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (ATC)

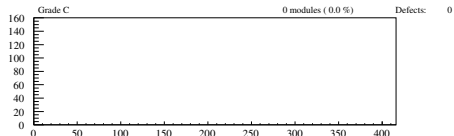
Grade A
(10 modules)



Grade B
(7 modules)



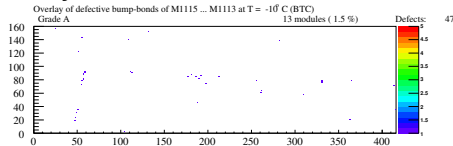
Grade C
(0 modules)



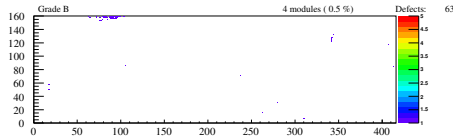
Defective bump-bonds $T = -10^{\circ}\text{C}$ (BTC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (BTC)

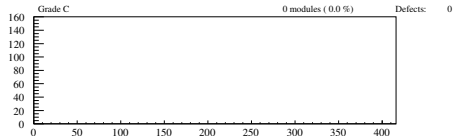
Grade A
(13 modules)



Grade B
(4 modules)



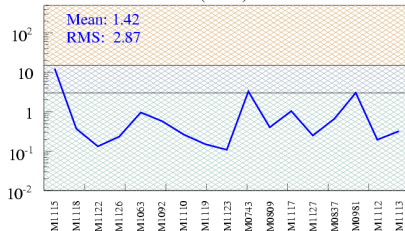
Grade C
(0 modules)



Current at 150 V

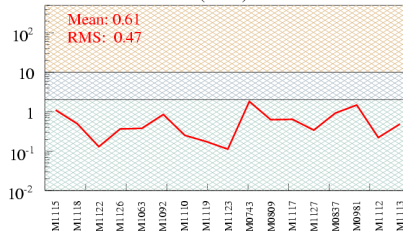
Current at 150 V (in μA) at $T = 17^\circ\text{C}$ and $T = -10^\circ\text{C}$

I150V at T = -10°C (ATC)



recalculated

I150V at T = 17°C (ATC)

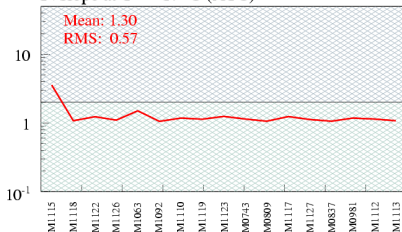


measured

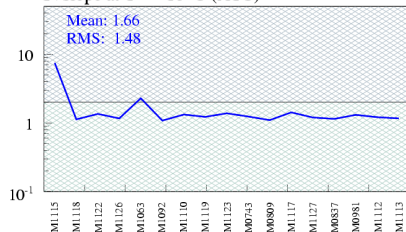
Slope of IV-Curve

Slope of IV-Curve at $T = 17^{\circ}\text{C}$ and $T = -10^{\circ}\text{C}$

IVslope at $T = 17^{\circ}\text{C}$ (ATC)

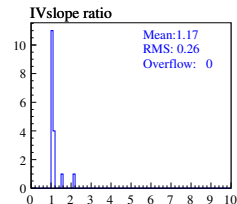
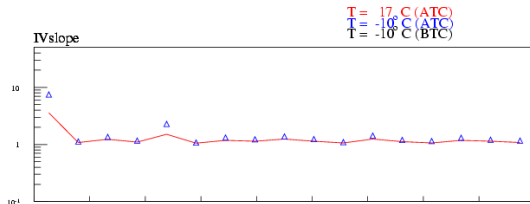
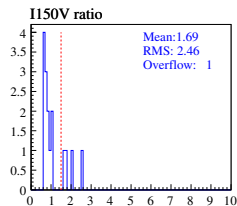
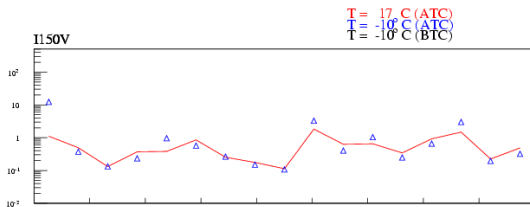


IVslope at $T = -10^{\circ}\text{C}$ (ATC)



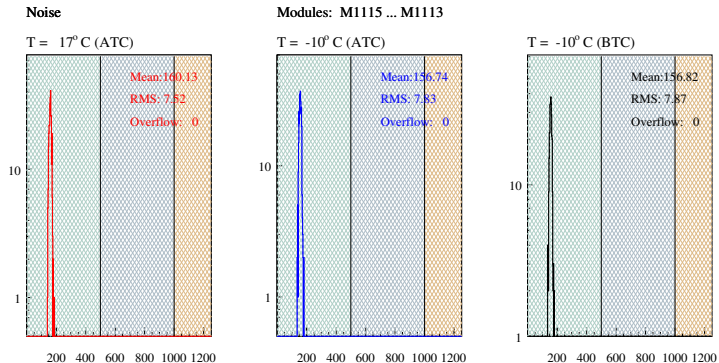
Current recalculation to $T = 17^{\circ}\text{C}$

Cross check of recalculated values with measured values



Noise

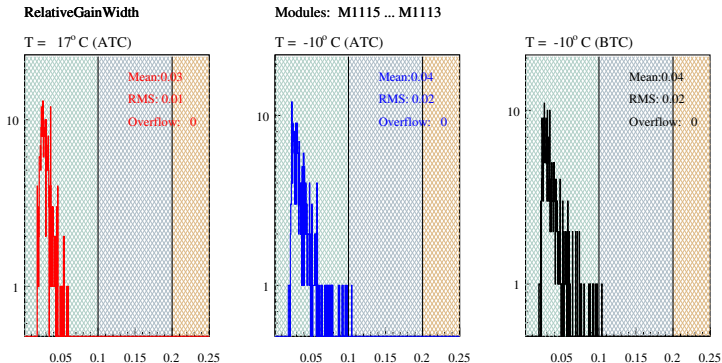
MeanNoise of chips



Noise in e^-

Relative Gain Width

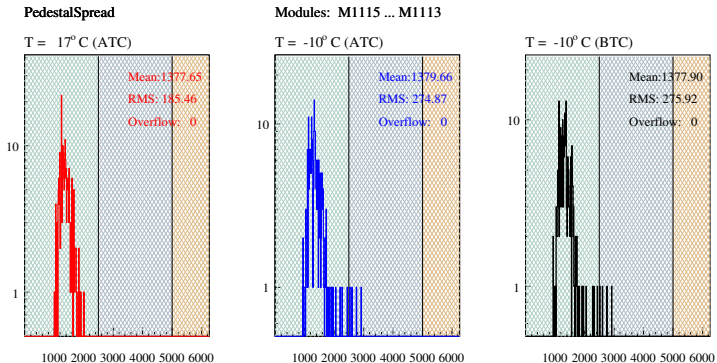
RelativeGainWidth of chips



Rel. Gain Width in %

Pedestal Spread

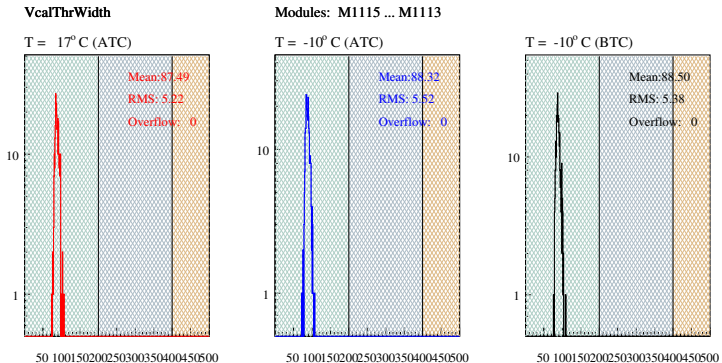
PedestalSpread of chips



Pedestal Spread in e^-

Vcal Threshold Width

VcalThresholdWidth of chips

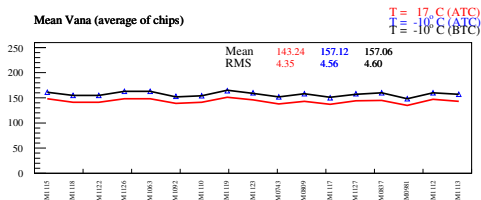


Vcal Thr. Width in e^-

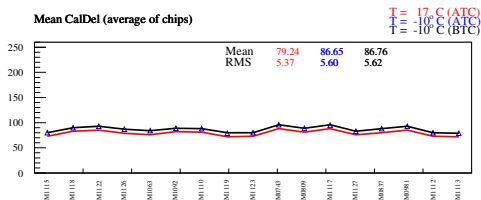
Operational parameters I

Mean DACs I

Mean Vana (average of chips)



Mean CalDel (average of chips)

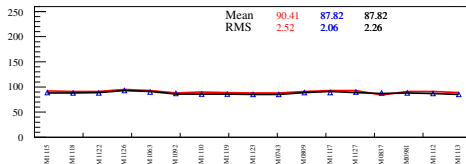


Operational parameters II

Mean DACs II

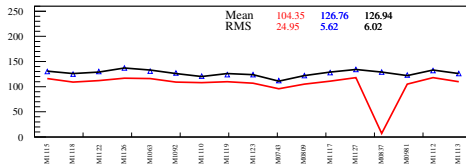
Mean VthrComp (average of chips)

T = 17° C (ATC)
T = -10° C (ATC)
T = -10° C (BTC)



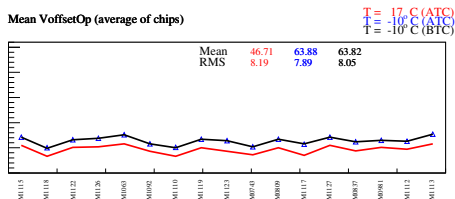
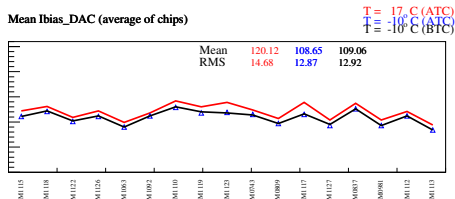
Mean Vtrim (average of chips)

T = 17° C (ATC)
T = -10° C (ATC)
T = -10° C (BTC)



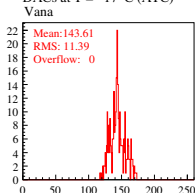
Operational parameters III

Mean DACs III

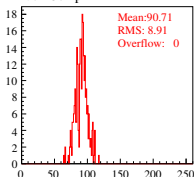


Operational parameters at $T = +17^{\circ}\text{C}$ (ATC)

DAC distribution (of chips)

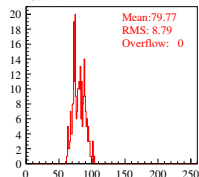
DACs at $T = 17^{\circ}\text{C}$ (ATC)

VthrComp

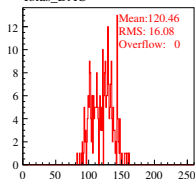


Modules: M1115 ... M1113

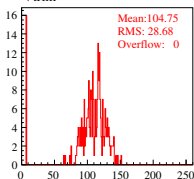
CalDel



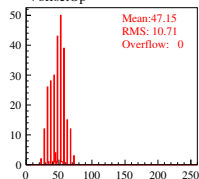
Ibias_DAC



Vtrim



VoffsetOp

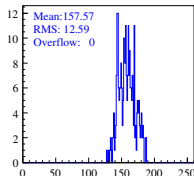


Operational parameters at $T = -10^{\circ}\text{C}$ (ATC)

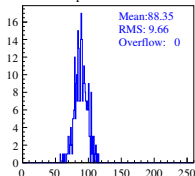
DAC distribution (of chips)

DACs at $T = -10^{\circ}\text{C}$ (ATC)

Vana

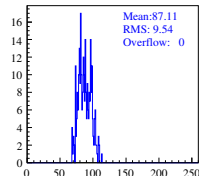


VthrComp

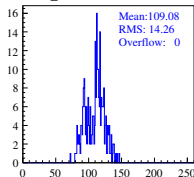


Modules: M1115 ... M1113

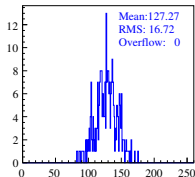
CalDel



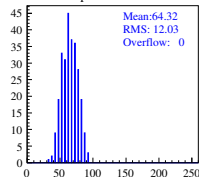
Ibias_DAC



Vtrim

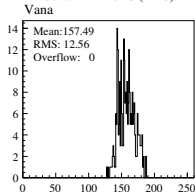


VoffsetOp

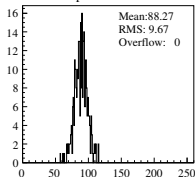


Operational parameters at $T = +17^{\circ}\text{C}$ (BTC)

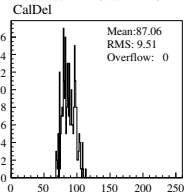
DAC distribution (of chips)

DACs at $T = -10^{\circ}\text{C}$ (BTC)

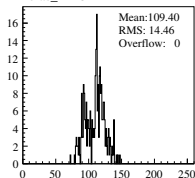
VthrComp



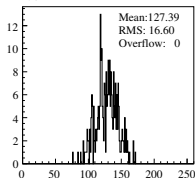
Modules: M1115 ... M1113



Ibias_DAC



Vtrim



VoffsetOp

