BPIX Module Testing Status - Week 40

8th October 2007

Production overview

Production Status: 803 modules produced (692 full/ 111 half)

- 488/123 graded as A/B → 88% || 80/20 → 90%
- 81 graded as C → 12% || 11 → 10%

Module Testing Report of Week 40:

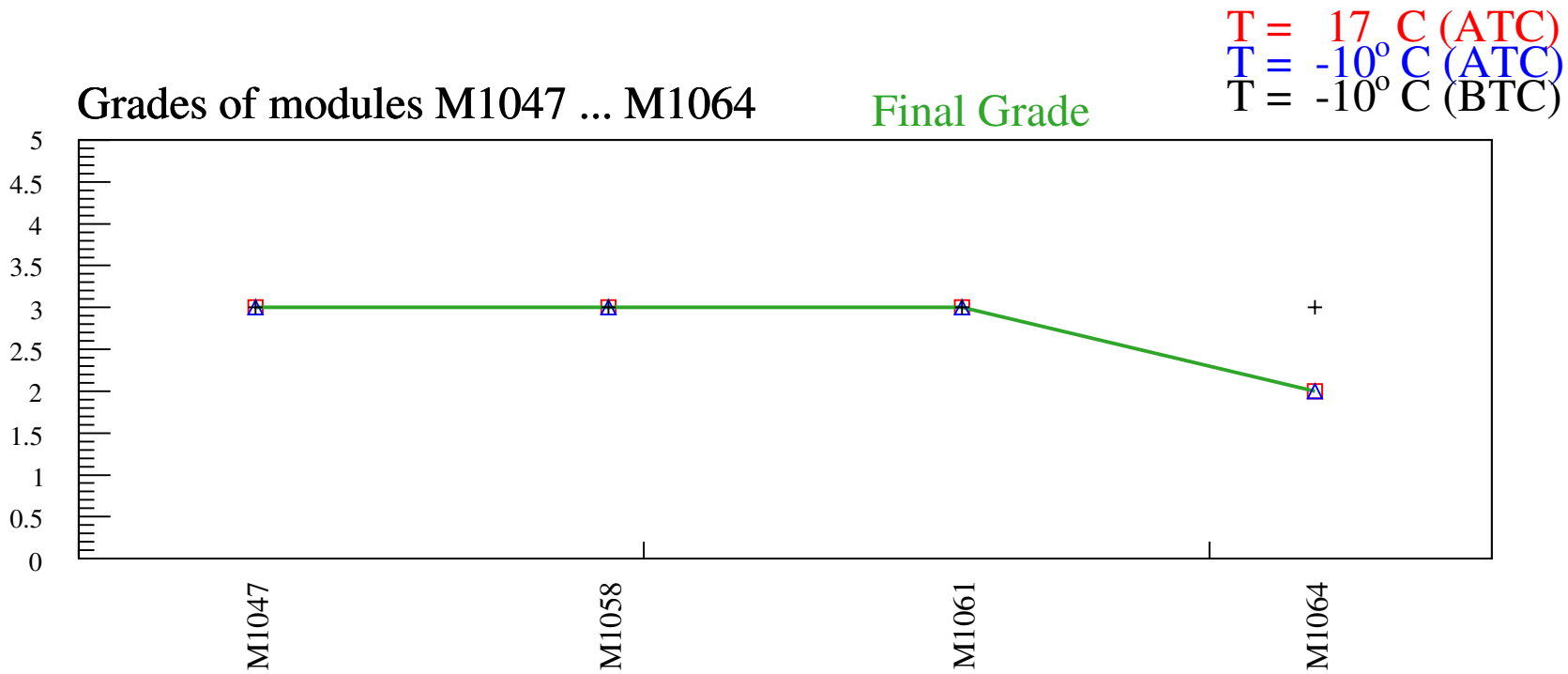
- 4 modules fully tested and therm. cycled (0 retested)

	Modules (4)			*Halfmodules* (–)		
Grade	**A**	**B**	**C**	**A**	**B**	**C**
T = -10^o C, BTC*	4	0	0	–	–	–
T = -10^o C, ATC	3	1	0	–	–	–
T = $+17^o$ C, ATC	3	1	0	–	–	–
Final Grade	3	1	0	–	–	–

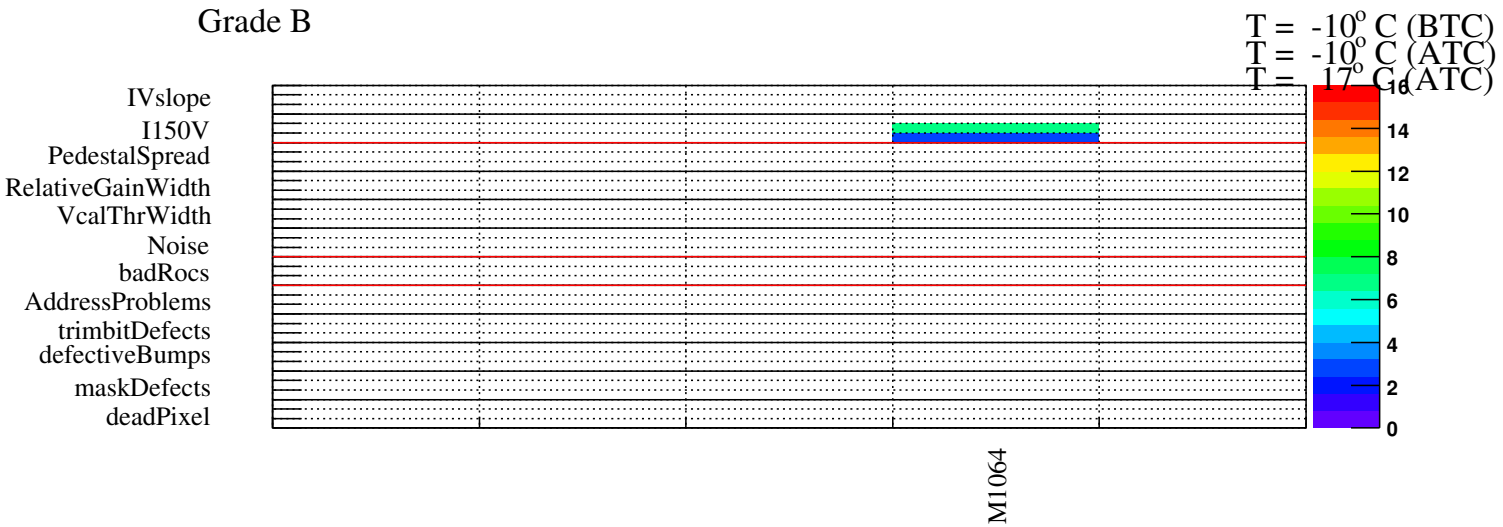
- no retests with new DAC settings

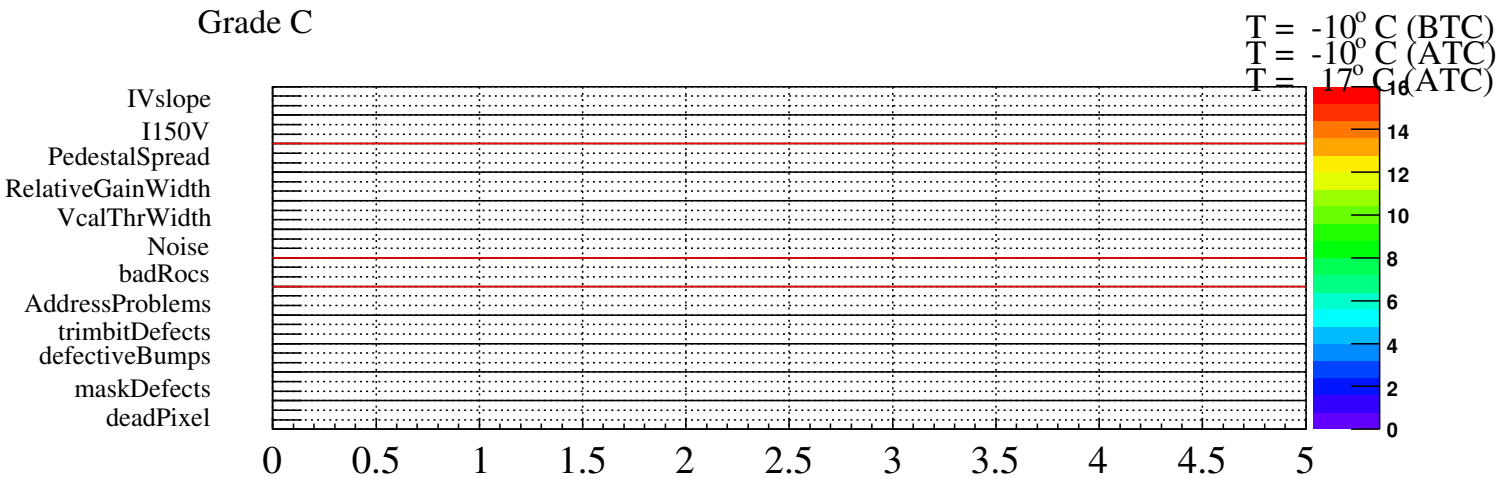
*without IV-criteria

Production summary



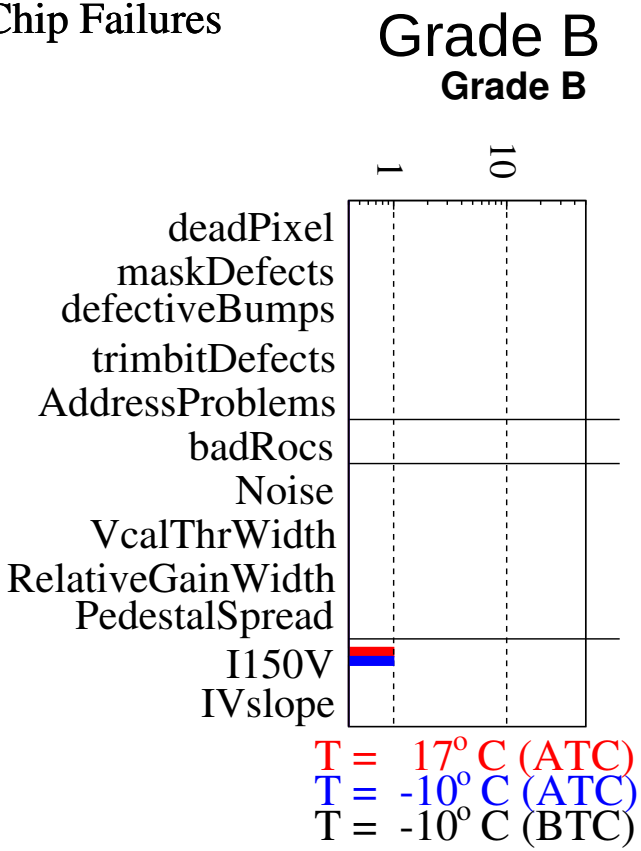
Module Failures Overview

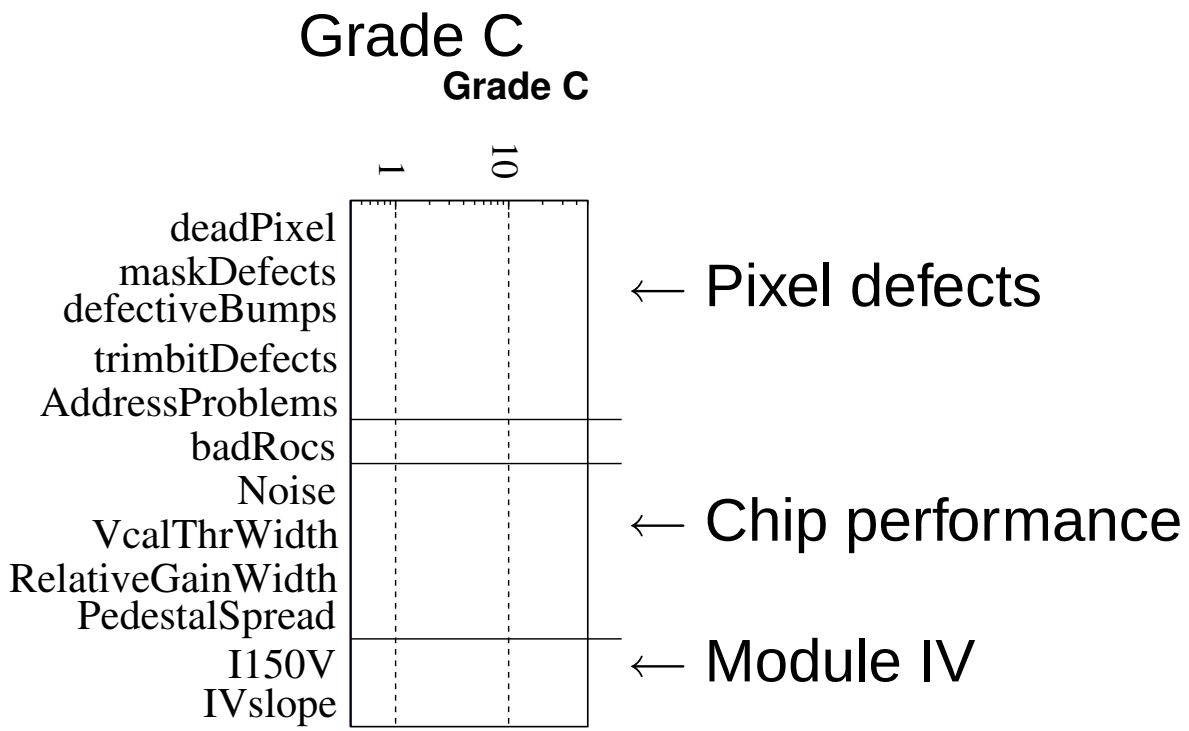




Production quality

Chip Failures

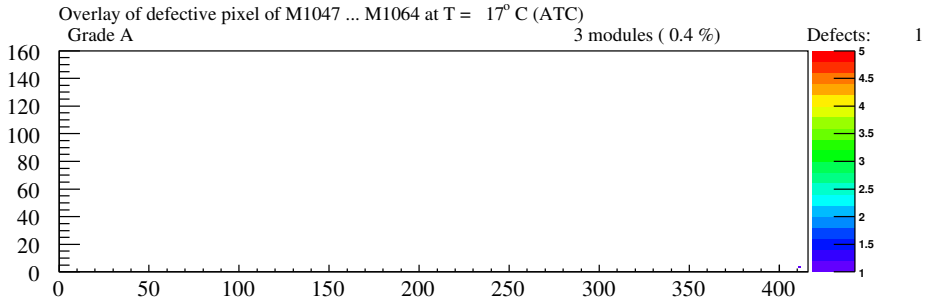




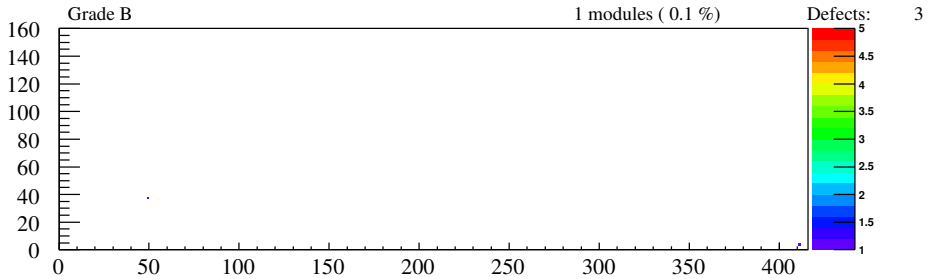
Defective pixel $T = 17^{o}C$ (ATC)

Overlay of all fully tested modules at T = $+17^{o}$ C (ATC)

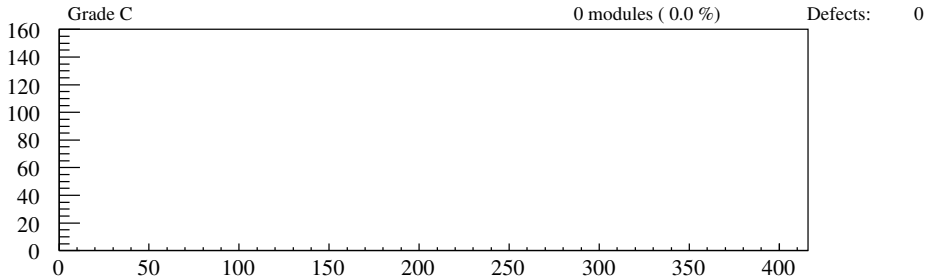
Grade A
(3 modules)



Grade B
(1 modules)



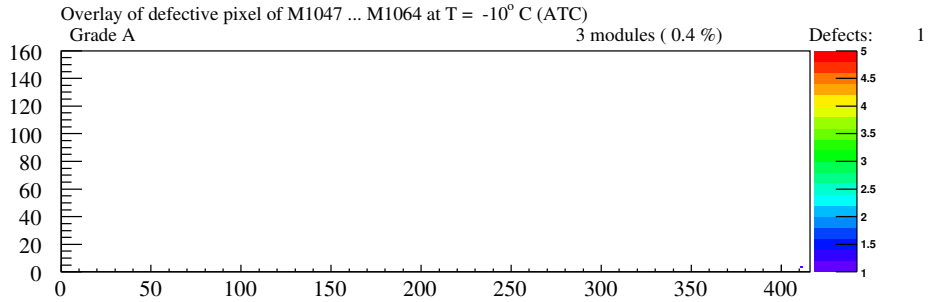
Grade C
(0 modules)



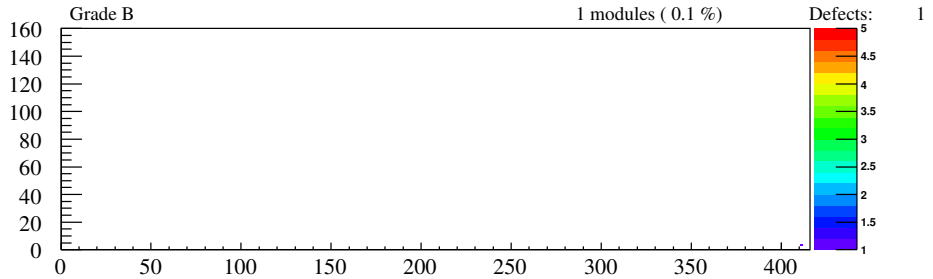
Defective pixel $T = -10^{o}C$ (ATC)

Overlay of all fully tested modules at T = -10^{o} C (ATC)

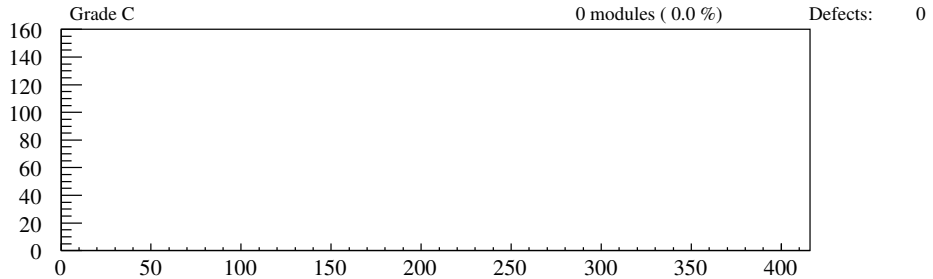
Grade A
(3 modules)



Grade B
(1 modules)



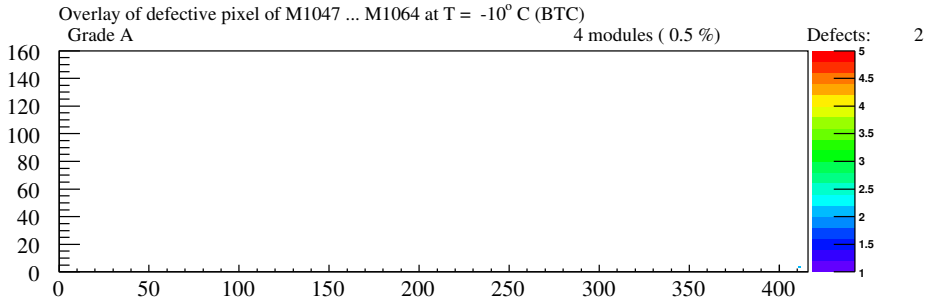
Grade C
(0 modules)



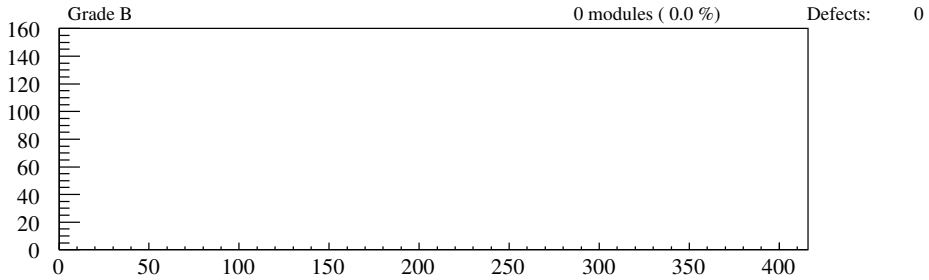
Defective pixel $T = -10^{o}C$ (BTC)

Overlay of all fully tested modules at T = -10^{o} C (BTC)

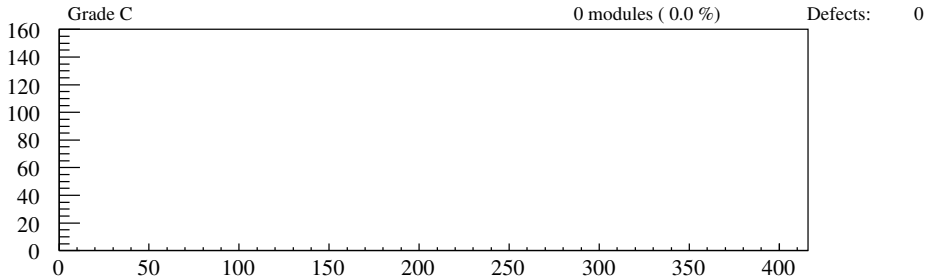
Grade A
(4 modules)



Grade B
(0 modules)



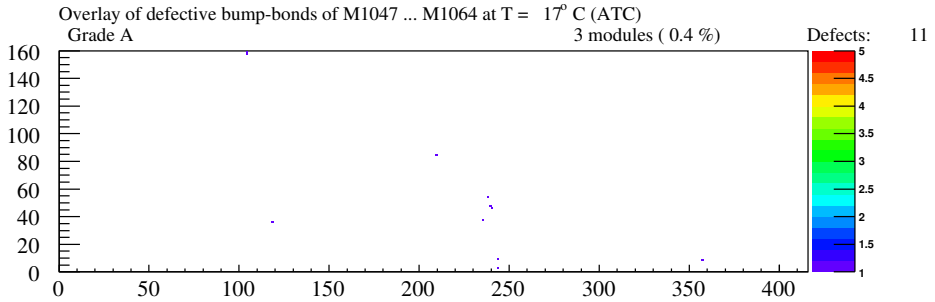
Grade C
(0 modules)



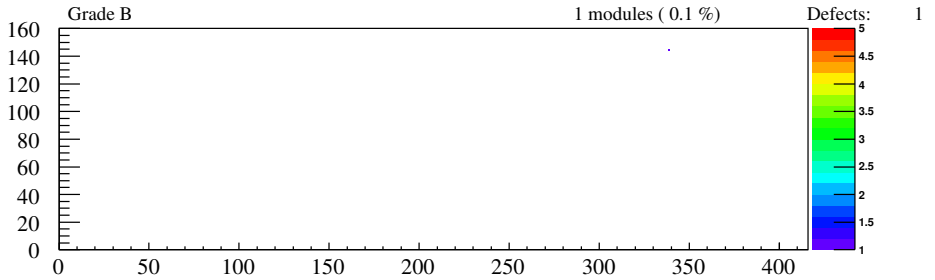
Defective bump-bonds $T = 17^oC$ (ATC)

Overlay of all fully tested modules at T = $+17^o$ C (ATC)

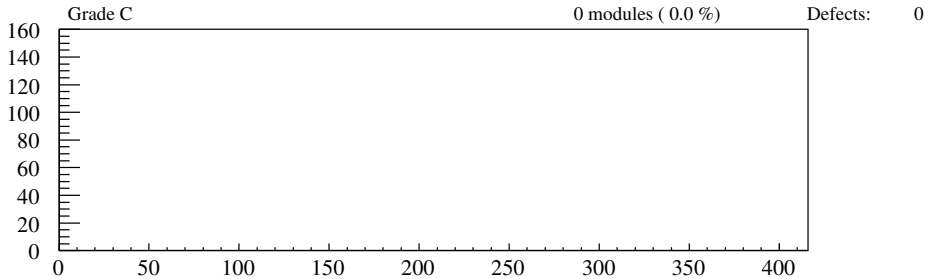
Grade A
(3 modules)



Grade B
(1 modules)



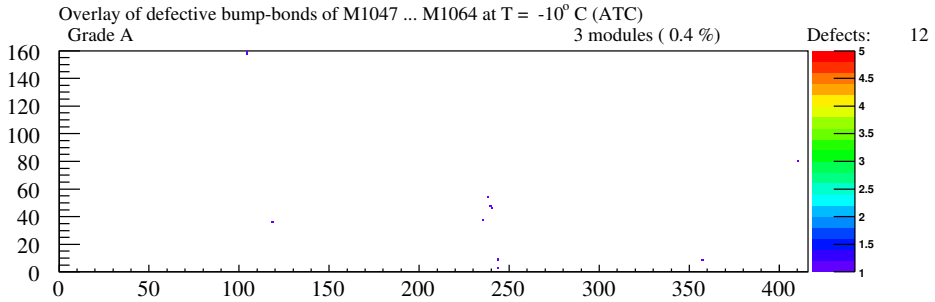
Grade C
(0 modules)



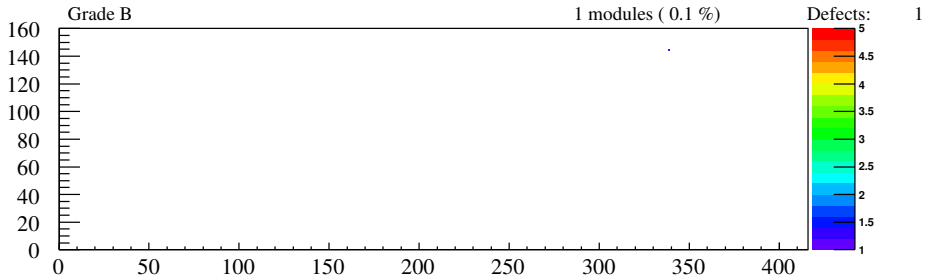
Defective bump-bonds $T = -10^{o}C$ (ATC)

Overlay of all fully tested modules at T = -10^{o} C (ATC)

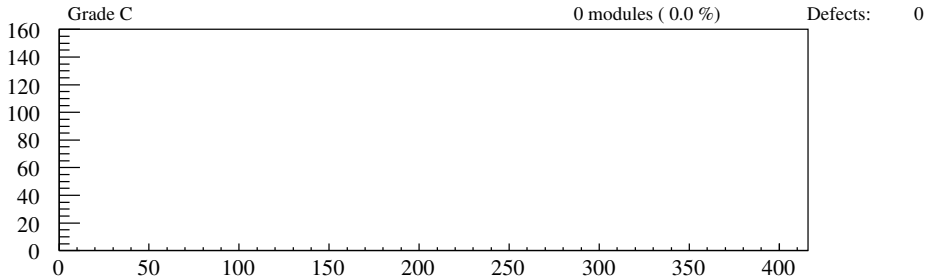
Grade A
(3 modules)



Grade B
(1 modules)



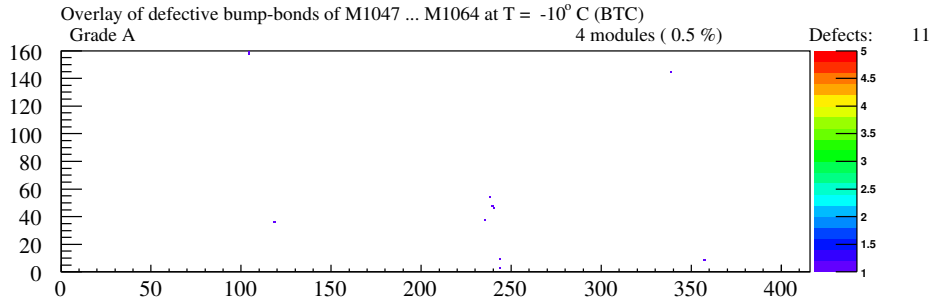
Grade C
(0 modules)



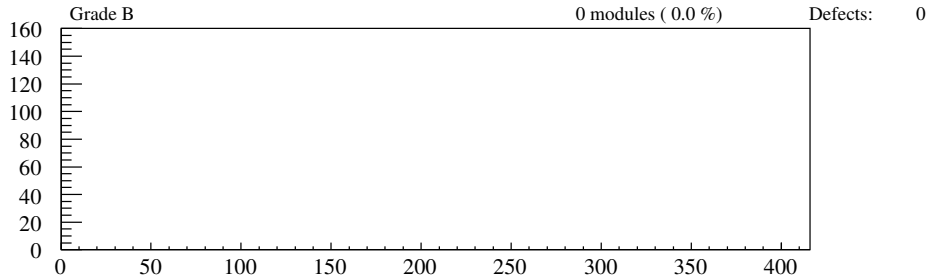
Defective bump-bonds $T = -10^{o}C$ (BTC)

Overlay of all fully tested modules at T = -10^{o} C (BTC)

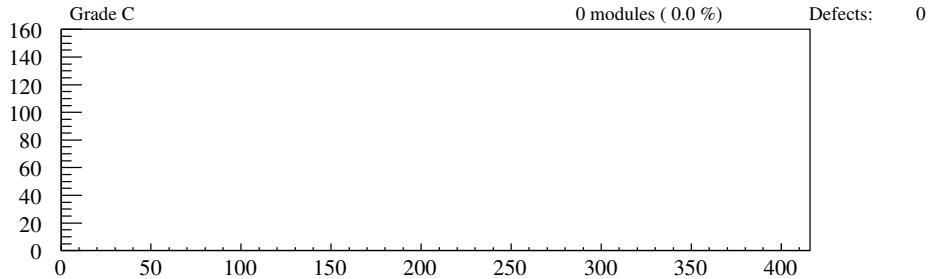
Grade A
(4 modules)



Grade B
(0 modules)

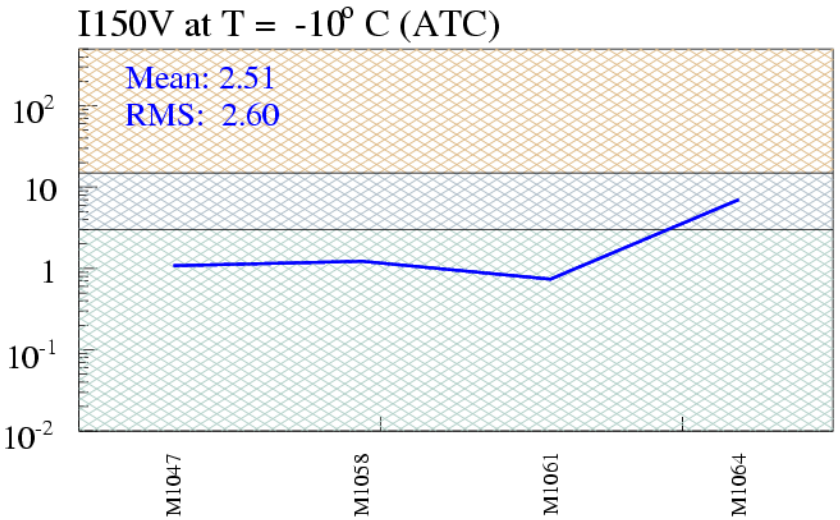


Grade C
(0 modules)

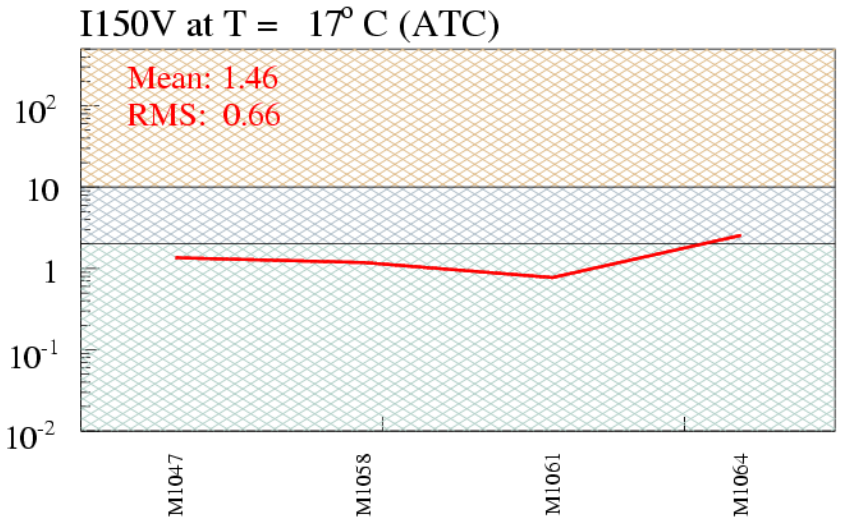


Current at 150 V

Current at 150 V (in μA) at $T = 17^oC$ and $T = -10^oC$



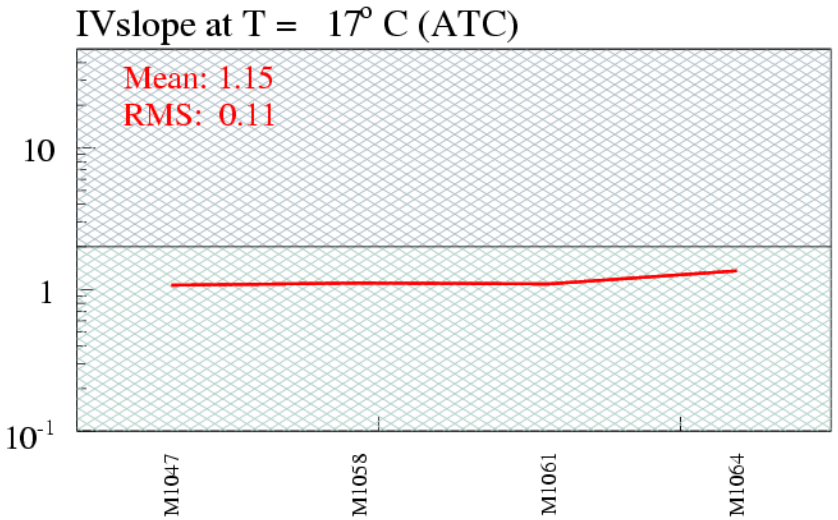
recalculated

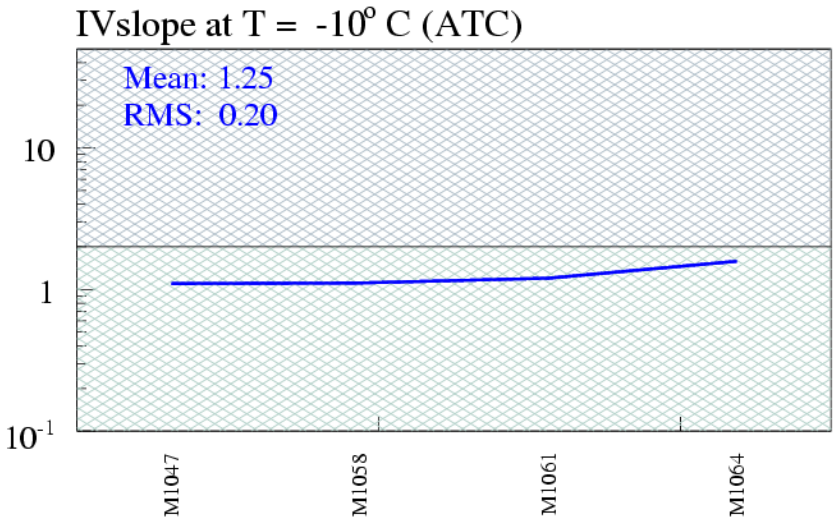


measured

Slope of IV-Curve

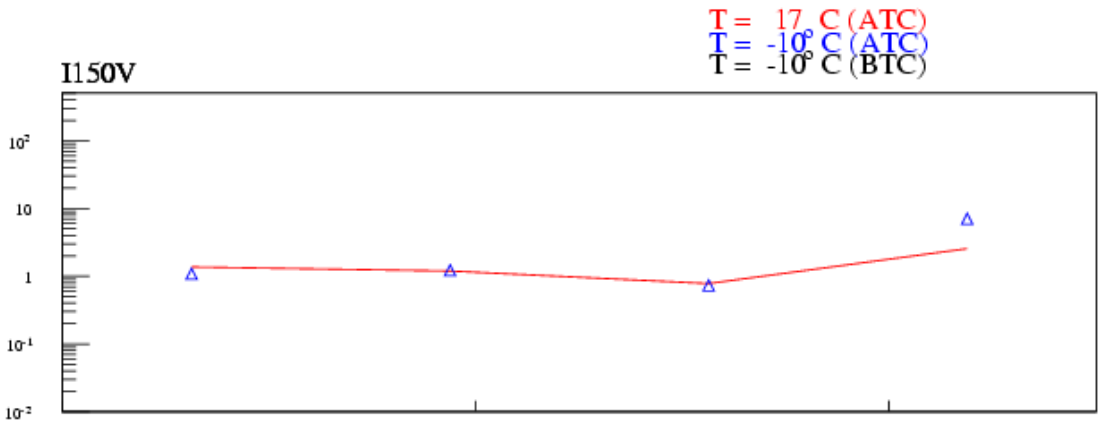
Slope of IV-Curveat $T = 17^oC$ and $T = -10^oC$

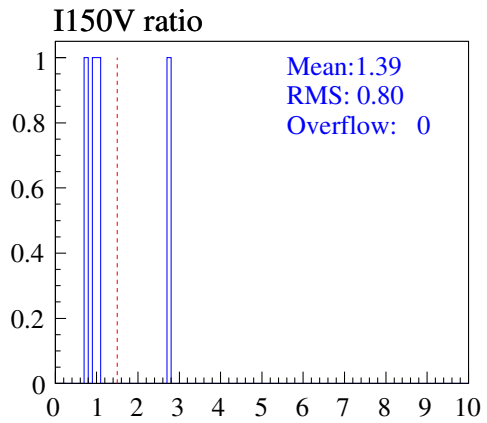


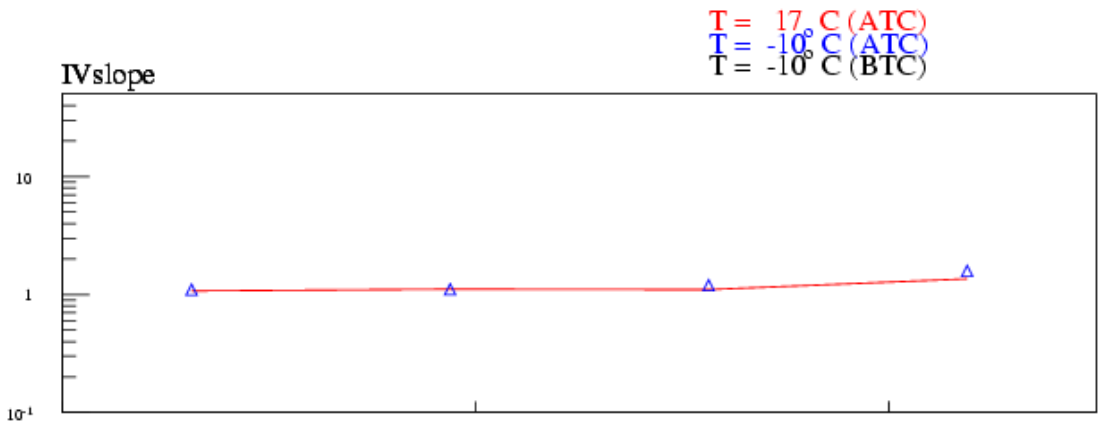


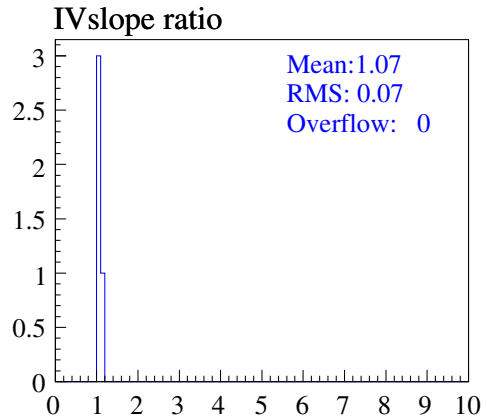
Current recalculation to $T = 17^oC$

Cross check of recalculated values with measured values



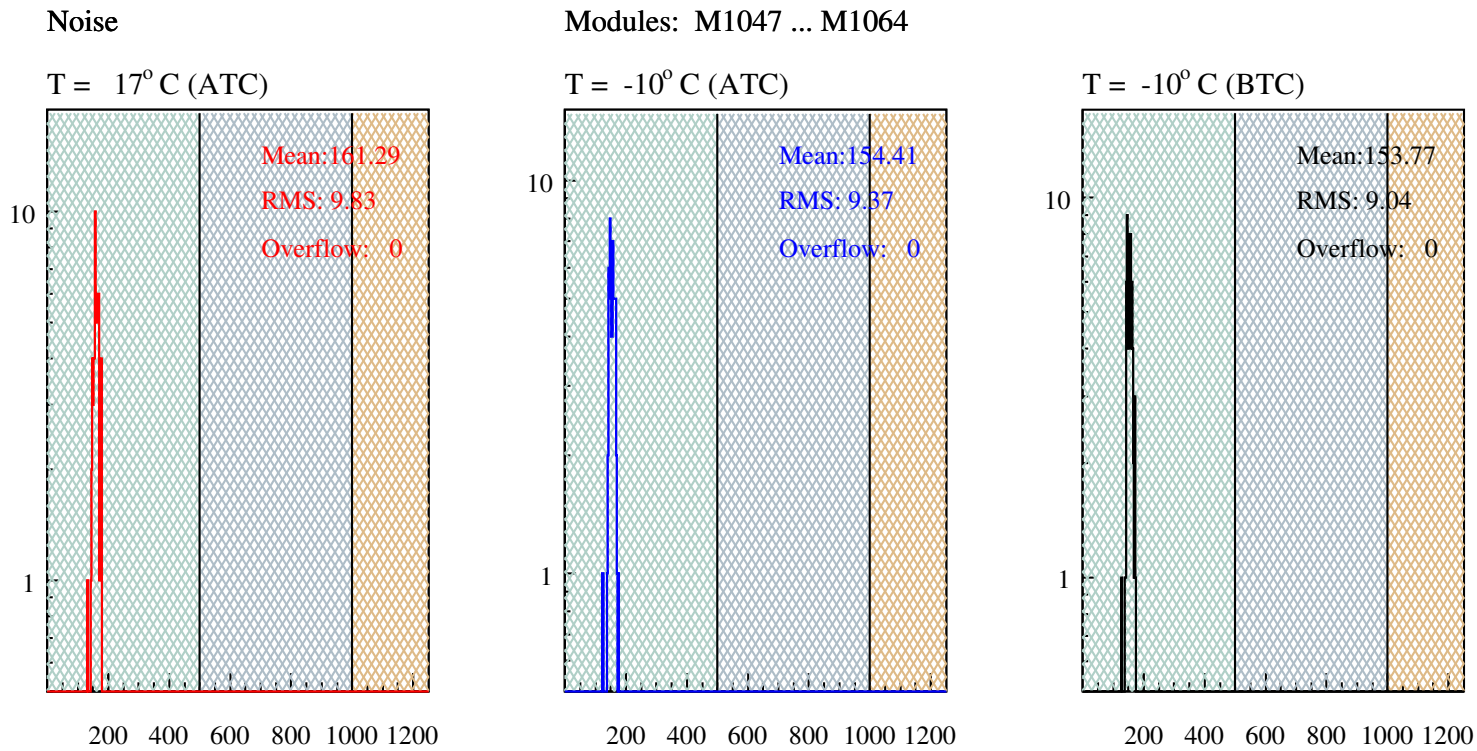






Noise

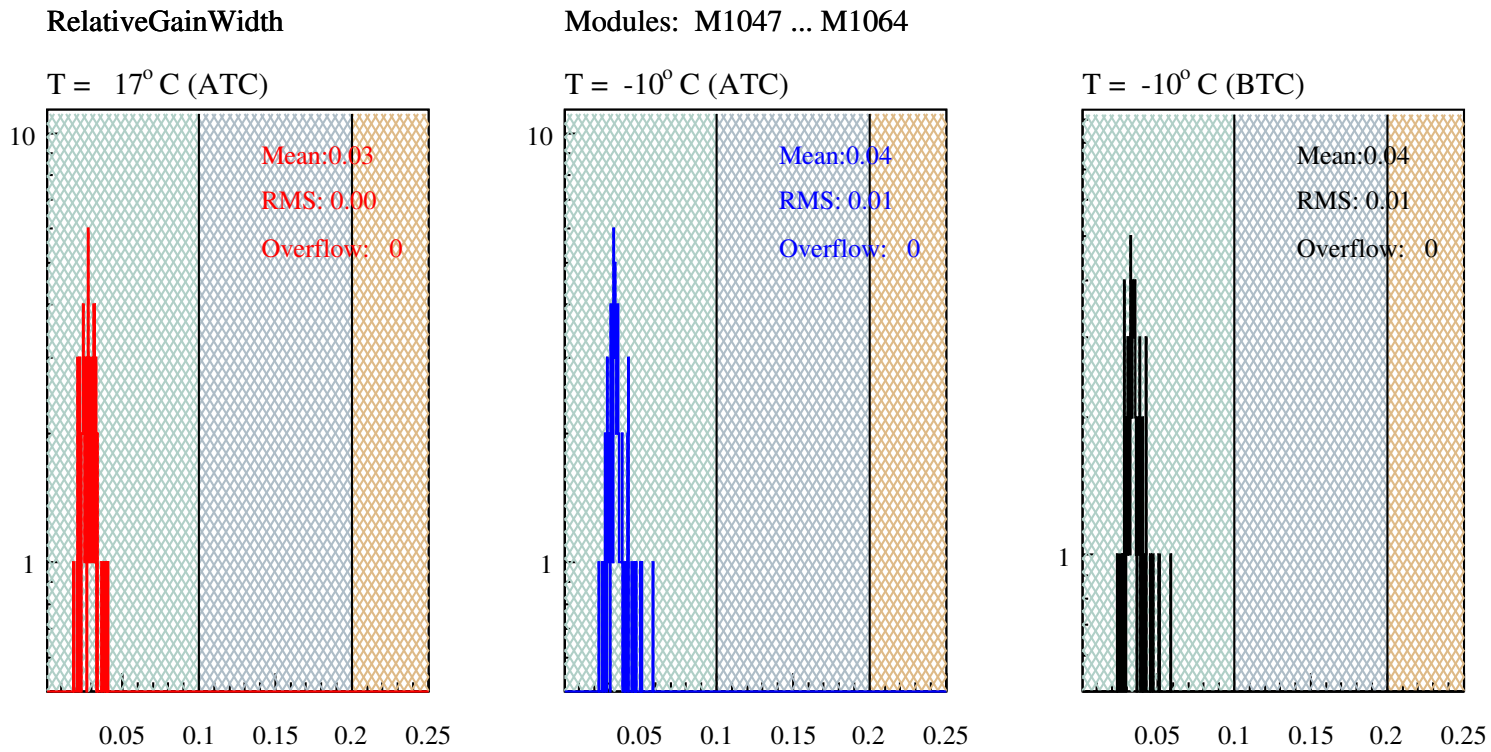
MeanNoise of chips



Noise in e^-

Relative Gain Width

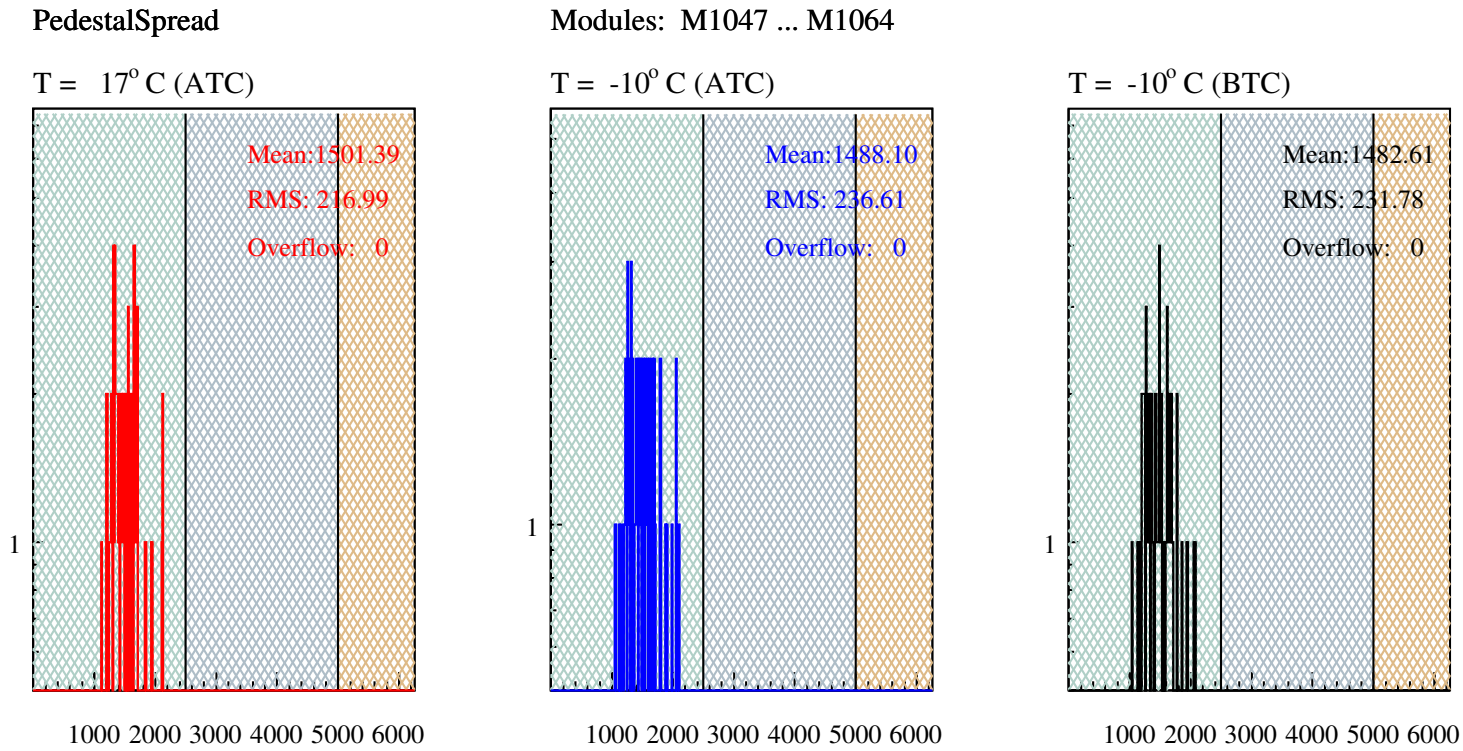
RelativeGainWidth of chips



Rel. Gain Width in %

Pedestal Spread

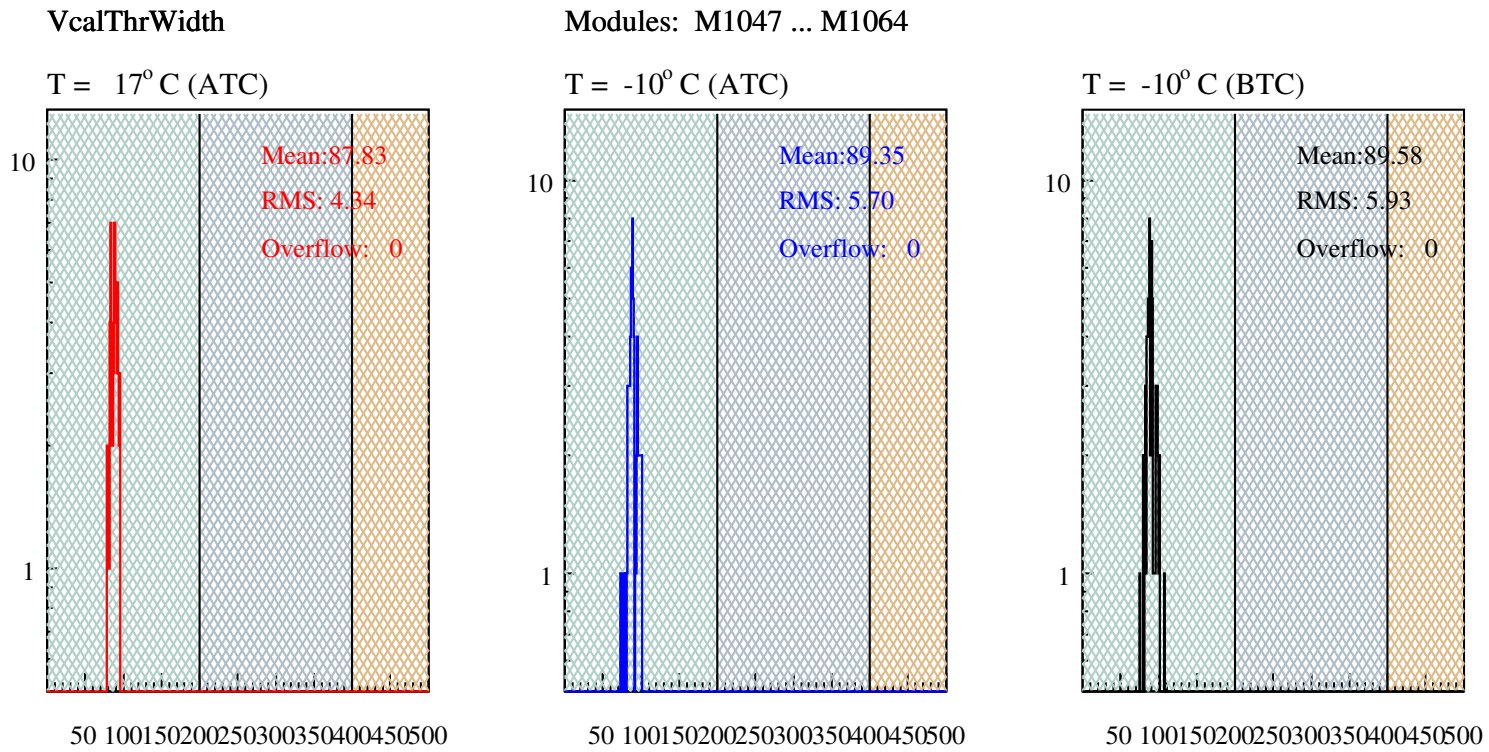
PedestalSpread of chips



Pedestal Spread in e^-

Vcal Threshold Width

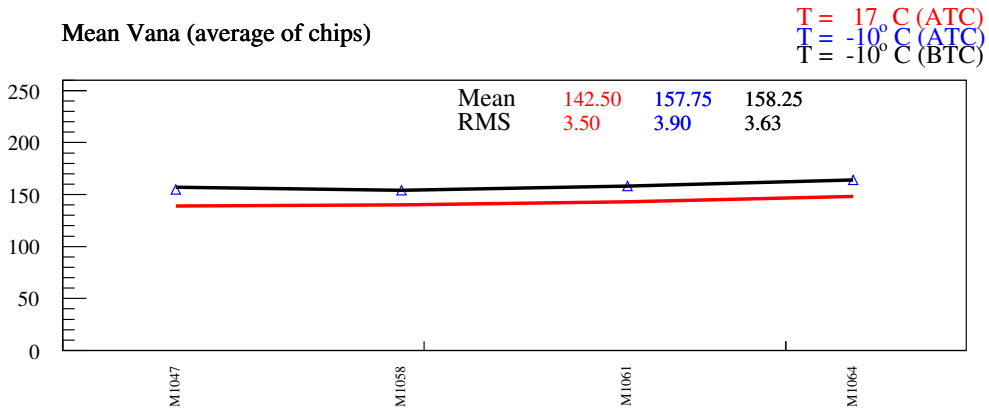
VcalThresholdWidth of chips

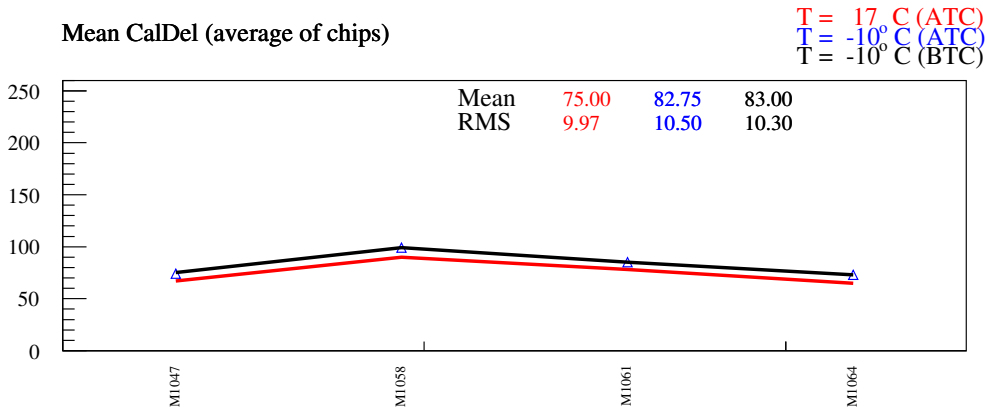


Vcal Thr. Width in e^-

Operational parameters I

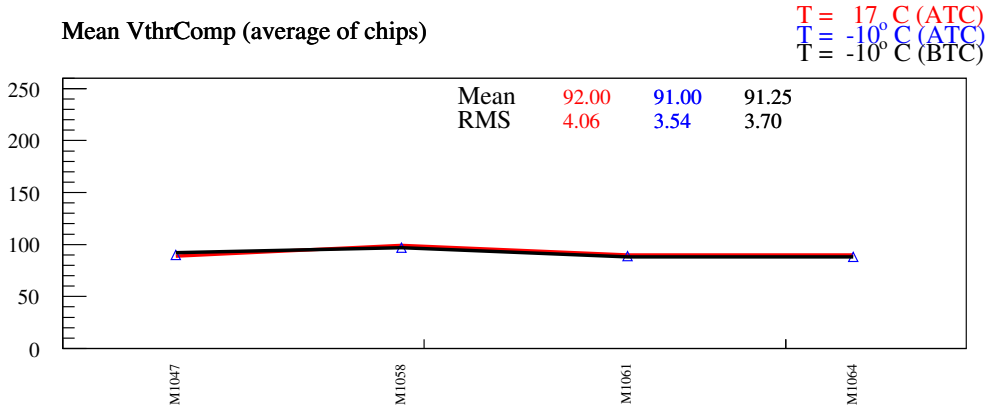
Mean DACs I

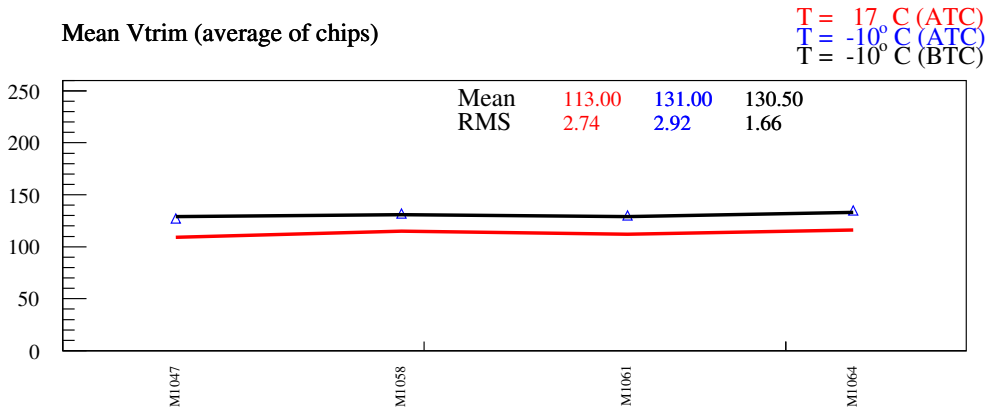




Operational parameters II

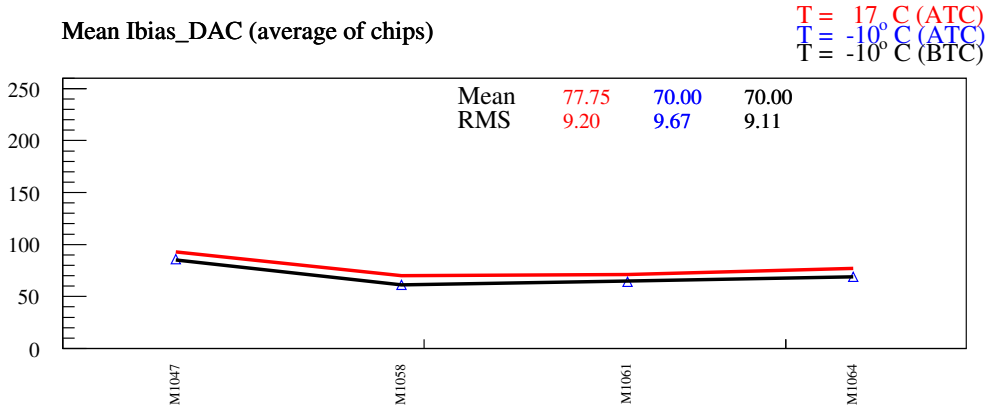
Mean DACs II

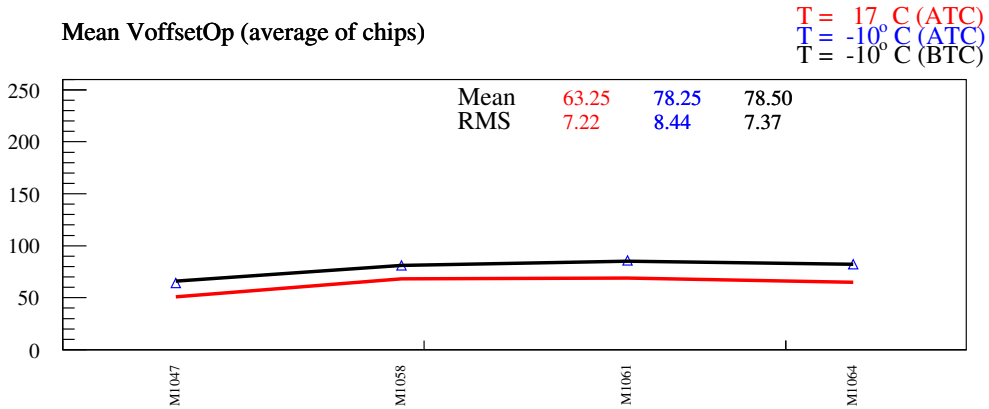




Operational parameters III

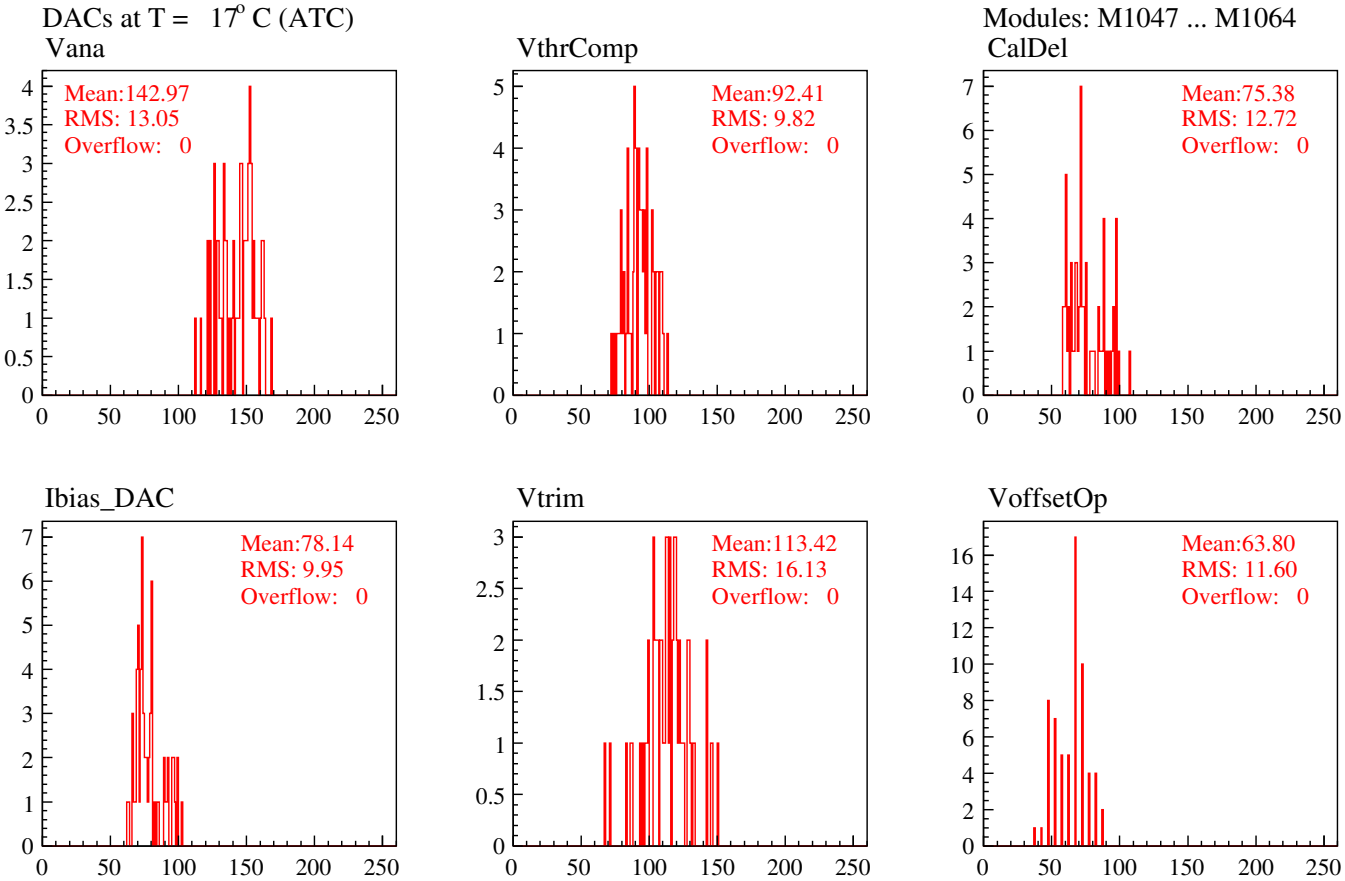
Mean DACs III





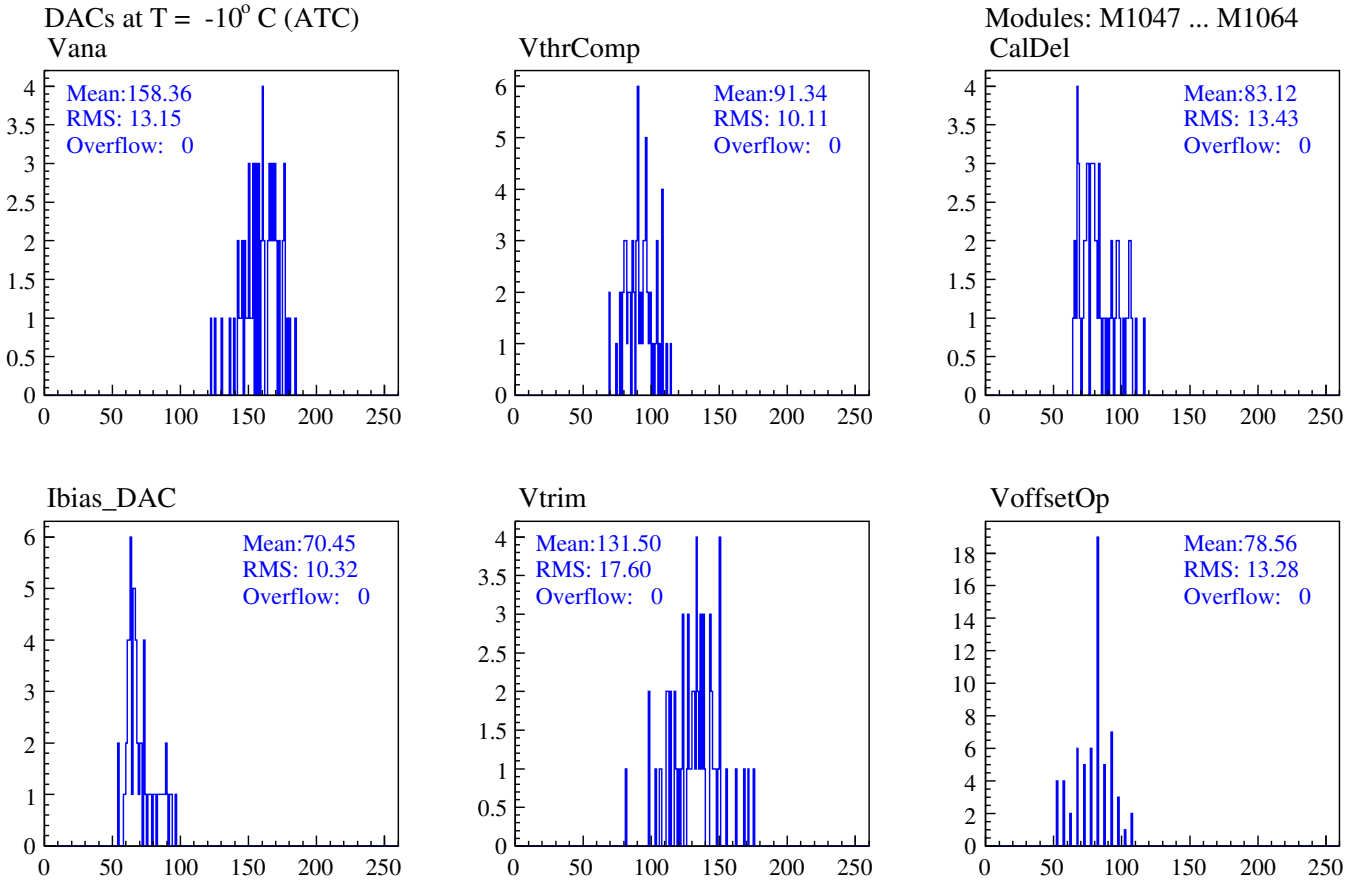
Operational parameters at $T = +17^{o}C$ (ATC)

DAC distribution (of chips)



Operational parameters at $T = -10^{o}C$ (ATC)

DAC distribution (of chips)



Operational parameters at $T = +17^{o}C$ (BTC)

DAC distribution (of chips)