

BPIX Module Testing Status - Week 40

8th October 2007

Production overview

Production Status: 803 modules produced (692 full/ 111 half)

- 488/123 graded as A/B → 88% || 80/20 → 90%
- 81 graded as C → 12% || 11 → 10%

Module Testing Report of Week 40:

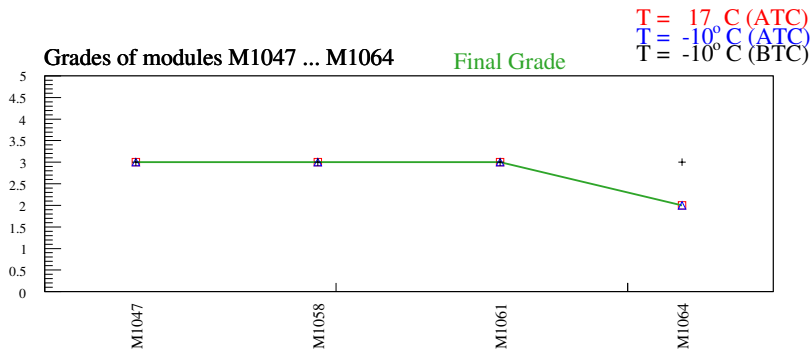
- 4 modules fully tested and therm. cycled (0 retested)

	Modules (4)			Halfmodules (–)		
Grade	A	B	C	A	B	C
T = –10° C, BTC*	4	0	0	–	–	–
T = –10° C, ATC	3	1	0	–	–	–
T = +17° C, ATC	3	1	0	–	–	–
Final Grade	3	1	0	–	–	–

- no retests with new DAC settings

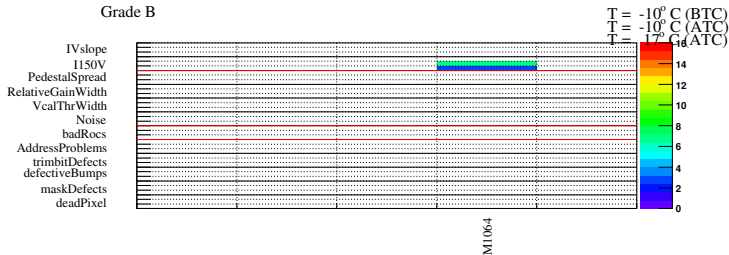
*without IV-criteria

Production summary

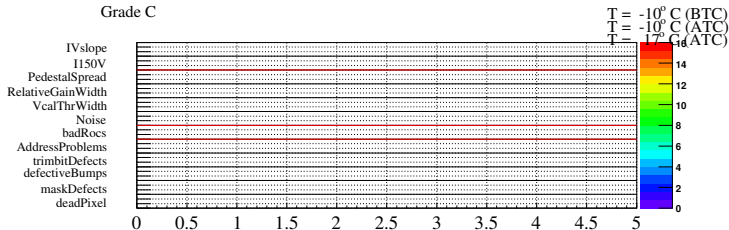


Module Failures Overview

Grade B



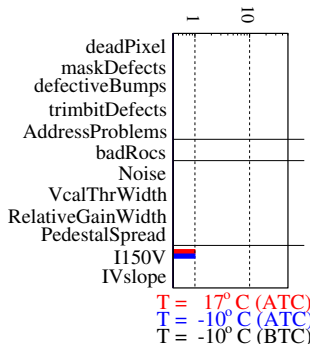
Grade C



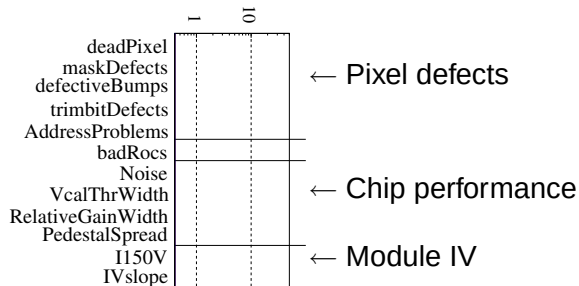
Production quality

Chip Failures

Grade B
Grade B



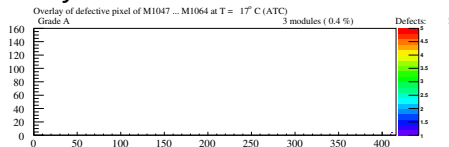
Grade C
Grade C



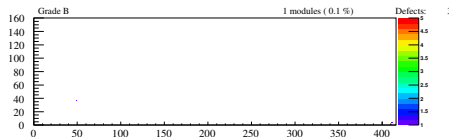
Defective pixel $T = 17^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = +17^{\circ}\text{C}$ (ATC)

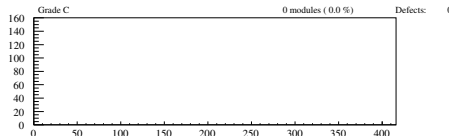
Grade A
(3 modules)



Grade B
(1 modules)



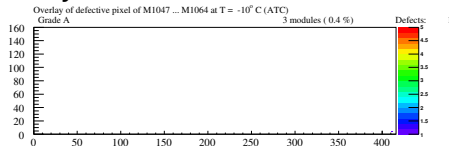
Grade C
(0 modules)



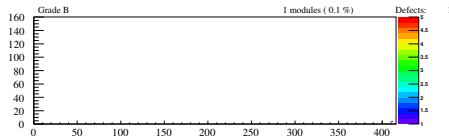
Defective pixel $T = -10^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (ATC)

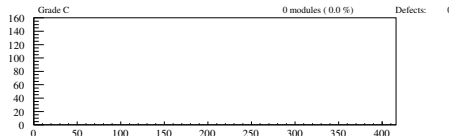
Grade A
(3 modules)



Grade B
(1 modules)



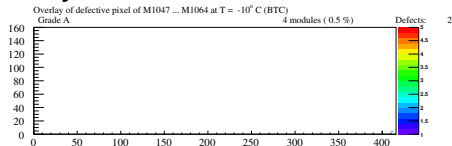
Grade C
(0 modules)



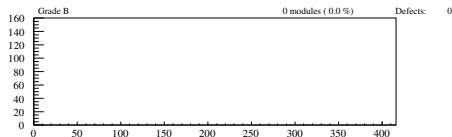
Defective pixel $T = -10^{\circ}\text{C}$ (BTC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (BTC)

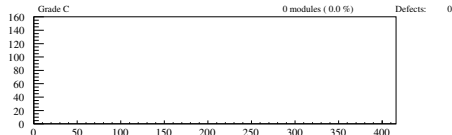
Grade A
(4 modules)



Grade B
(0 modules)



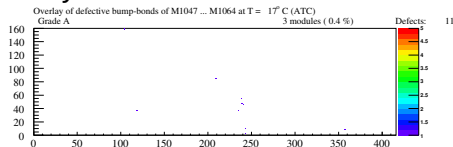
Grade C
(0 modules)



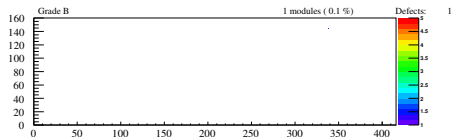
Defective bump-bonds $T = 17^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = +17^{\circ}\text{C}$ (ATC)

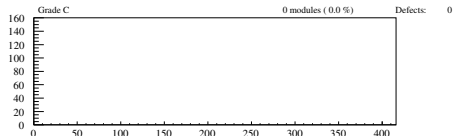
Grade A
(3 modules)



Grade B
(1 modules)



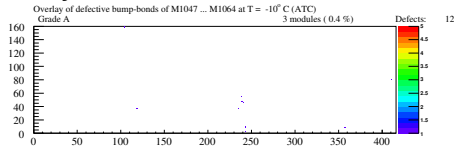
Grade C
(0 modules)



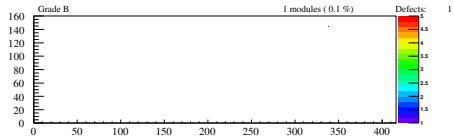
Defective bump-bonds $T = -10^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (ATC)

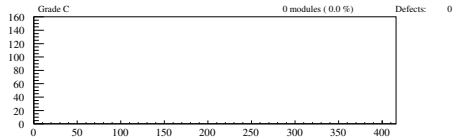
Grade A
(3 modules)



Grade B
(1 modules)



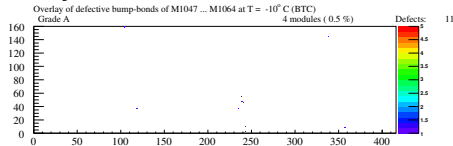
Grade C
(0 modules)



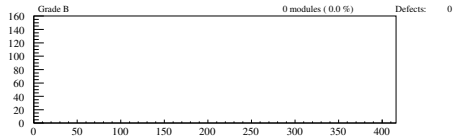
Defective bump-bonds $T = -10^{\circ}\text{C}$ (BTC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (BTC)

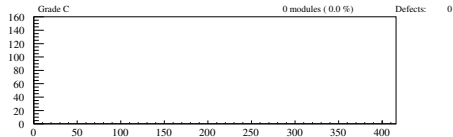
Grade A
(4 modules)



Grade B
(0 modules)



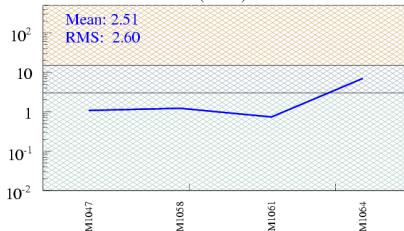
Grade C
(0 modules)



Current at 150 V

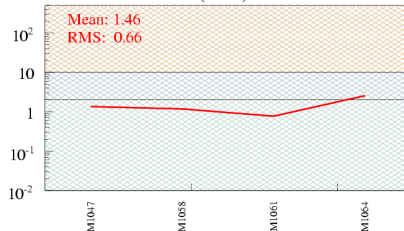
Current at 150 V (in μA) at $T = 17^\circ\text{C}$ and $T = -10^\circ\text{C}$

I150V at $T = -10^\circ\text{C}$ (ATC)



recalculated

I150V at $T = 17^\circ\text{C}$ (ATC)

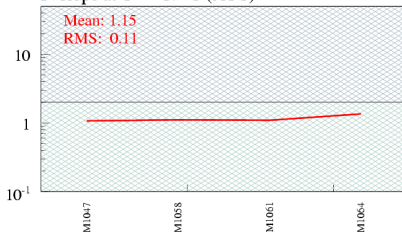


measured

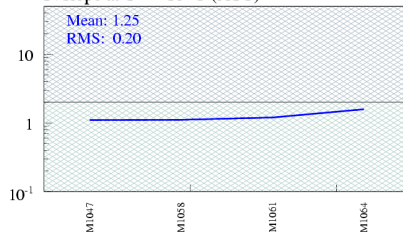
Slope of IV-Curve

Slope of IV-Curve at $T = 17^{\circ}\text{C}$ and $T = -10^{\circ}\text{C}$

IVslope at $T = 17^{\circ}\text{C}$ (ATC)

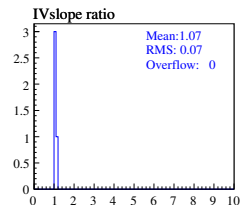
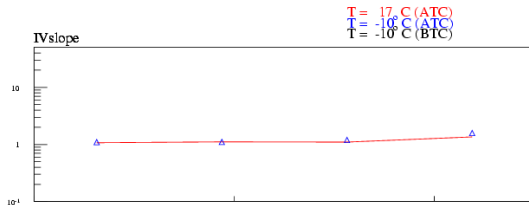
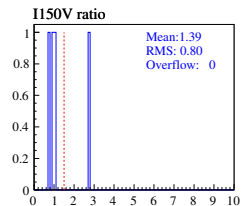
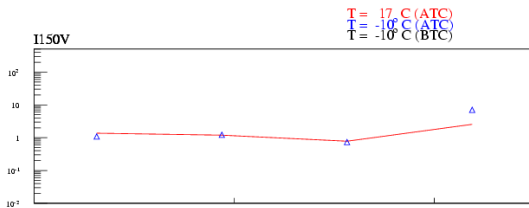


IVslope at $T = -10^{\circ}\text{C}$ (ATC)



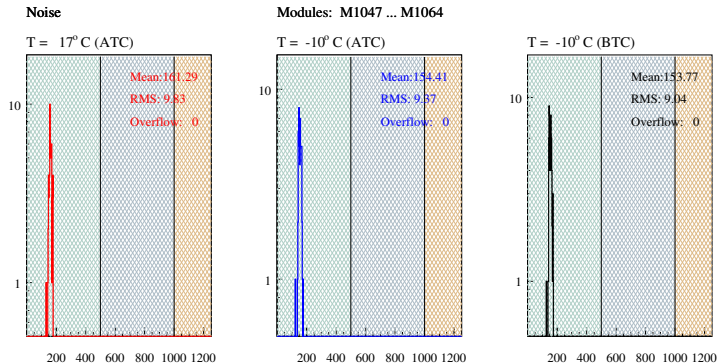
Current recalculation to $T = 17^{\circ}\text{C}$

Cross check of recalculated values with measured values



Noise

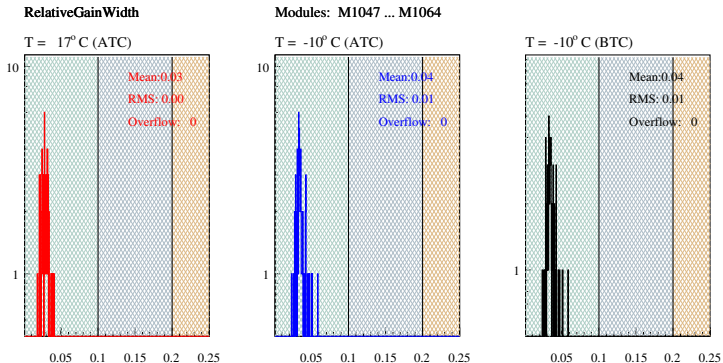
MeanNoise of chips



Noise in e^-

Relative Gain Width

RelativeGainWidth of chips



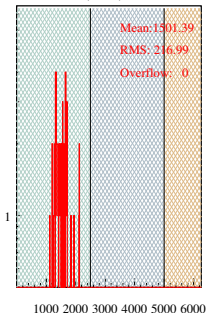
Rel. Gain Width in %

Pedestal Spread

PedestalSpread of chips

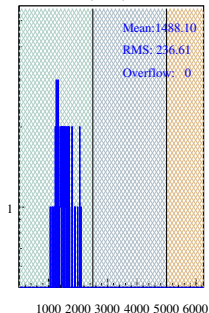
PedestalSpread

T = 17° C (ATC)

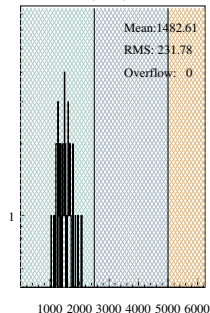


Modules: M1047 ... M1064

T = -10° C (ATC)



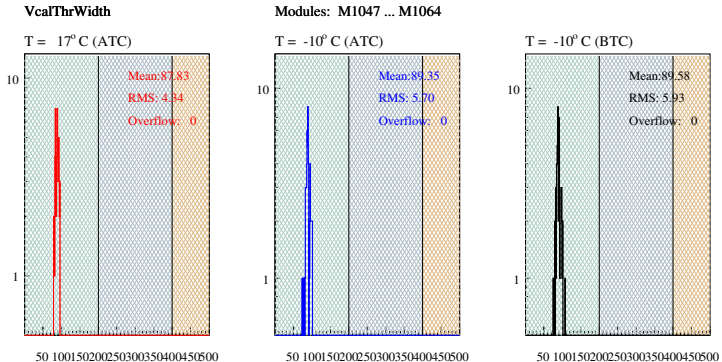
T = -10° C (BTC)



Pedestal Spread in e^-

Vcal Threshold Width

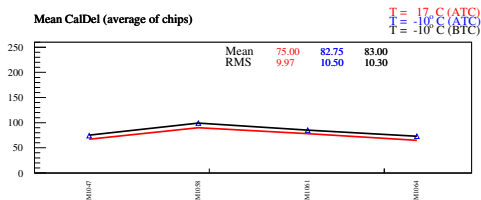
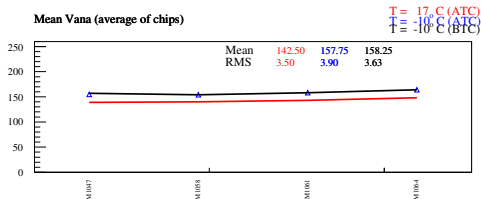
VcalThresholdWidth of chips



Vcal Thr. Width in e^-

Operational parameters I

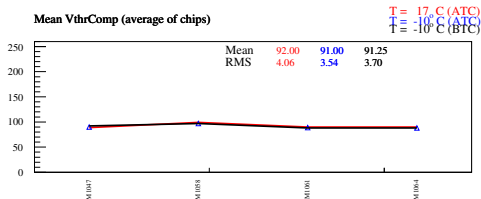
Mean DACs I



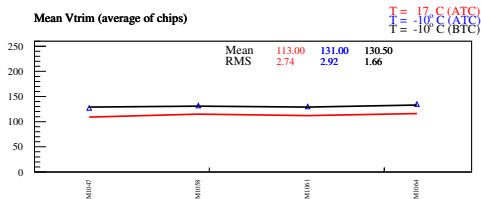
Operational parameters II

Mean DACs II

Mean VthrComp (average of chips)



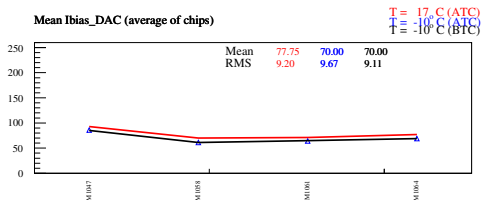
Mean Vtrim (average of chips)



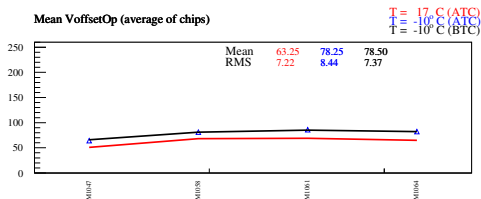
Operational parameters III

Mean DACs III

Mean Ibias_DAC (average of chips)

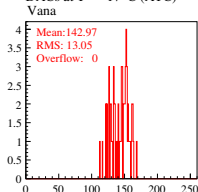


Mean VoffsetOp (average of chips)

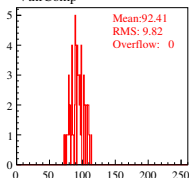


Operational parameters at $T = +17^{\circ}\text{C}$ (ATC)

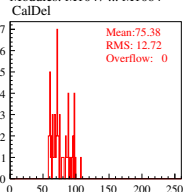
DAC distribution (of chips)

DACs at $T = 17^{\circ}\text{C}$ (ATC)

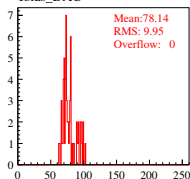
VthrComp



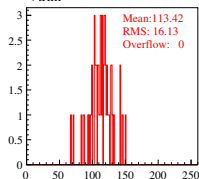
Modules: M1047 ... M1064



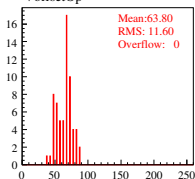
Ibias_DAC



Vtrim

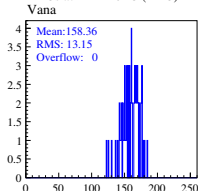


VoffsetOp

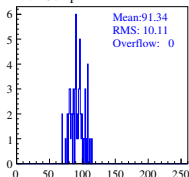


Operational parameters at $T = -10^{\circ}\text{C}$ (ATC)

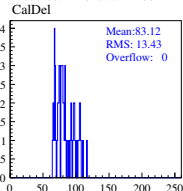
DAC distribution (of chips)

DACs at $T = -10^{\circ}\text{C}$ (ATC)

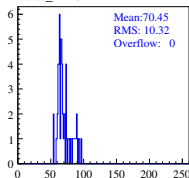
VthrComp



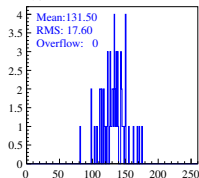
Modules: M1047 ... M1064



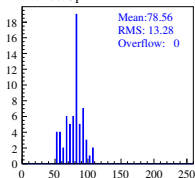
Ibias_DAC



Vtrim

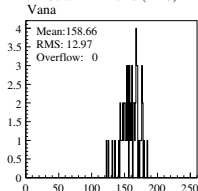


VoffsetOp

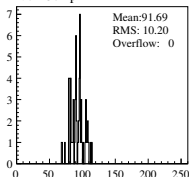


Operational parameters at $T = +17^{\circ}\text{C}$ (BTC)

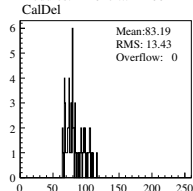
DAC distribution (of chips)

DACs at $T = -10^{\circ}\text{C}$ (BTC)

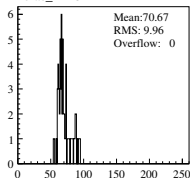
VthrComp



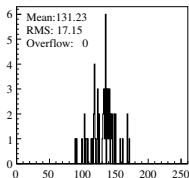
Modules: M1047 ... M1064



Ibias_DAC



Vtrim



VoffsetOp

