

BPIX Module Testing Status - Week 24

18th June 2007

Production overview

Production Status: 699 modules produced (618 full/ 81 half)

- 438/103 graded as A/B → 88% || 62/12 → 91%
- 77 graded as C → 12% || 7 → 9%

Module Testing Report of Week 24:

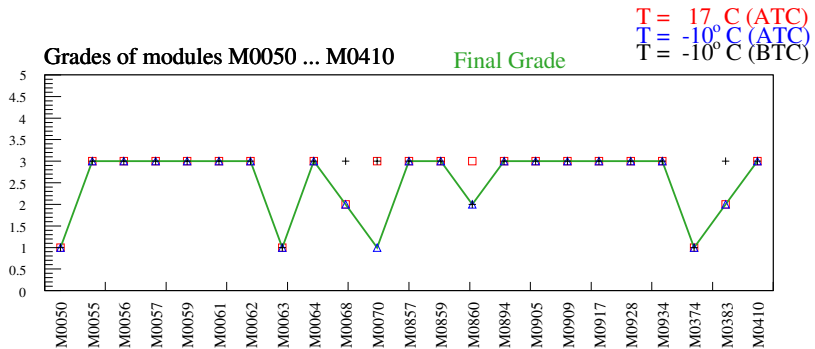
- 23 modules fully tested and therm. cycled (0 retested)

	Modules (20)			Halfmodules (3)		
Grade	A	B	C	A	B	C
T = -10° C, BTC*	17	1	2	2	0	1
T = -10° C, ATC	15	2	3	1	1	1
T = +17° C, ATC	17	1	2	1	1	1
Final Grade	15	2	3	1	1	1

- no retests with new DAC settings

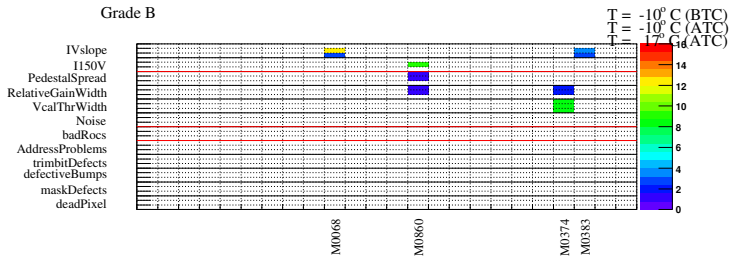
*without IV-criteria

Production summary

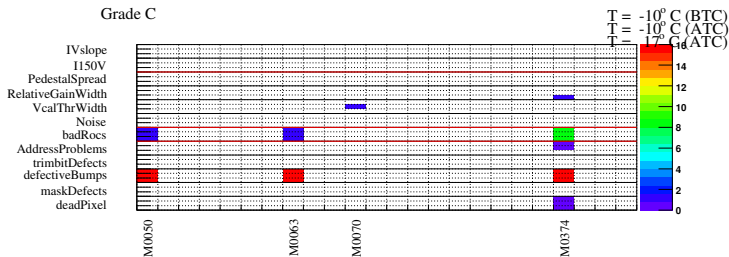


Module Failures Overview

Grade B



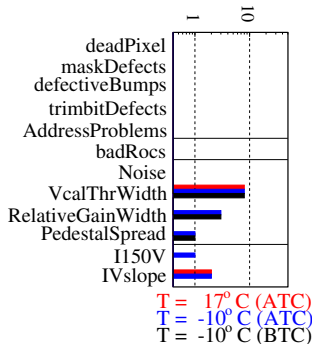
Grade C



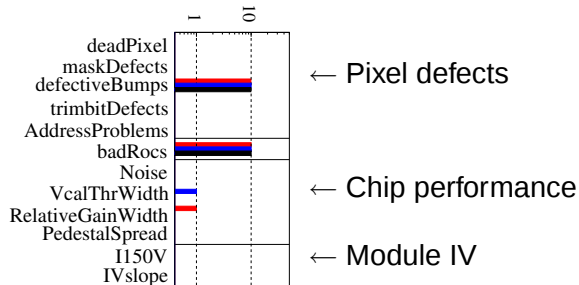
Production quality

Chip Failures

Grade B
Grade B



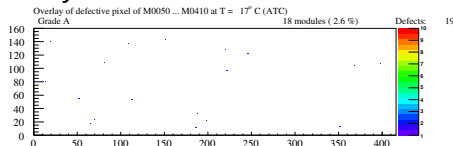
Grade C
Grade C



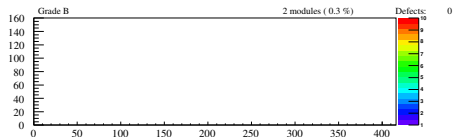
Defective pixel $T = 17^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = +17^{\circ}\text{C}$ (ATC)

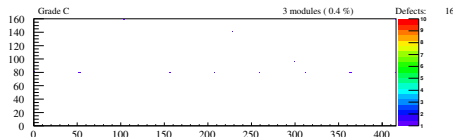
Grade A
(18 modules)



Grade B
(2 modules)



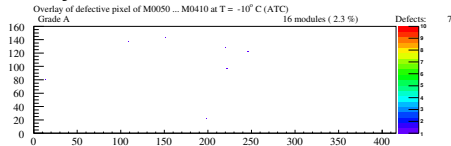
Grade C
(3 modules)



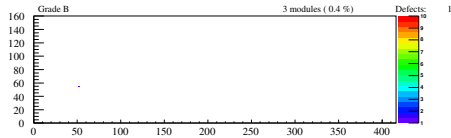
Defective pixel $T = -10^0\text{C}$ (ATC)

Overlay of all fully tested modules at $T = -10^0\text{C}$ (ATC)

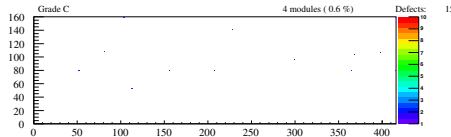
Grade A
(16 modules)



Grade B
(3 modules)



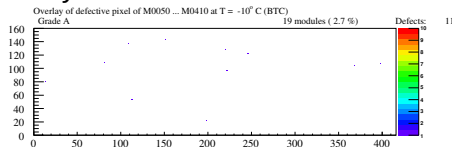
Grade C
(4 modules)



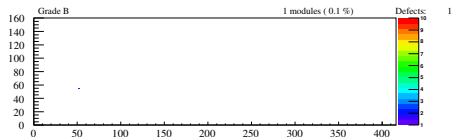
Defective pixel $T = -10^0\text{C}$ (BTC)

Overlay of all fully tested modules at $T = -10^0\text{C}$ (BTC)

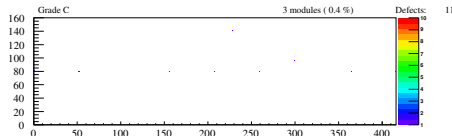
Grade A
(19 modules)



Grade B
(1 modules)



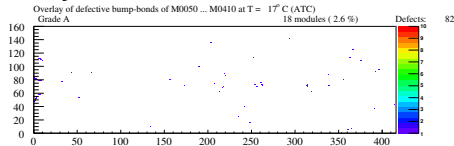
Grade C
(3 modules)



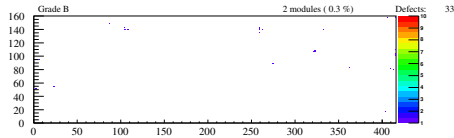
Defective bump-bonds $T = 17^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = +17^{\circ}\text{C}$ (ATC)

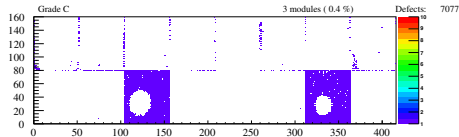
Grade A
(18 modules)



Grade B
(2 modules)



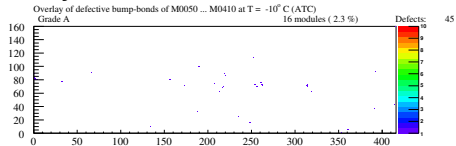
Grade C
(3 modules)



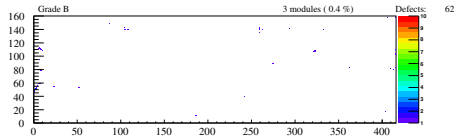
Defective bump-bonds $T = -10^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (ATC)

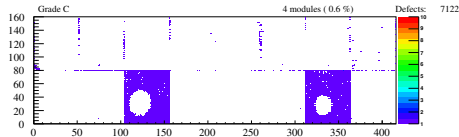
Grade A
(16 modules)



Grade B
(3 modules)



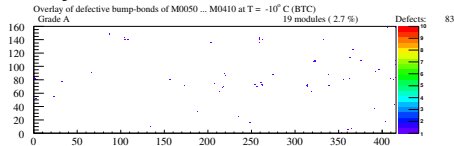
Grade C
(4 modules)



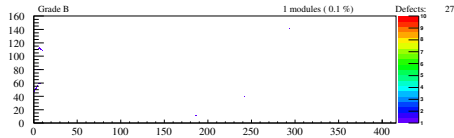
Defective bump-bonds $T = -10^{\circ}\text{C}$ (BTC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (BTC)

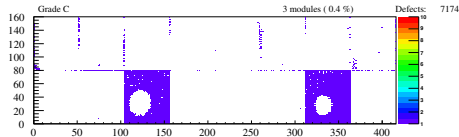
Grade A
(19 modules)



Grade B
(1 modules)



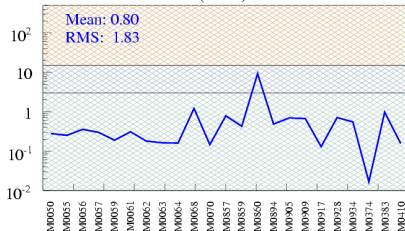
Grade C
(3 modules)



Current at 150 V

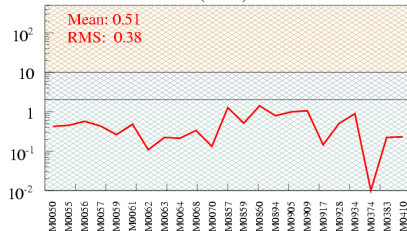
Current at 150 V (in μA) at $T = 17^\circ\text{C}$ and $T = -10^\circ\text{C}$

I150V at T = -10°C (ATC)



recalculated

I150V at T = 17°C (ATC)

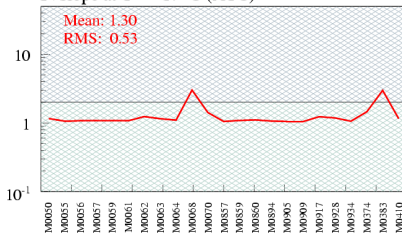


measured

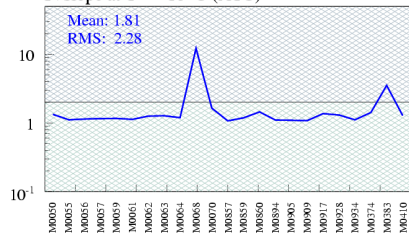
Slope of IV-Curve

Slope of IV-Curve at $T = 17^{\circ}\text{C}$ and $T = -10^{\circ}\text{C}$

IVslope at $T = 17^{\circ}\text{C}$ (ATC)

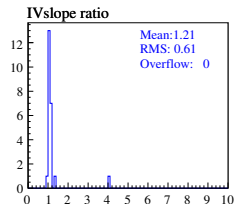
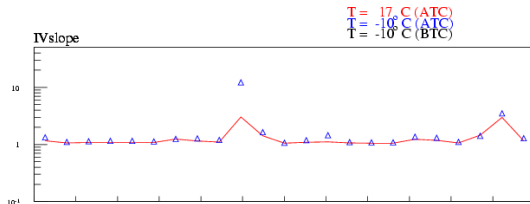
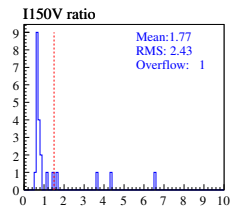
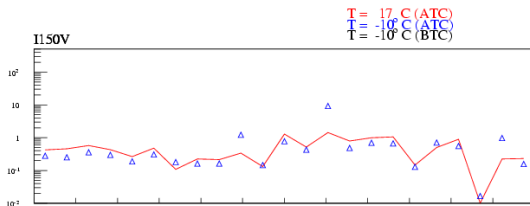


IVslope at $T = -10^{\circ}\text{C}$ (ATC)



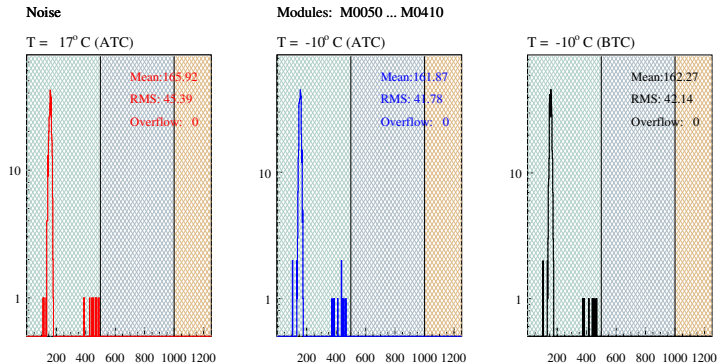
Current recalculation to $T = 17^{\circ}\text{C}$

Cross check of recalculated values with measured values



Noise

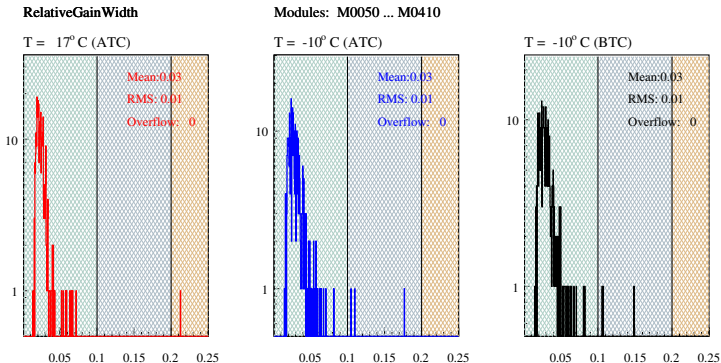
MeanNoise of chips



Noise in e^-

Relative Gain Width

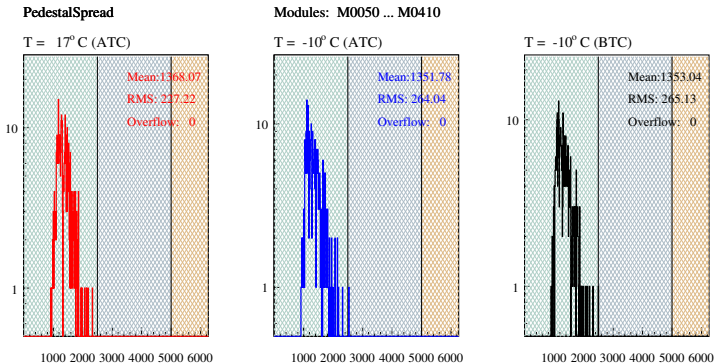
RelativeGainWidth of chips



Rel. Gain Width in %

Pedestal Spread

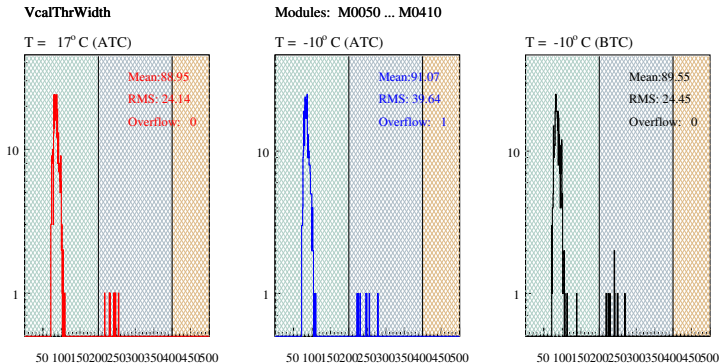
PedestalSpread of chips



Pedestal Spread in e^-

Vcal Threshold Width

VcalThresholdWidth of chips

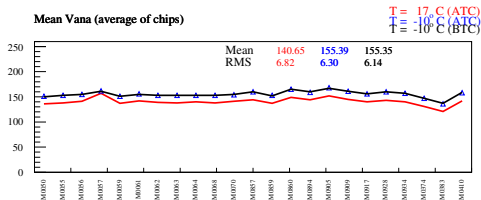


Vcal Thr. Width in e^-

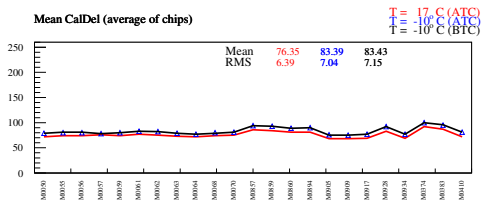
Operational parameters I

Mean DACs I

Mean Vana (average of chips)



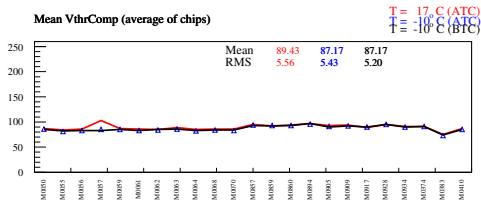
Mean CalDel (average of chips)



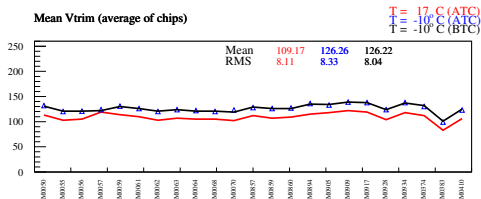
Operational parameters II

Mean DACs II

Mean VthrComp (average of chips)



Mean Vtrim (average of chips)

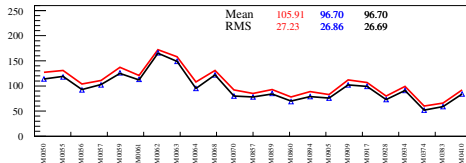


Operational parameters III

Mean DACs III

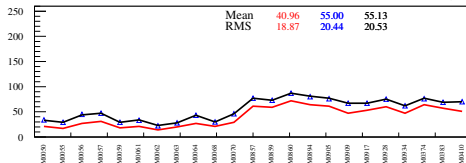
Mean Ibias_DAC (average of chips)

T = 17° C (ATC)
T = -10° C (ATC)
T = -10° C (BTC)



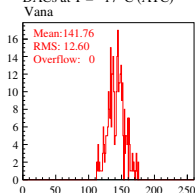
Mean VoffsetOp (average of chips)

T = 17° C (ATC)
T = -10° C (ATC)
T = -10° C (BTC)

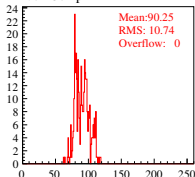


Operational parameters at $T = +17^{\circ}\text{C}$ (ATC)

DAC distribution (of chips)

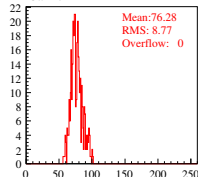
DACs at $T = 17^{\circ}\text{C}$ (ATC)

VthrComp

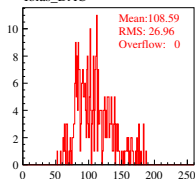


Modules: M0050 ... M0410

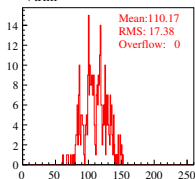
CalDel



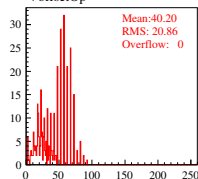
Ibias_DAC



Vtrim

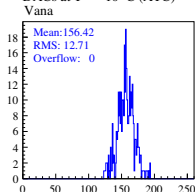


VoffsetOp

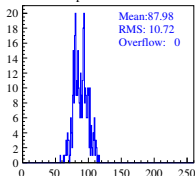


Operational parameters at $T = -10^{\circ}\text{C}$ (ATC)

DAC distribution (of chips)

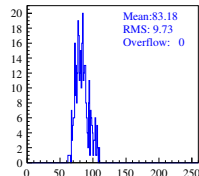
DACs at $T = -10^{\circ}\text{C}$ (ATC)

VthrComp

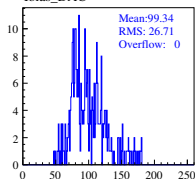


Modules: M0050 ... M0410

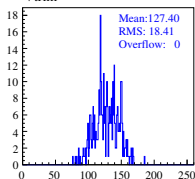
CalDel



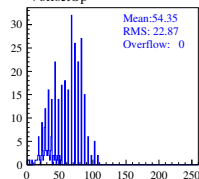
Ibias_DAC



Vtrim

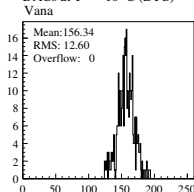


VoffsetOp

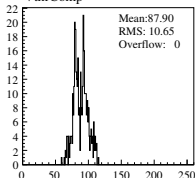


Operational parameters at $T = +17^{\circ}\text{C}$ (BTC)

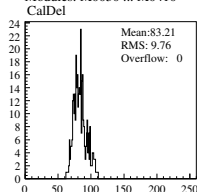
DAC distribution (of chips)

DACs at $T = -10^{\circ}\text{C}$ (BTC)

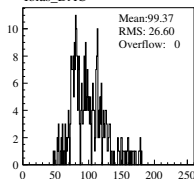
VthrComp



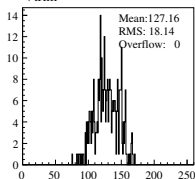
Modules: M0050 ... M0410



Ibias_DAC



Vtrim



VoffsetOp

