BPIX Module Testing Status - Week 17

4th May 2007

Production overview

Production Status: 616 modules produced (538 full/ 78 half))

- 375/92 graded as A/B → 87% || 61/11 → 92%
- 71 graded as C → 13% || 6 → 8%

Module Testing Report of Week 17:

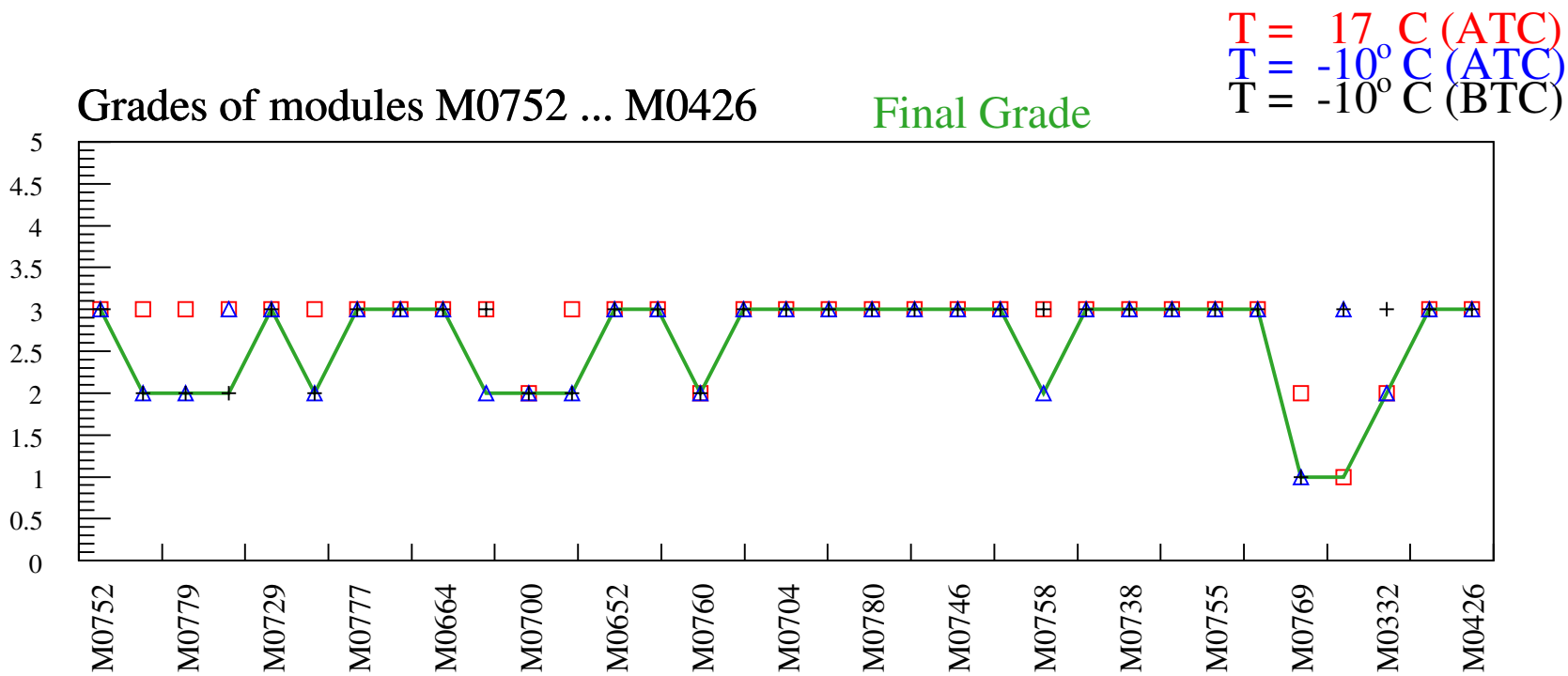
- 33 modules fully tested and therm. cycled (0 retested)

	Modules (29)			*Halfmodules* (4)		
Grade	**A**	**B**	**C**	**A**	**B**	**C**
T = -10^o C, BTC*	21	7	1	4	0	0
T = -10^o C, ATC	20	8	1	3	1	0
T = $+17^o$ C, ATC	26	3	0	2	1	1
Final Grade	19	9	1	2	1	1

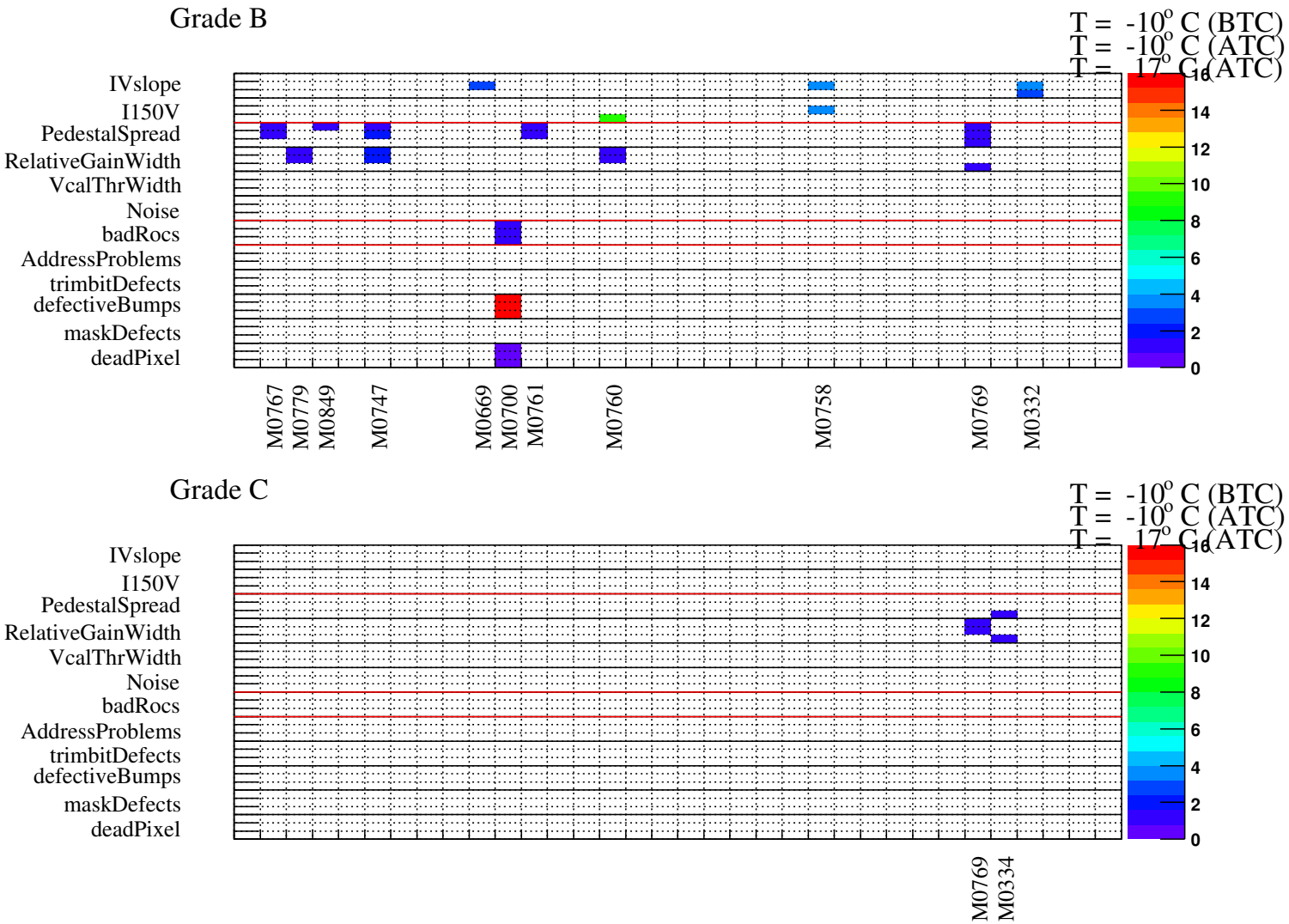
- no retests with new DAC settings

*without IV-criteria

Production summary

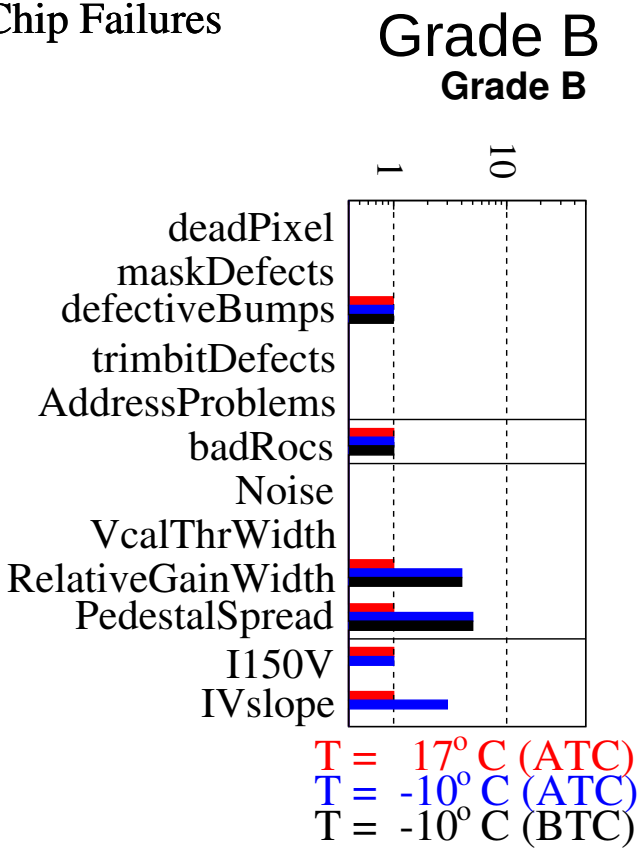


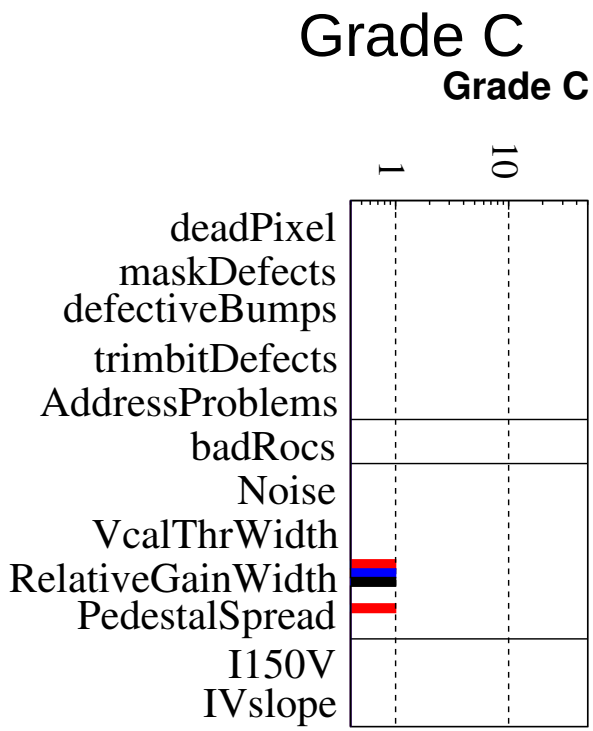
Module Failures Overview



Production quality

Chip Failures





← Pixel defects

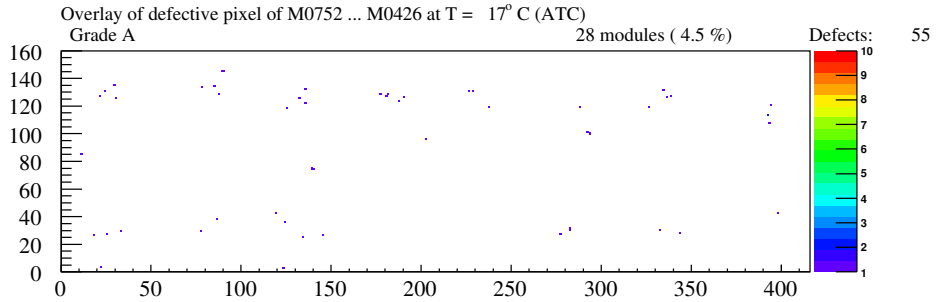
← Chip performance

← Module IV

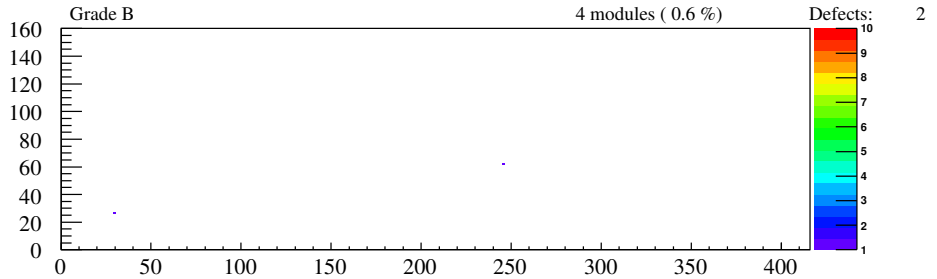
Defective pixel $T = 17^{o}C$ (ATC)

Overlay of all fully tested modules at T = $+17^{o}$ C (ATC)

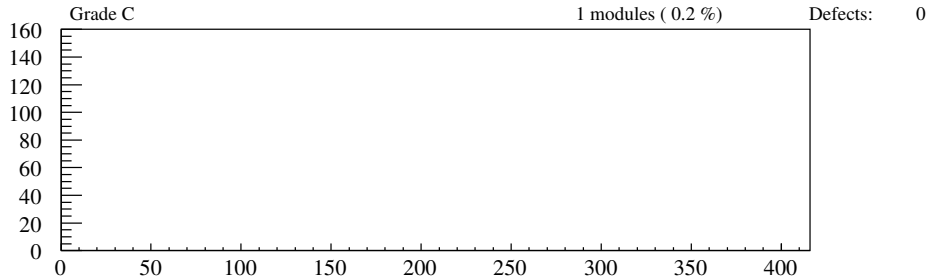
Grade A
(28 modules)



Grade B
(4 modules)



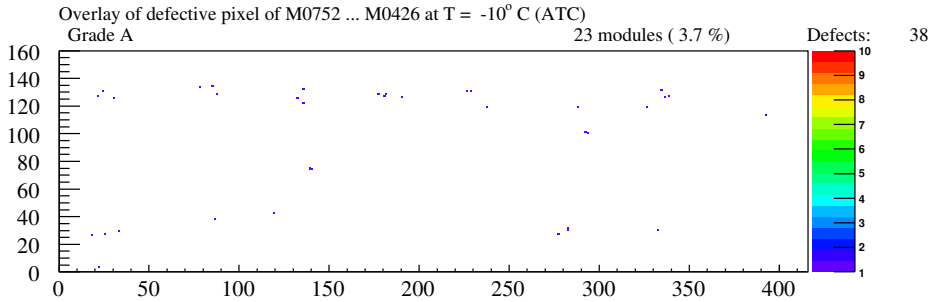
Grade C
(1 modules)



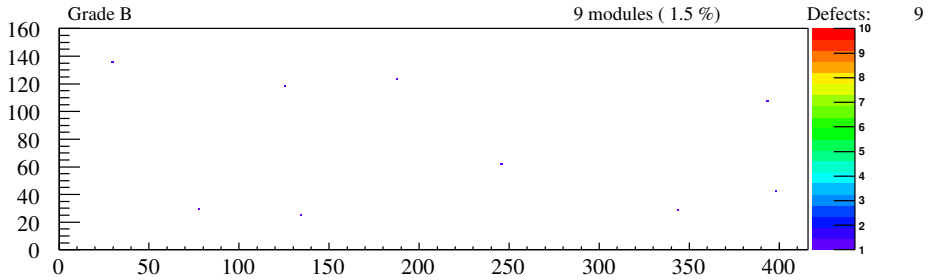
Defective pixel $T = -10^oC$ (ATC)

Overlay of all fully tested modules at T = -10^o C (ATC)

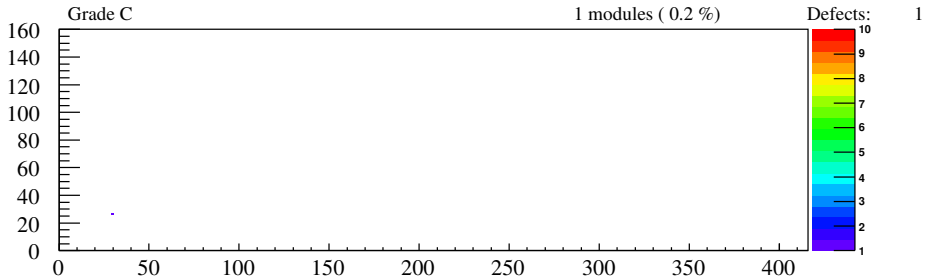
Grade A
(23 modules)



Grade B
(9 modules)



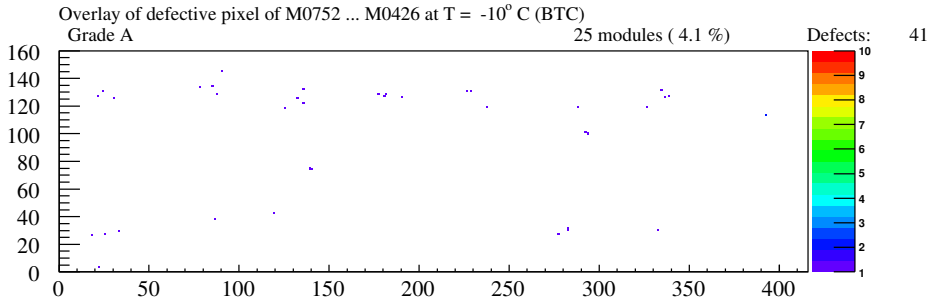
Grade C
(1 modules)



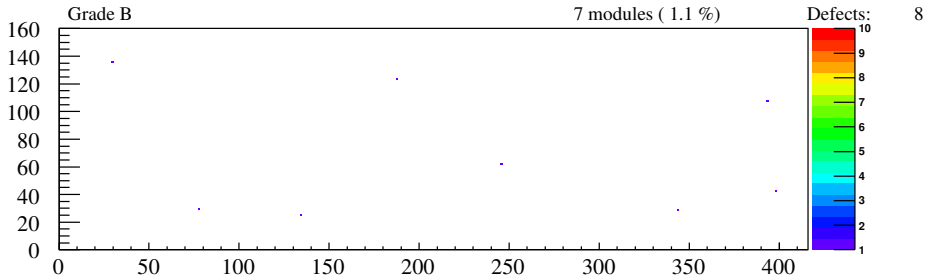
Defective pixel $T = -10^{o}C$ (BTC)

Overlay of all fully tested modules at T = -10^{o} C (BTC)

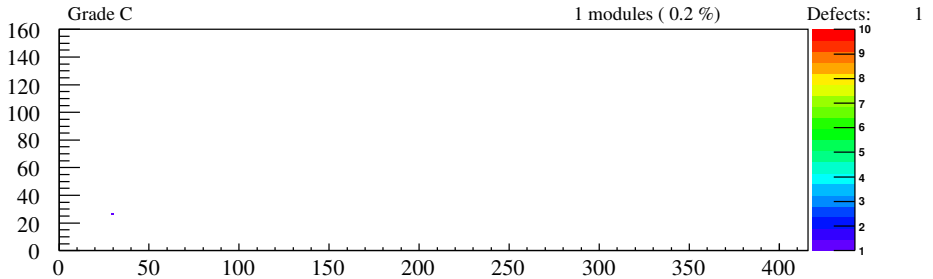
Grade A
(25 modules)



Grade B
(7 modules)



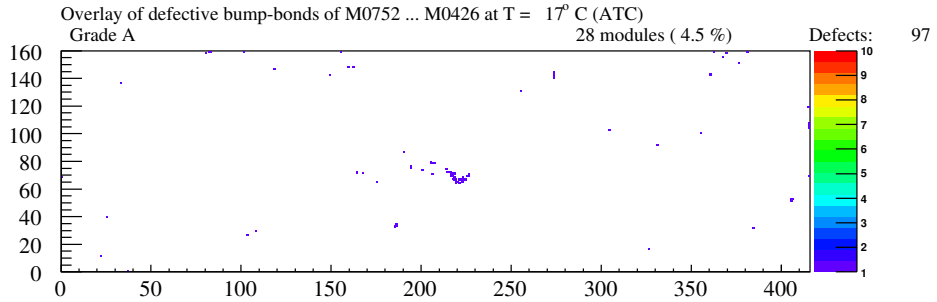
Grade C
(1 modules)



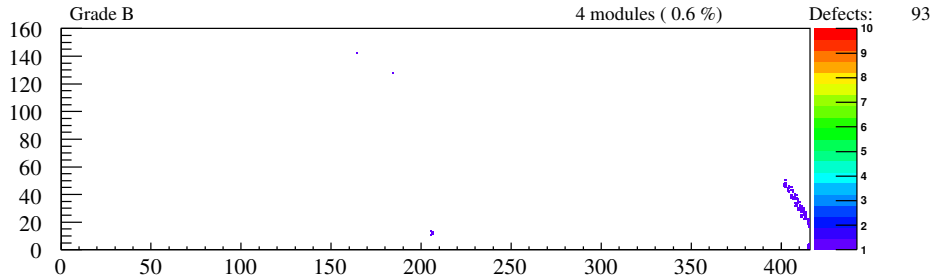
Defective bump-bonds $T = 17^oC$ (ATC)

Overlay of all fully tested modules at T = $+17^o$ C (ATC)

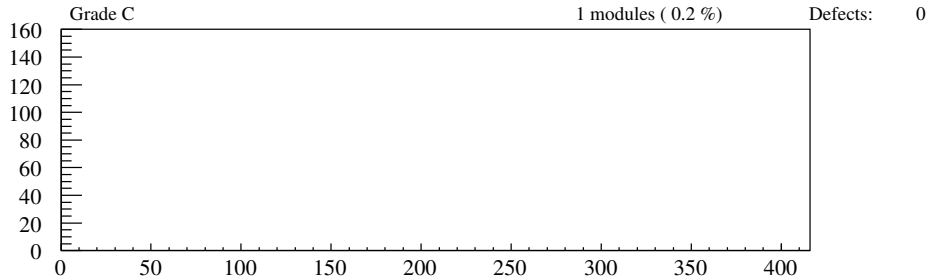
Grade A
(28 modules)



Grade B
(4 modules)



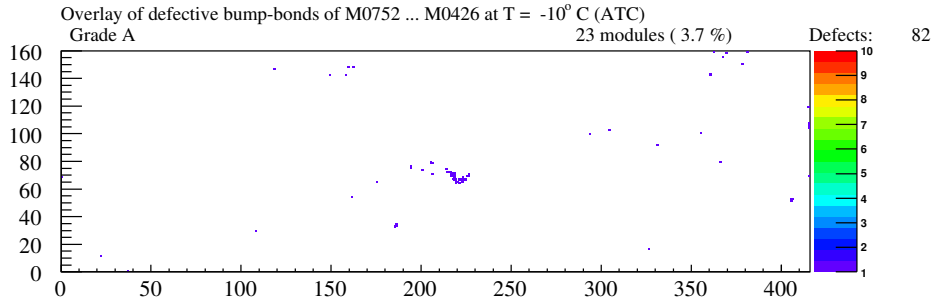
Grade C
(1 modules)



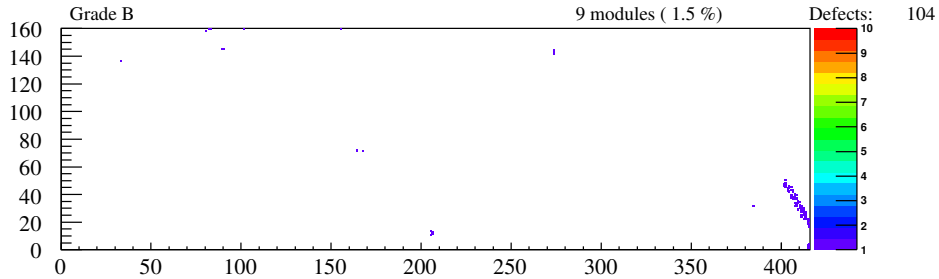
Defective bump-bonds $T = -10^{o}C$ (ATC)

Overlay of all fully tested modules at T = -10^{o} C (ATC)

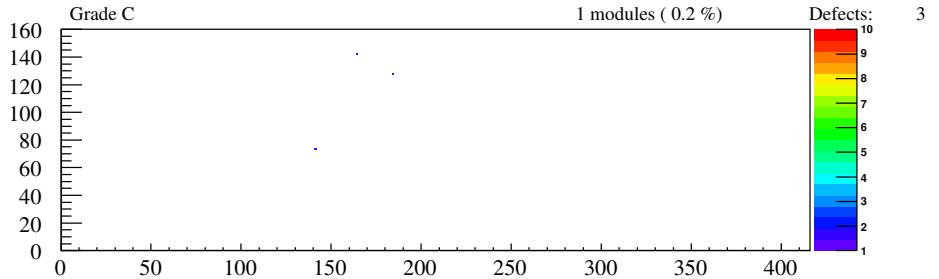
Grade A
(23 modules)



Grade B
(9 modules)



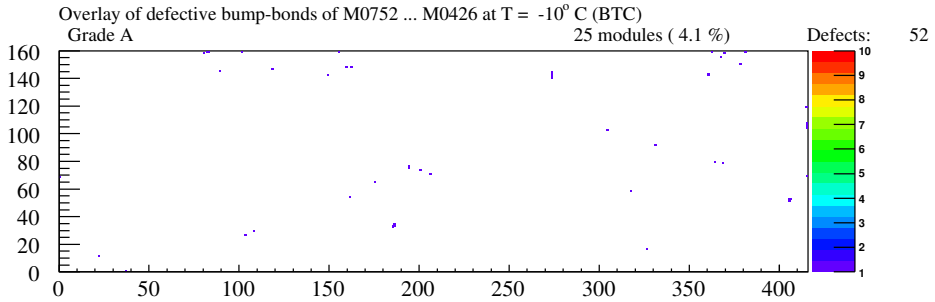
Grade C
(1 modules)



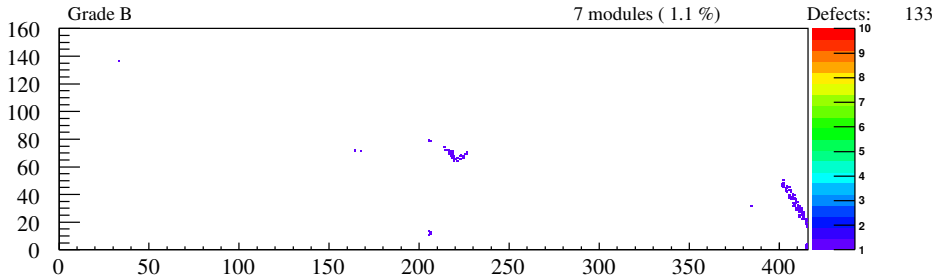
Defective bump-bonds $T = -10^{o}C$ (BTC)

Overlay of all fully tested modules at T = -10^{o} C (BTC)

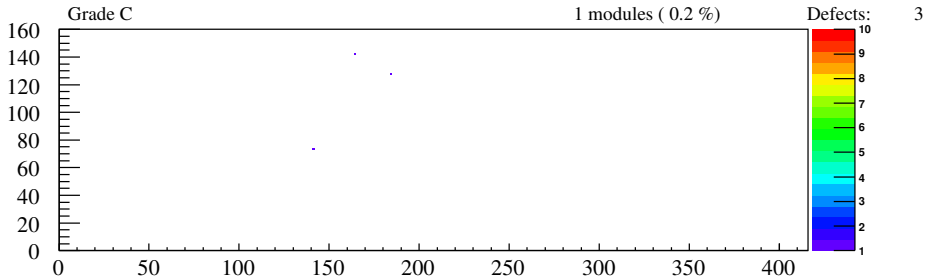
Grade A
(25 modules)



Grade B
(7 modules)

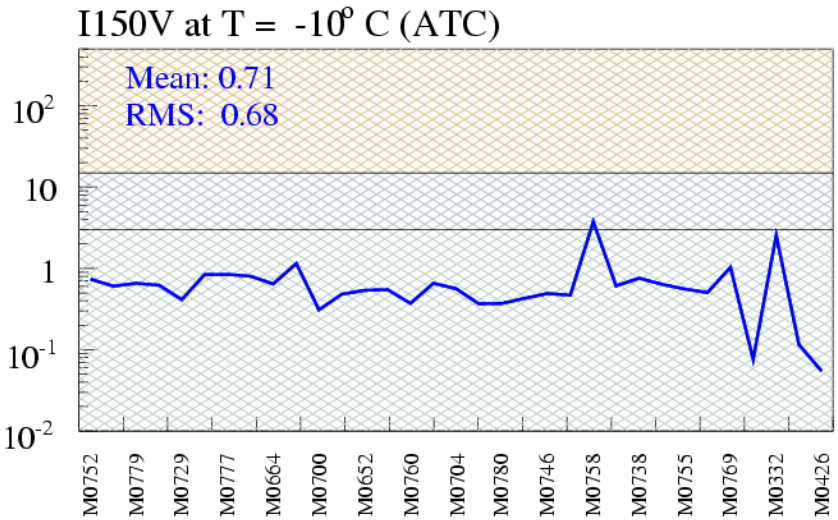


Grade C
(1 modules)

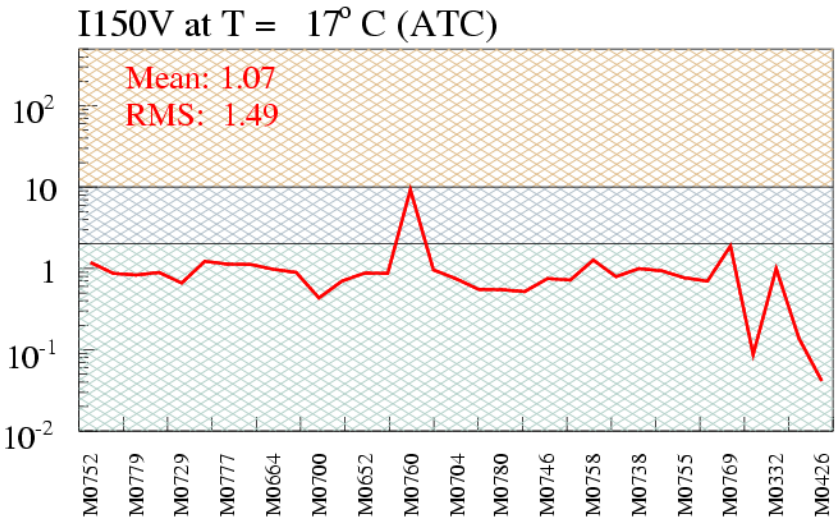


Current at 150 V

Current at 150 V (in μA) at $T = 17^oC$ and $T = -10^oC$



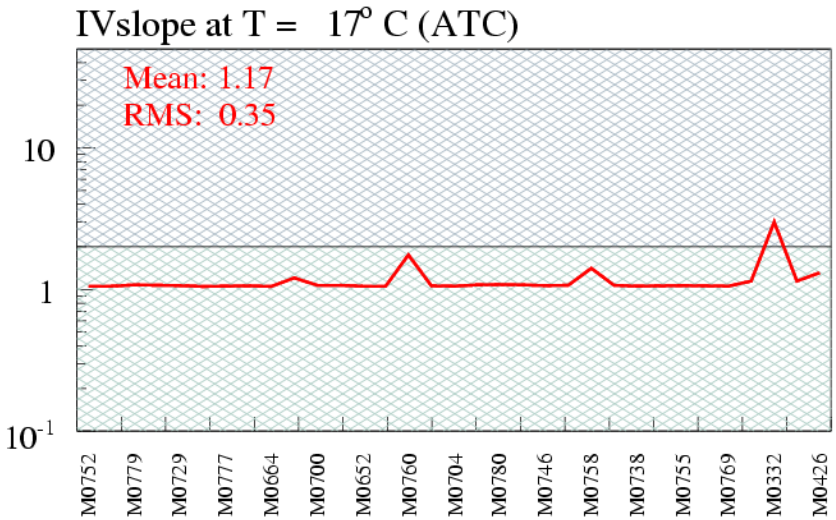
recalculated

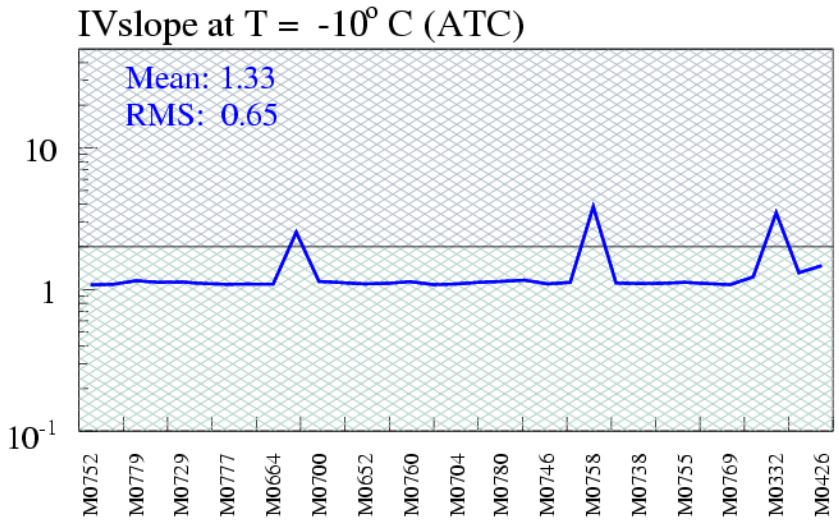


measured

Slope of IV-Curve

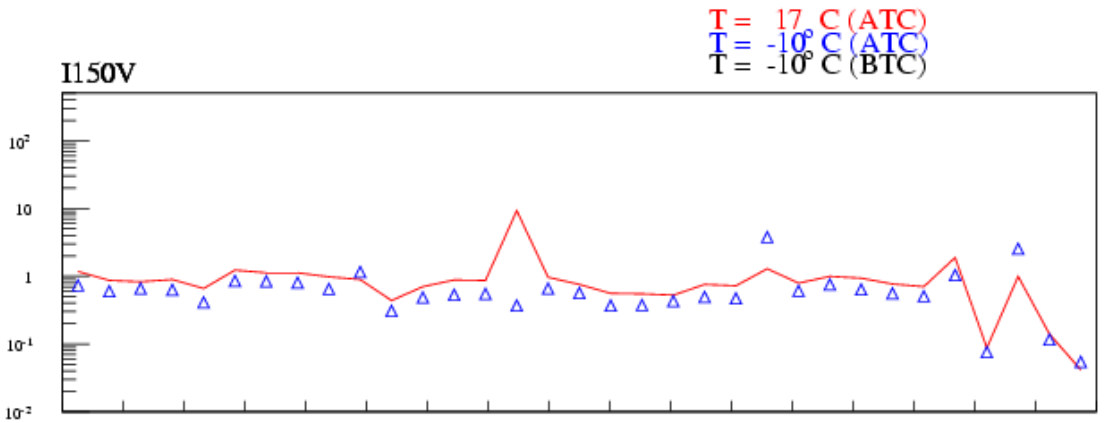
Slope of IV-Curveat $T = 17^oC$ and $T = -10^oC$

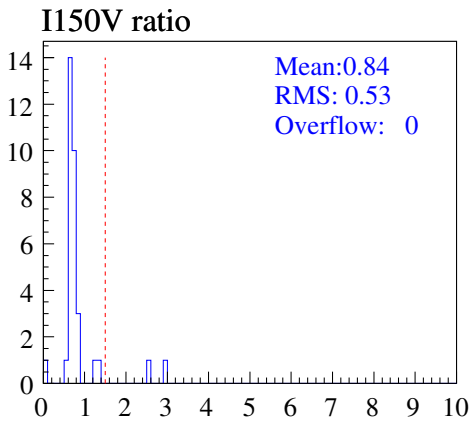


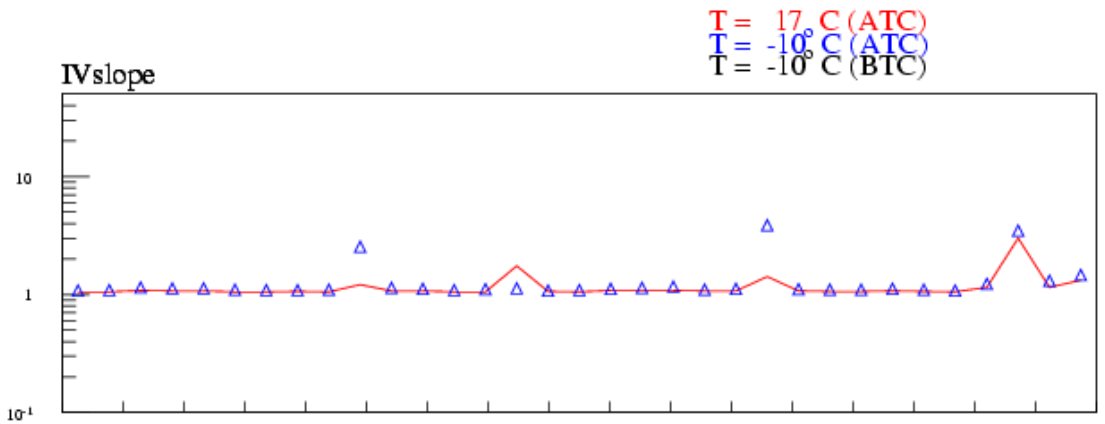


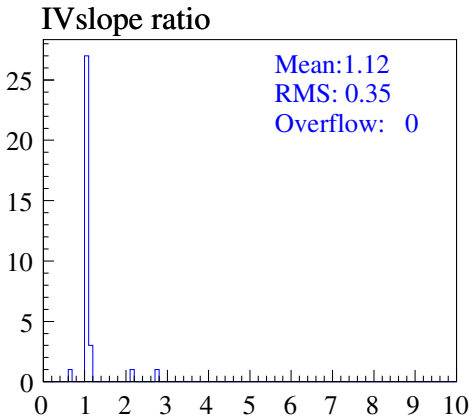
Current recalculation to $T = 17^oC$

Cross check of recalculated values with measured values



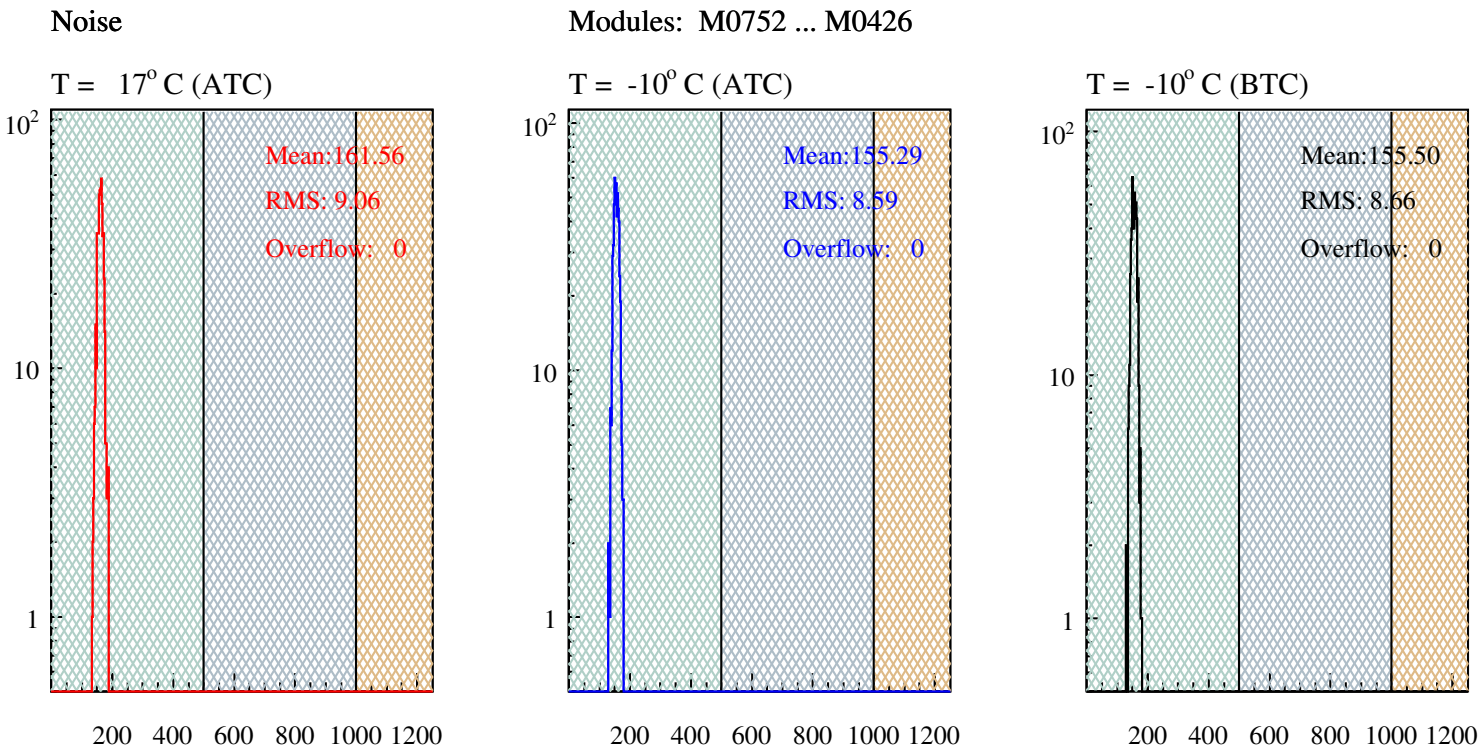






Noise

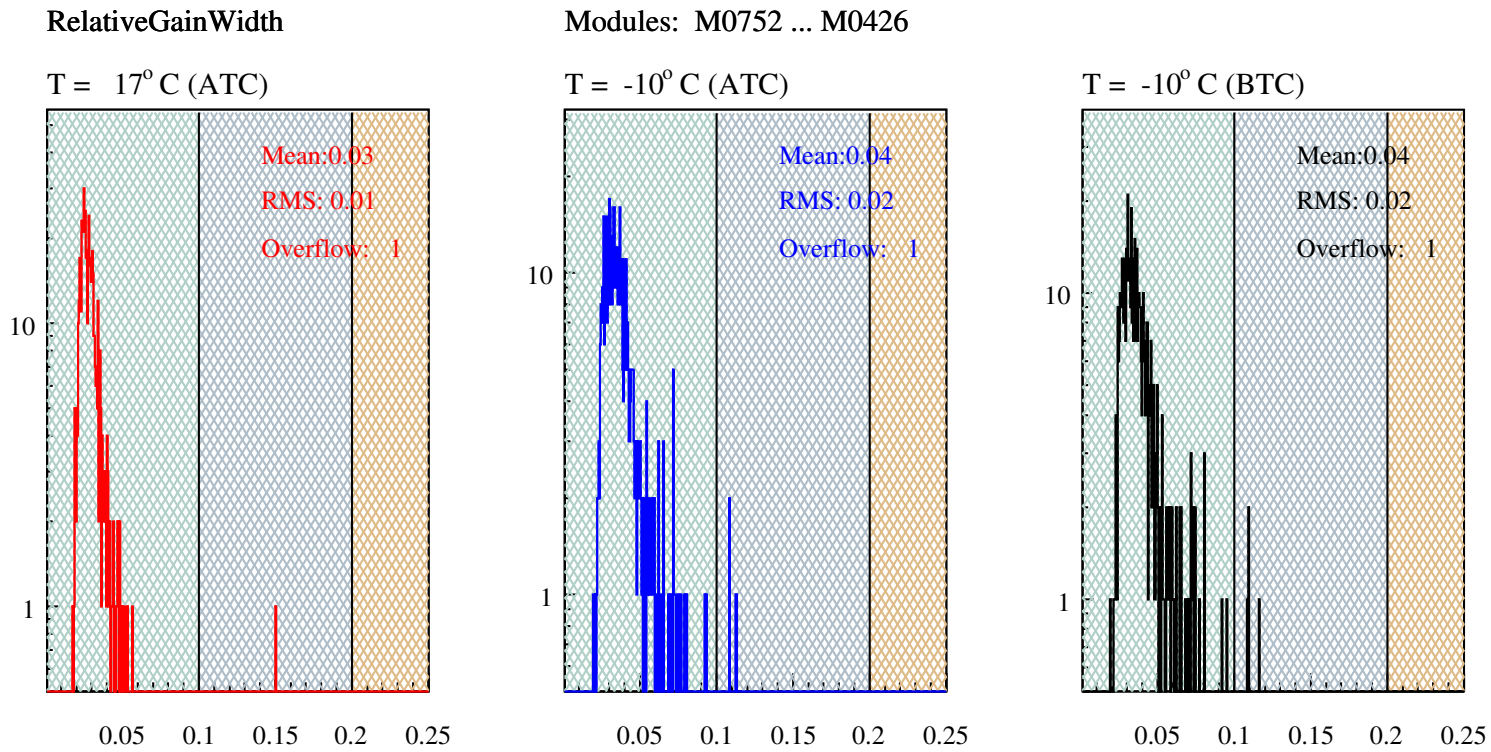
MeanNoise of chips



Noise in e^-

Relative Gain Width

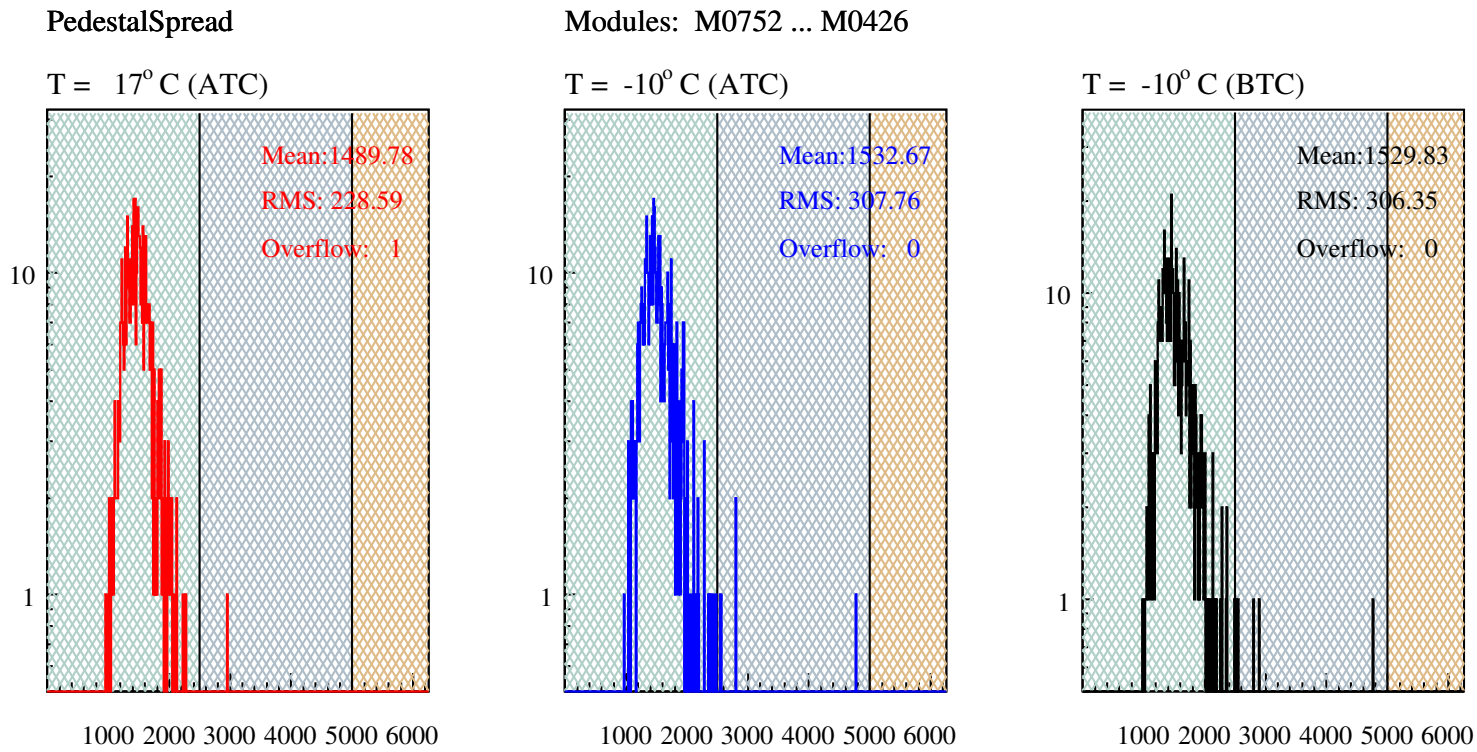
RelativeGainWidth of chips



Rel. Gain Width in %

Pedestal Spread

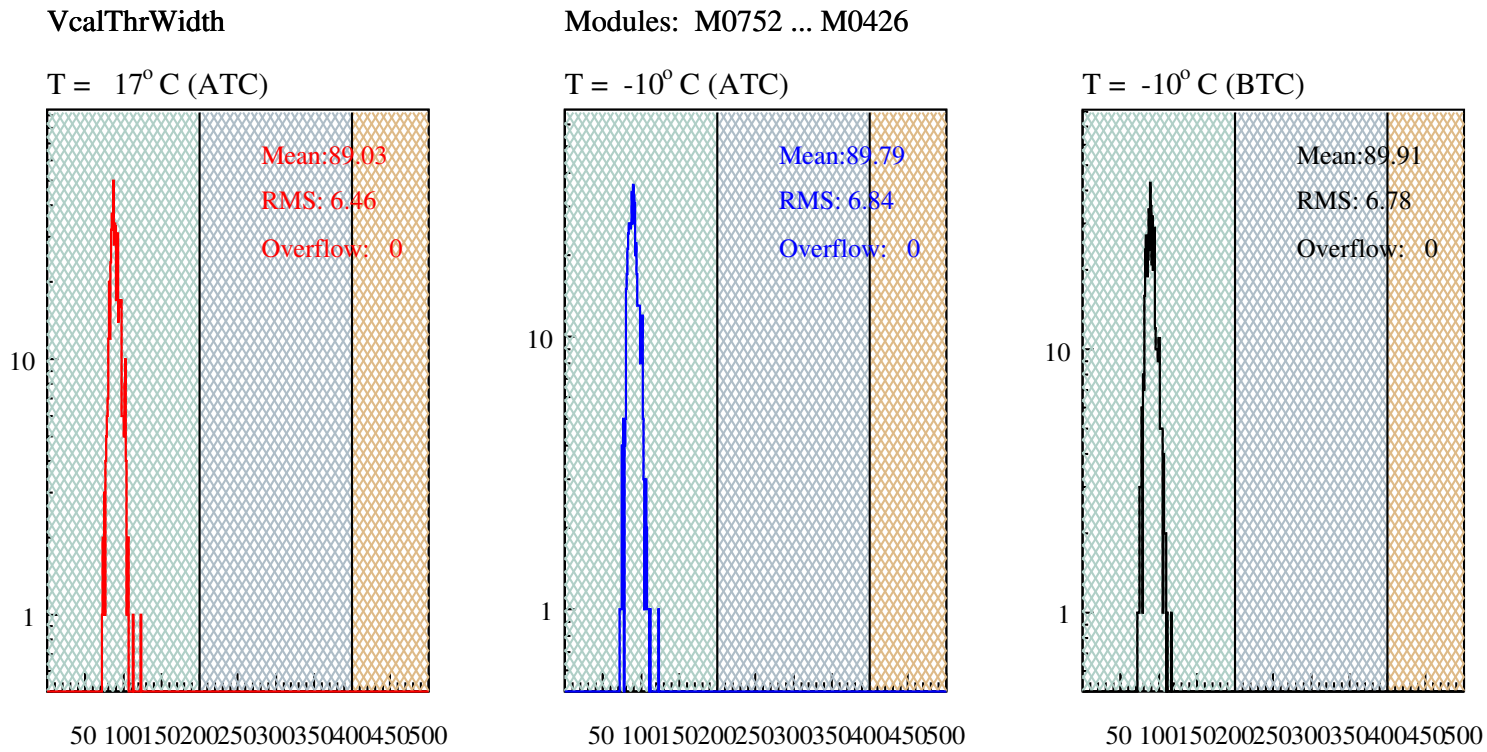
PedestalSpread of chips



Pedestal Spread in e^-

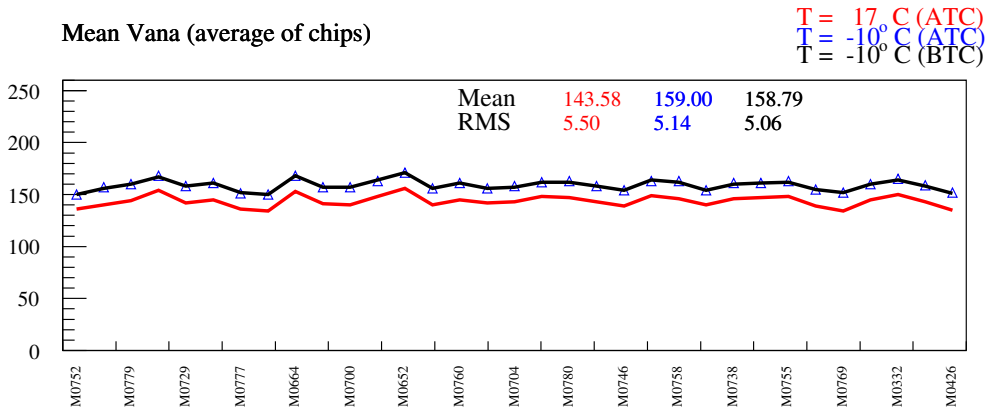
Vcal Threshold Width

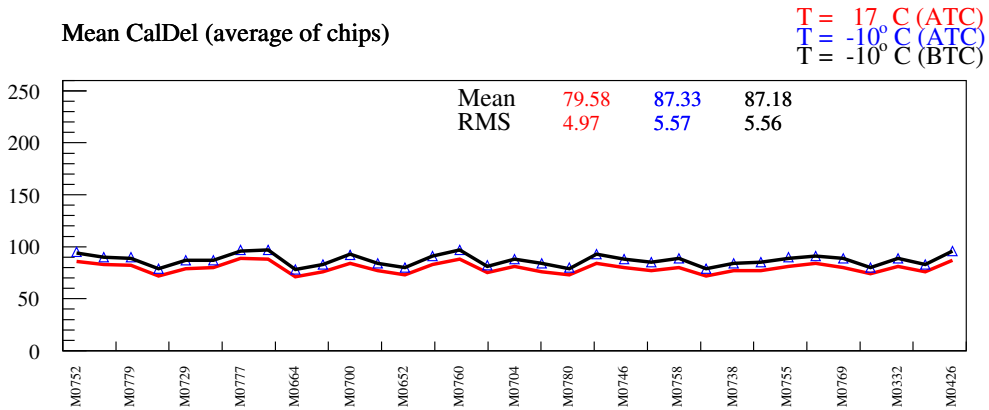
VcalThresholdWidth of chips



Operational parameters I

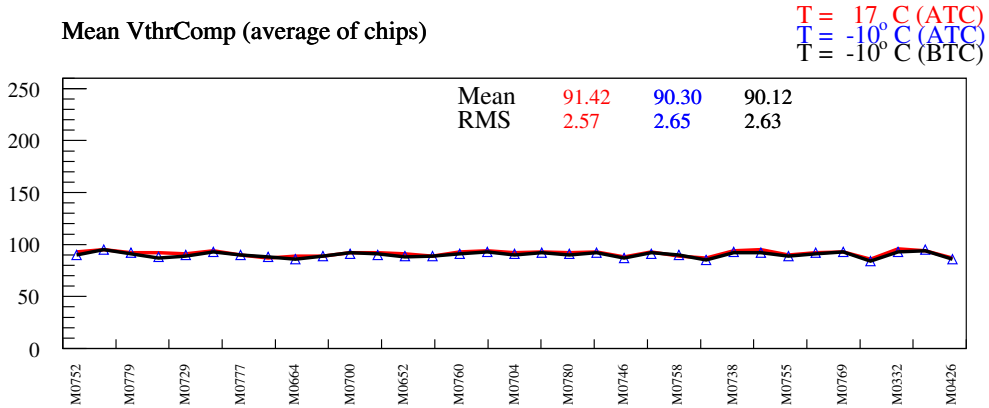
Mean DACs I

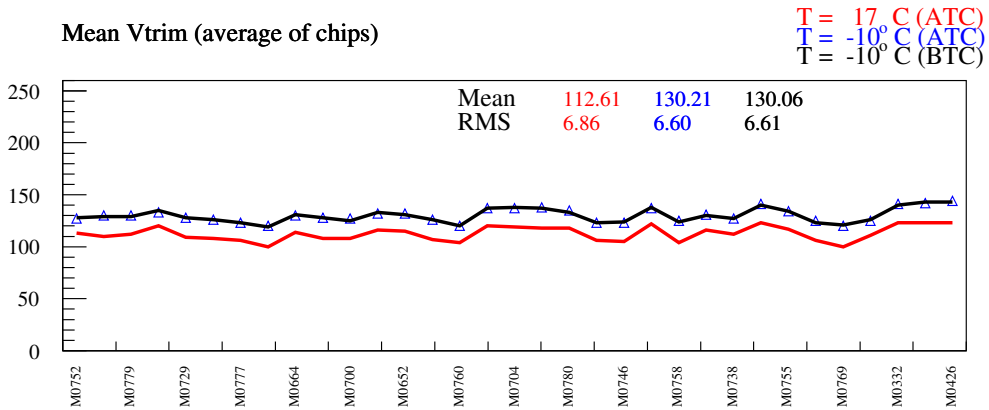




Operational parameters II

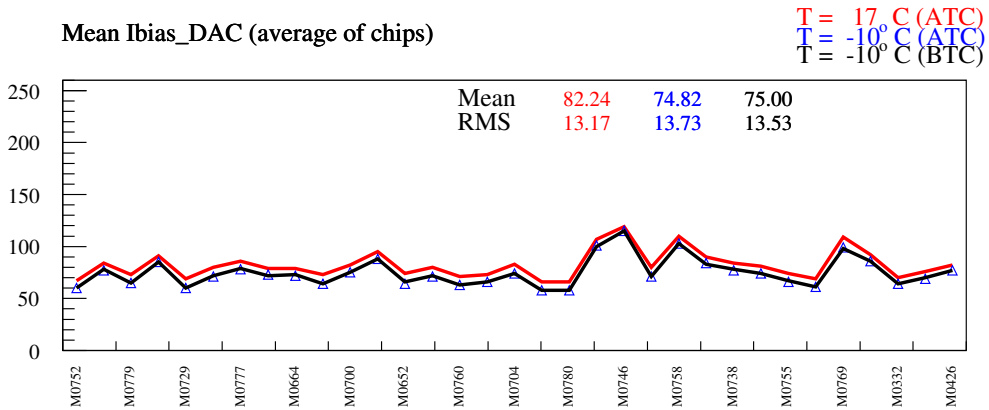
Mean DACs II

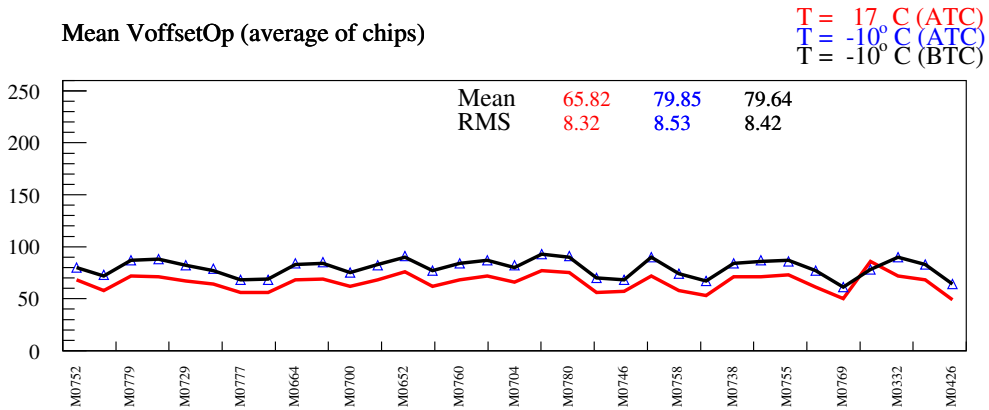




Operational parameters III

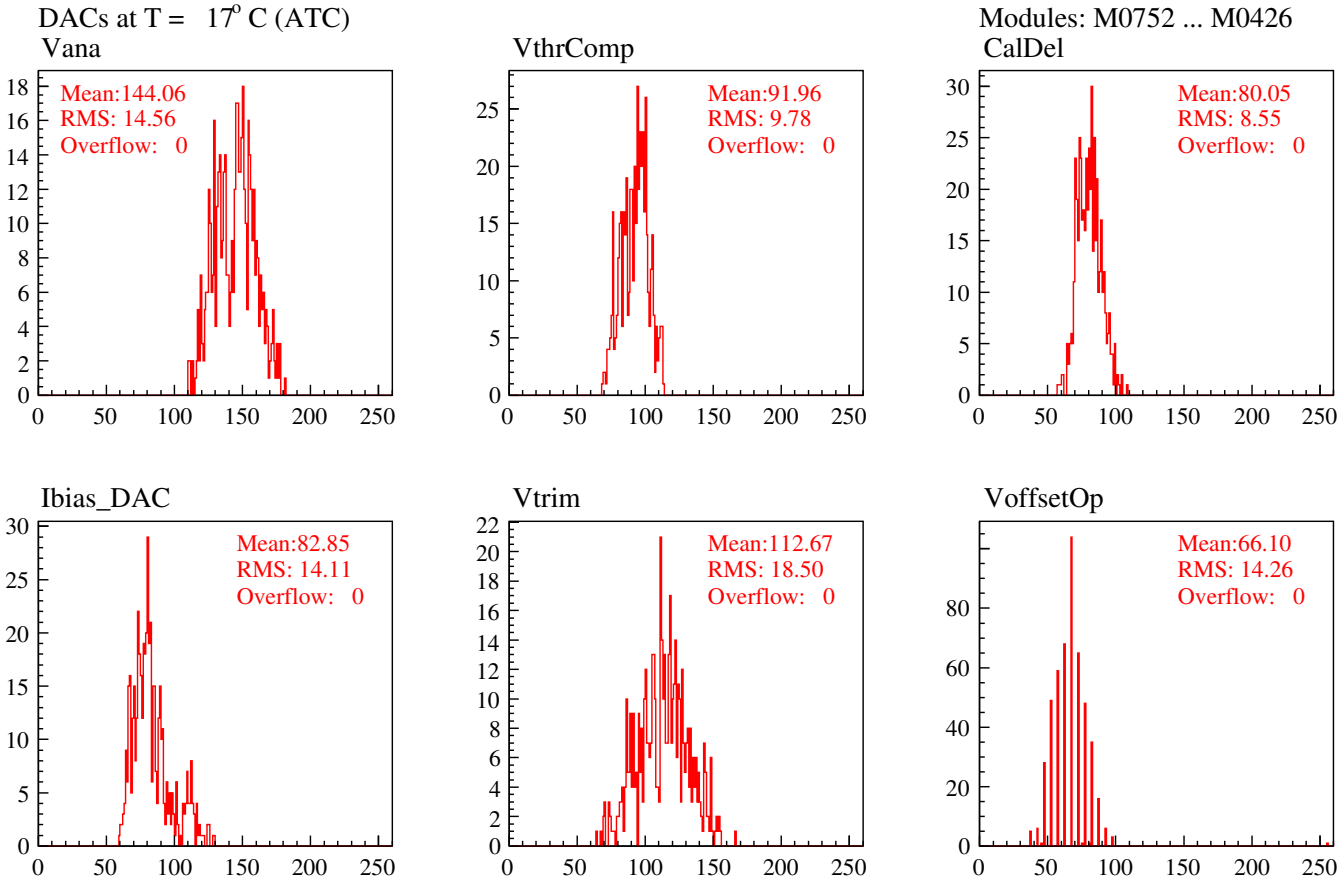
Mean DACs III





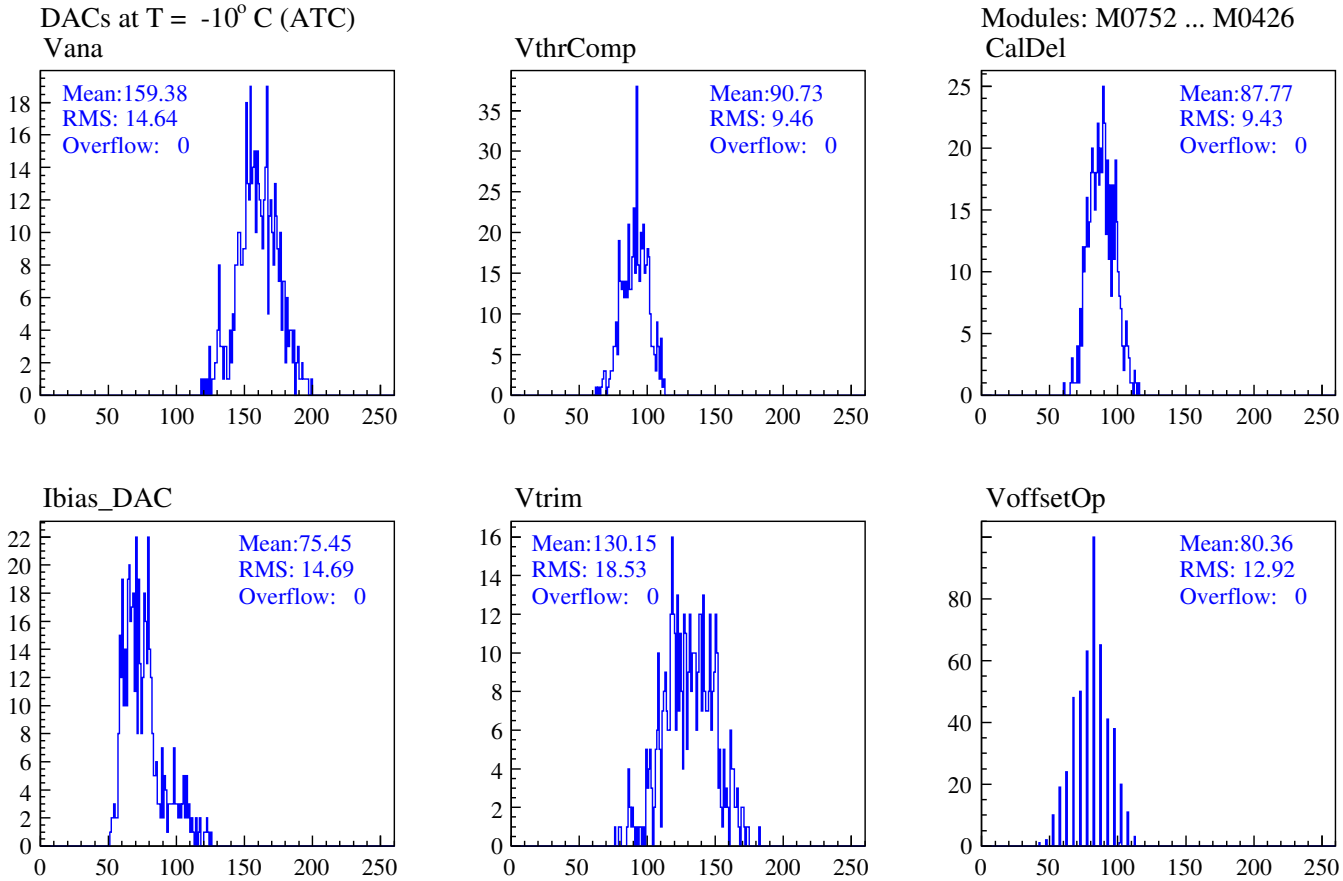
Operational parameters at $T = +17^{o}C$ (ATC)

DAC distribution (of chips)



Operational parameters at $T = -10^{o}C$ (ATC)

DAC distribution (of chips)



Operational parameters at $T = +17^{o}C$ (BTC)

DAC distribution (of chips)