

BPIX Module Testing Status - week 43

5th January 2007

Production Status: 308 modules produced

- 213/40 graded as A/B → 82%
- 55 graded as C → 18%

Testing Status of week 43:

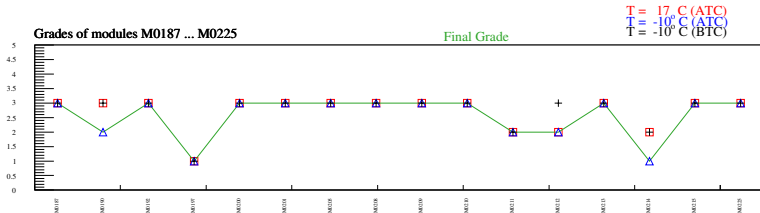
- 16 modules fully tested and therm. cycled

Grade	A	B	C
T = -10° C, BTC*	13	2	1
T = -10° C, ATC	11	3	2
T = $+17^{\circ}$ C, ATC	12	3	1
Final Grade	11	3	2

- 8 partially tested / testing failed
- 14 were retested (nothing changed)

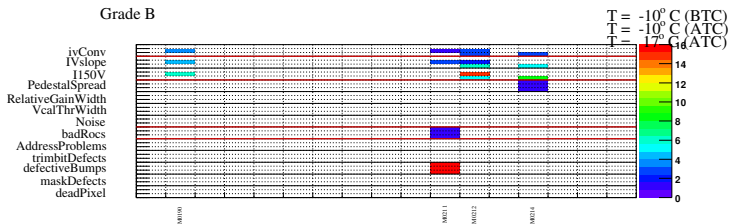
*without IV-criteria

Production summary

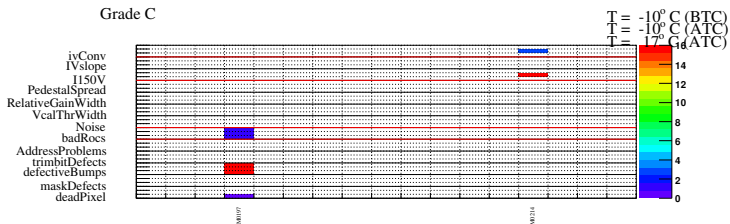


Module Failures Overview

Grade B



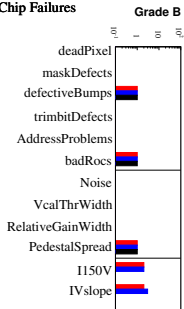
Grade C



Production quality

Grade B

Chip Failures

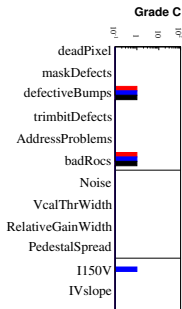


T = 17° C (ATC)

T = -10° C (ATC)

T = -10° C (BTC)

Grade C Failures



← Pixel defects

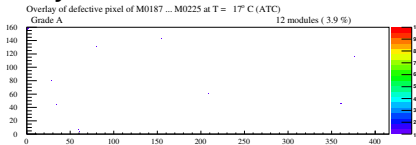
← Chip performance

← Module IV

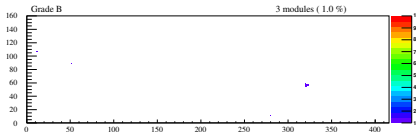
Defective pixel $T = 17^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = +17^{\circ}\text{C}$ (ATC)

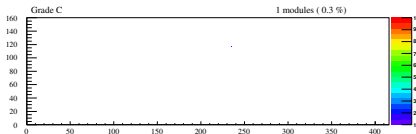
Grade A
(12 modules)



Grade B
(3 modules)



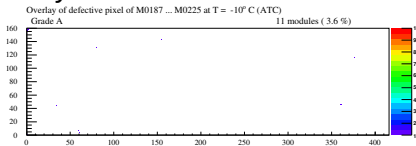
Grade C
(1 modules)



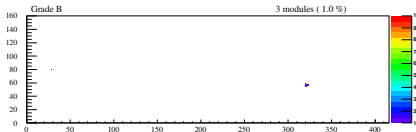
Defective pixel $T = -10^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (ATC)

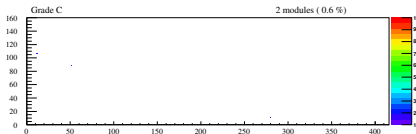
Grade A
(11 modules)



Grade B
(3 modules)



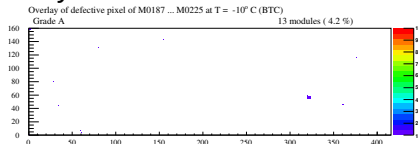
Grade C
(2 modules)



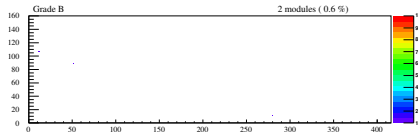
Defective pixel $T = -10^{\circ}\text{C}$ (BTC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (BTC)

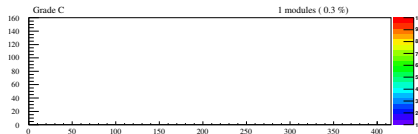
Grade A
(13 modules)



Grade B
(2 modules)



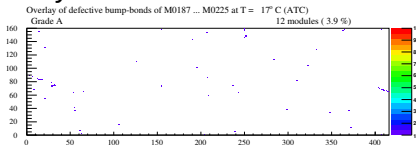
Grade C
(1 modules)



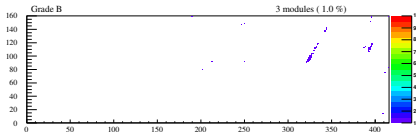
Defective bump-bonds $T = 17^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = +17^{\circ}\text{C}$ (ATC)

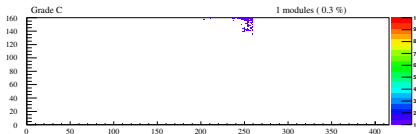
Grade A
(12 modules)



Grade B
(3 modules)



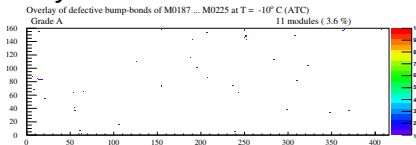
Grade C
(1 modules)



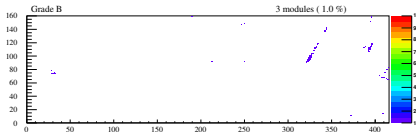
Defective bump-bonds $T = -10^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (ATC)

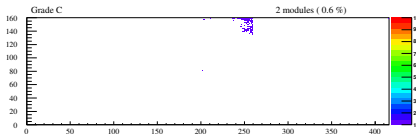
Grade A
(11 modules)



Grade B
(3 modules)



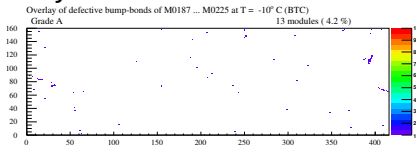
Grade C
(2 modules)



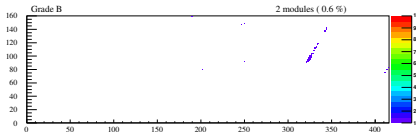
Defective bump-bonds $T = -10^{\circ}\text{C}$ (BTC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (BTC)

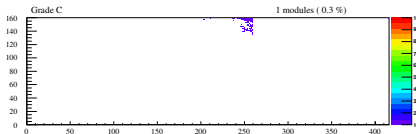
Grade A
(13 modules)



Grade B
(2 modules)



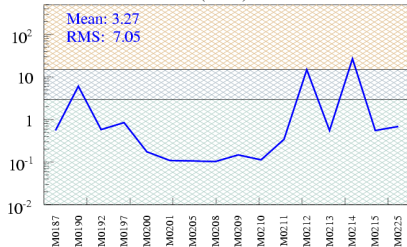
Grade C
(1 modules)



Current at 150 V

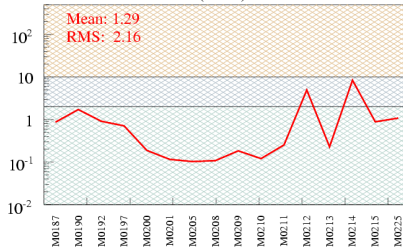
Current at 150 V (in μA) at $T = 17^\circ\text{C}$ and $T = -10^\circ\text{C}$

I150V at $T = -10^\circ\text{C}$ (ATC)



recalculated

I150V at $T = 17^\circ\text{C}$ (ATC)

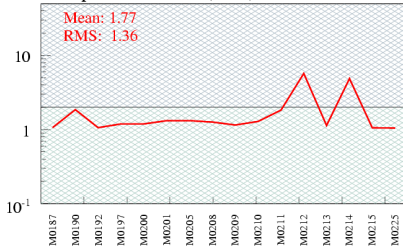


measured

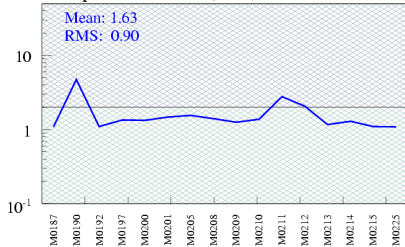
Slope of IV-Curve

Slope of IV-Curve at $T = 17^{\circ}\text{C}$ and $T = -10^{\circ}\text{C}$

IVslope at $T = 17^{\circ}\text{C}$ (ATC)



IVslope at $T = -10^{\circ}\text{C}$ (ATC)

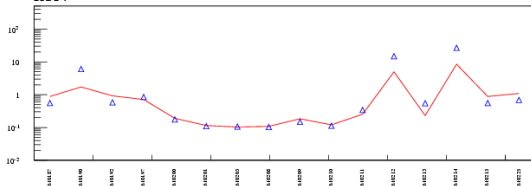


Current recalculation to $T = 17^{\circ}\text{C}$

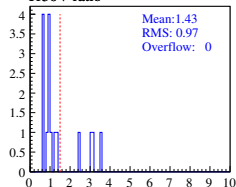
Cross check of recalculated values with measured values

$T = 17^{\circ}\text{C}$ (ATC)
 $T = -10^{\circ}\text{C}$ (ATC)
 $T = -10^{\circ}\text{C}$ (BTC)

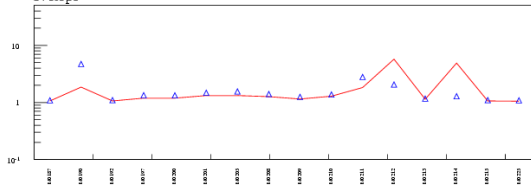
I150V



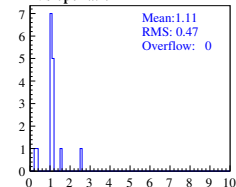
I150V ratio



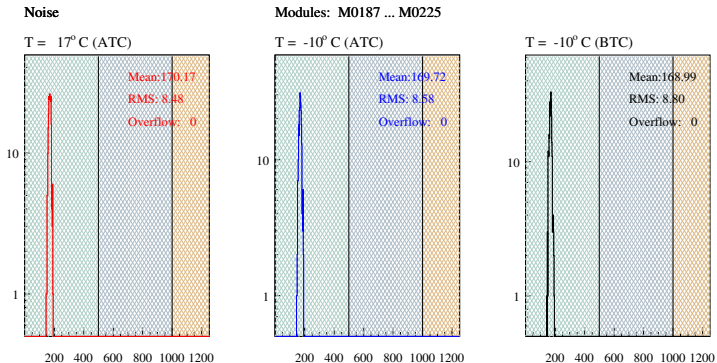
IVslope



IVslope ratio

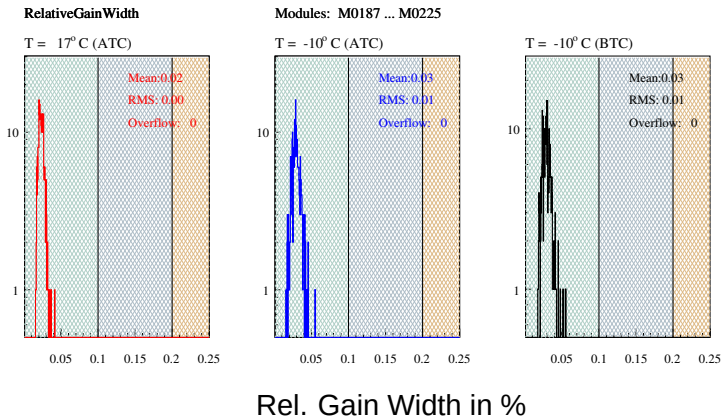


MeanNoise of chips

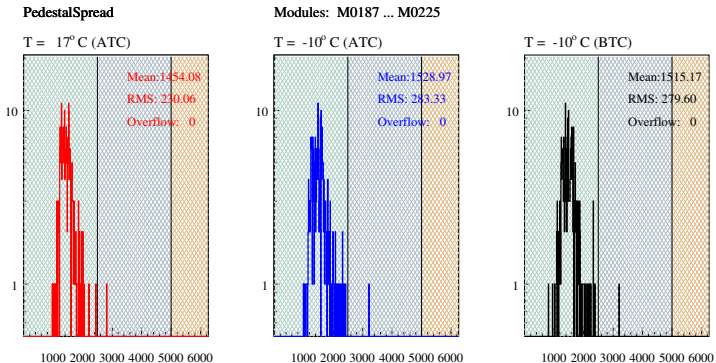


Noise in e^-

RelativeGainWidth of chips



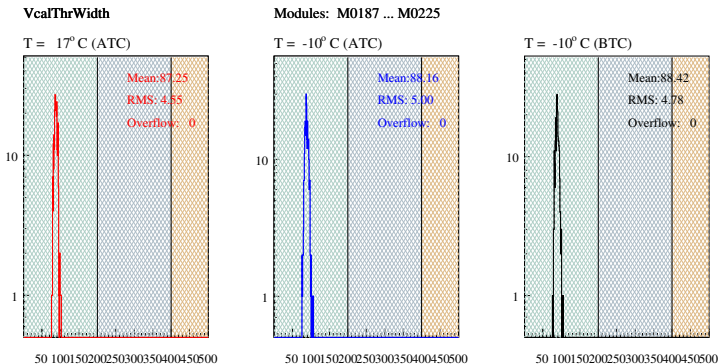
PedestalSpread of chips



Pedestal Spread in e^-

Vcal Threshold Width

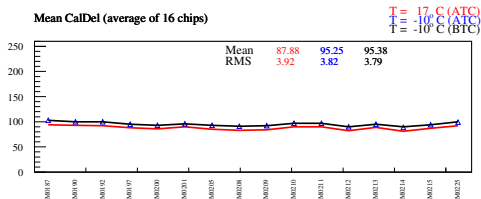
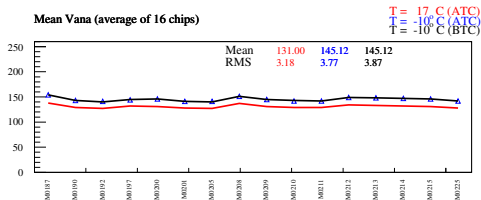
VcalThresholdWidth of chips



Vcal Thr. Width in e^-

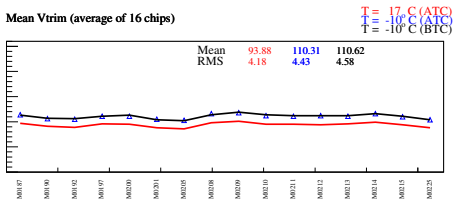
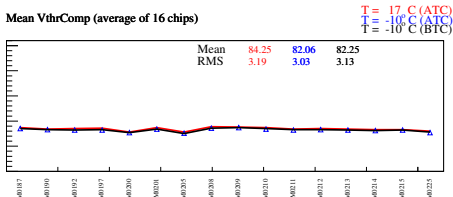
Operational parameters I

Mean DACs I



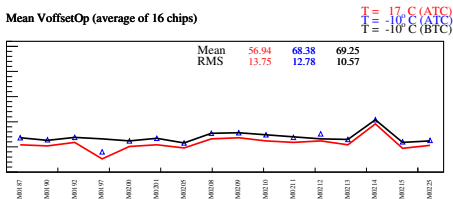
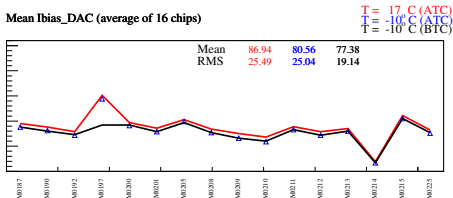
Operational parameters II

Mean DACs II



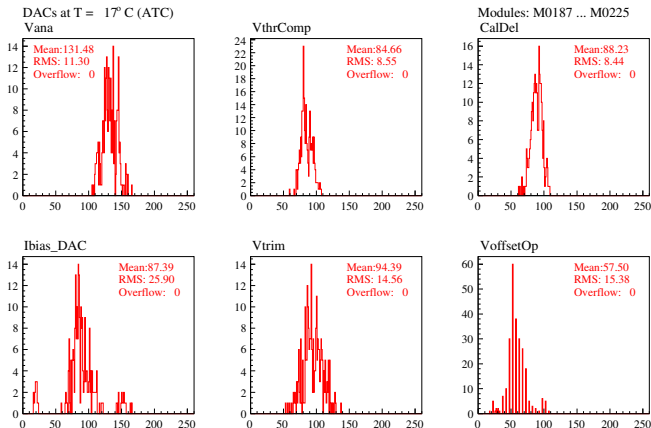
Operational parameters III

Mean DACs III



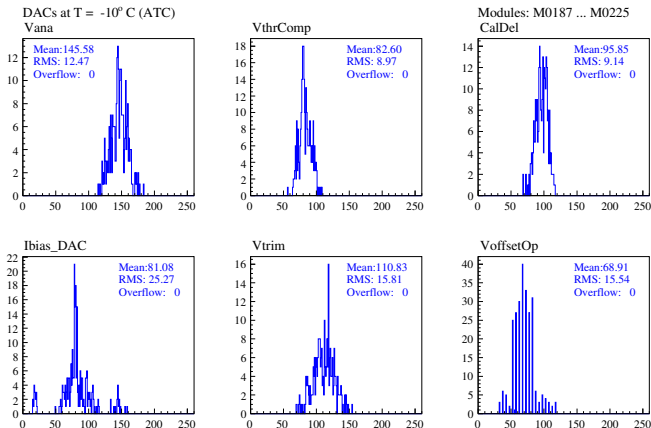
Operational parameters at $T = +17^{\circ}\text{C}$ (ATC)

DAC distribution (of chips)



Operational parameters at $T = -10^{\circ}\text{C}$ (ATC)

DAC distribution (of chips)

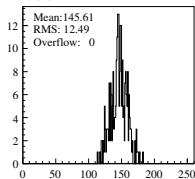


Operational parameters at $T = +17^{\circ}\text{C}$ (BTC)

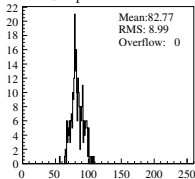
DAC distribution (of chips)

DACs at $T = -10^{\circ}\text{C}$ (BTC)

Vana

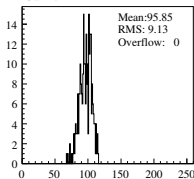


VthrComp

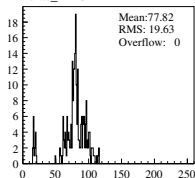


Modules: M0187 ... M0225

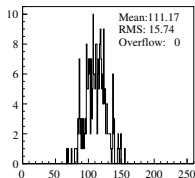
CalDel



Ibias_DAC



Vtrim



VoffsetOp

