

BPIX Module Testing Status - week 37

5th January 2007

Production Status: 308 modules produced

- 213/40 graded as A/B → 82%
- 55 graded as C → 18%

Testing Status of week 37:

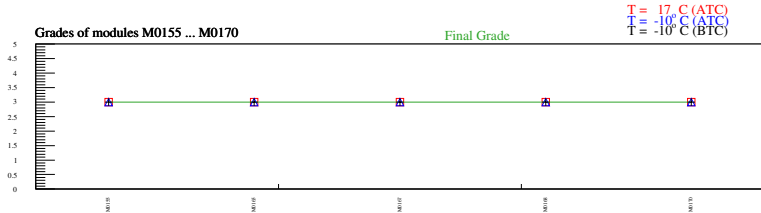
- 5 modules fully tested and therm. cycled

Grade	A	B	C
T = -10° C, BTC*	5	0	0
T = -10° C, ATC	5	0	0
T = $+17^{\circ}$ C, ATC	5	0	0
Final Grade	5	0	0

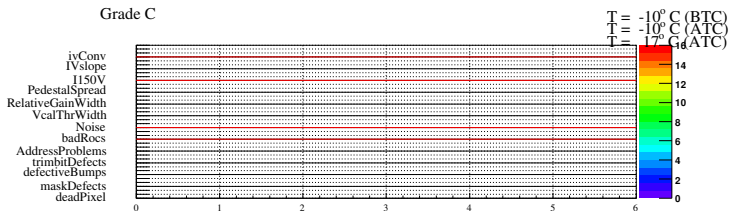
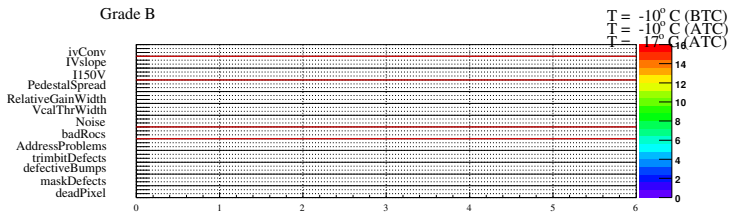
- 15 partially tested / testing failed
- no retests

*without IV-criteria

Production summary

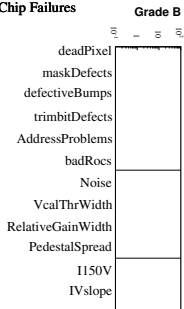


Module Failures Overview



Grade B

Chip Failures

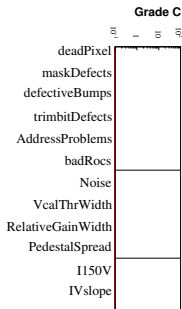


T = 17° C (ATC)

T = -10° C (ATC)

T = -10° C (BTC)

Grade C Failures



← Pixel defects

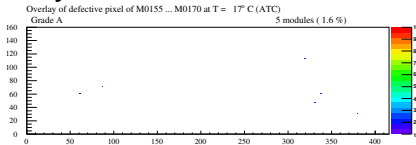
← Chip performance

← Module IV

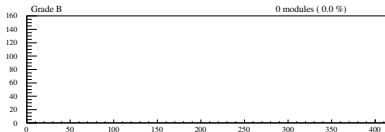
Defective pixel $T = 17^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = +17^{\circ}\text{C}$ (ATC)

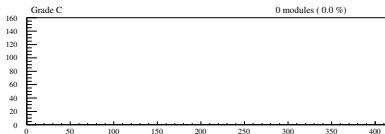
Grade A
(5 modules)



Grade B
(0 modules)



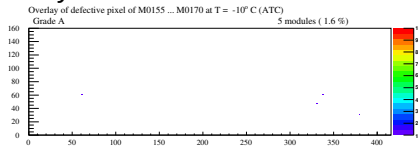
Grade C
(0 modules)



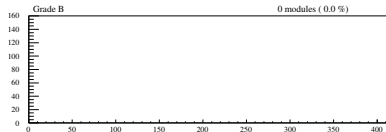
Defective pixel $T = -10^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (ATC)

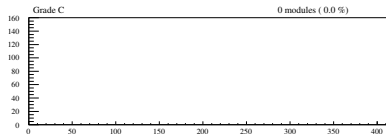
Grade A
(5 modules)



Grade B
(0 modules)



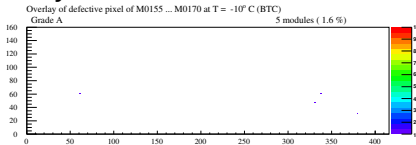
Grade C
(0 modules)



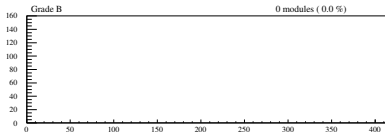
Defective pixel $T = -10^{\circ}\text{C}$ (BTC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (BTC)

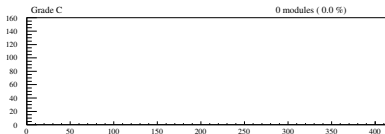
Grade A
(5 modules)



Grade B
(0 modules)



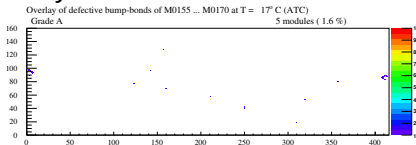
Grade C
(0 modules)



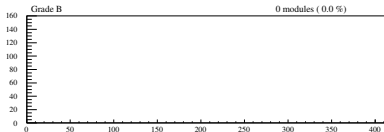
Defective bump-bonds $T = 17^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = +17^{\circ}\text{C}$ (ATC)

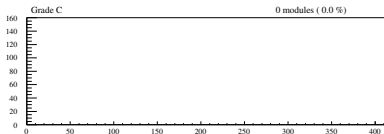
Grade A
(5 modules)



Grade B
(0 modules)



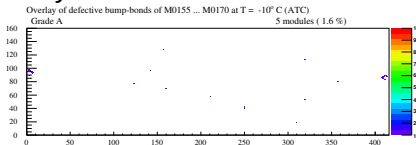
Grade C
(0 modules)



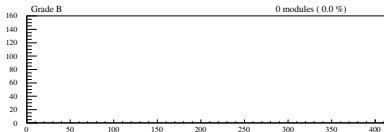
Defective bump-bonds $T = -10^{\circ}\text{C}$ (ATC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (ATC)

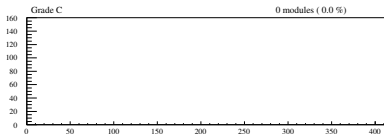
Grade A
(5 modules)



Grade B
(0 modules)



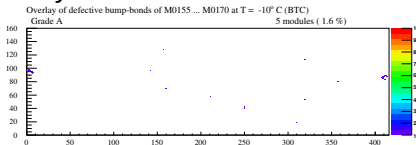
Grade C
(0 modules)



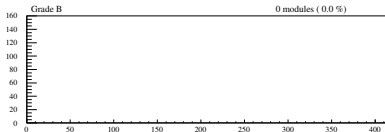
Defective bump-bonds $T = -10^{\circ}\text{C}$ (BTC)

Overlay of all fully tested modules at $T = -10^{\circ}\text{C}$ (BTC)

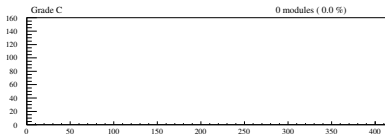
Grade A
(5 modules)



Grade B
(0 modules)

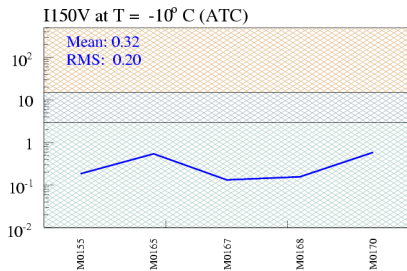


Grade C
(0 modules)

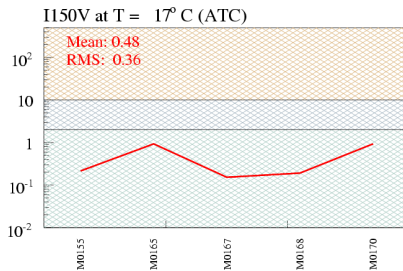


Current at 150 V

Current at 150 V (in μA) at $T = 17^\circ\text{C}$ and $T = -10^\circ\text{C}$



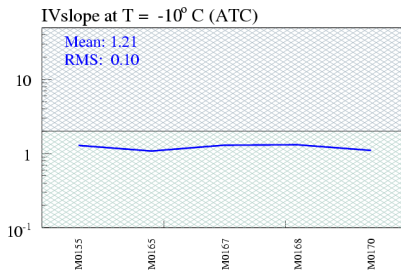
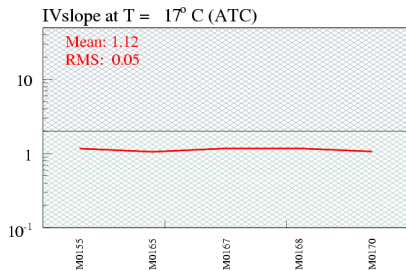
recalculated



measured

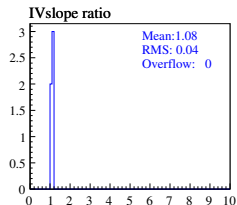
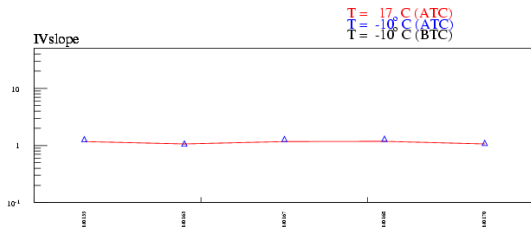
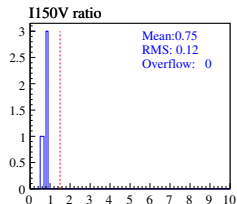
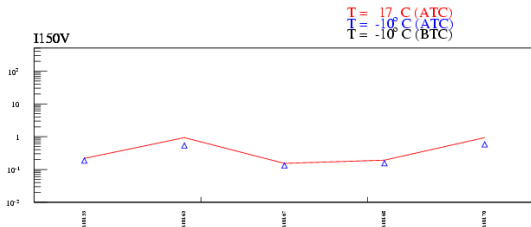
Slope of IV-Curve

Slope of IV-Curve at $T = 17^{\circ}\text{C}$ and $T = -10^{\circ}\text{C}$

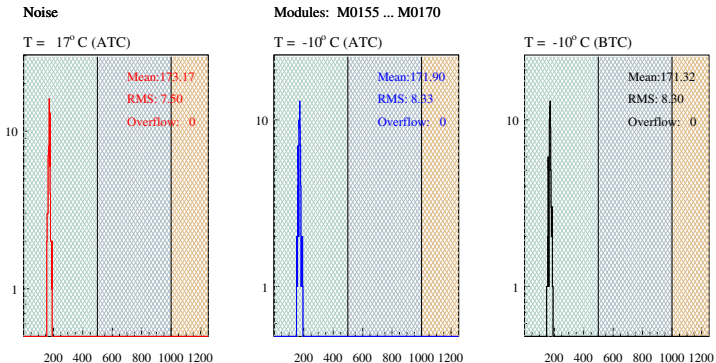


Current recalculation to $T = 17^{\circ}\text{C}$

Cross check of recalculated values with measured values

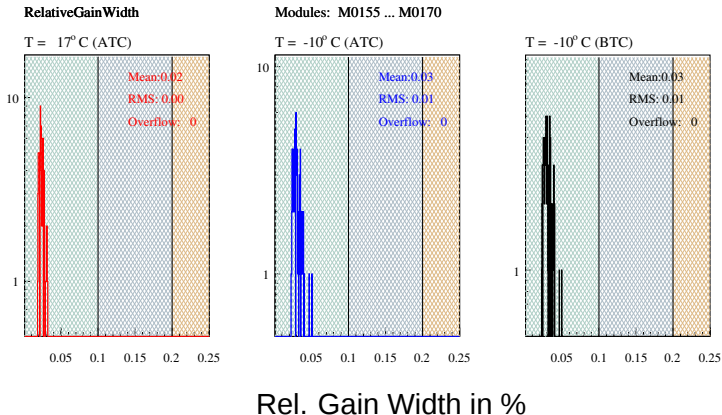


MeanNoise of chips



Noise in e^-

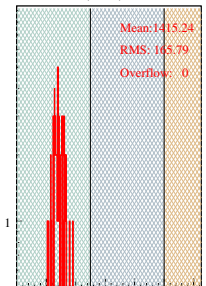
RelativeGainWidth of chips



PedestalSpread of chips

PedestalSpread

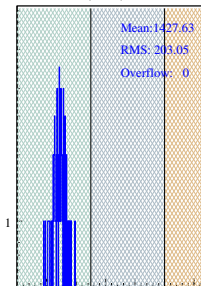
T = 17° C (ATC)



1000 2000 3000 4000 5000 6000

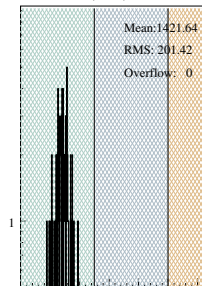
Modules: M0155 ... M0170

T = -10° C (ATC)



1000 2000 3000 4000 5000 6000

T = -10° C (BTC)

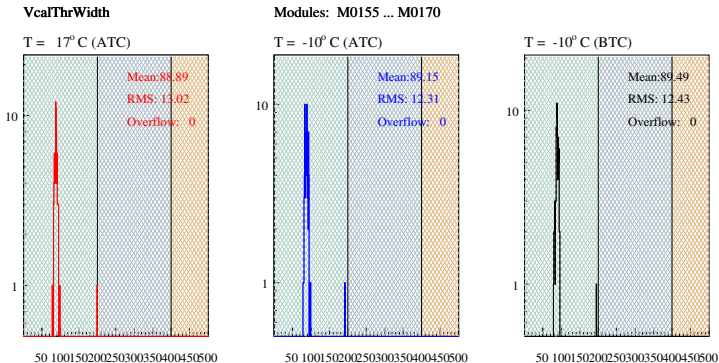


1000 2000 3000 4000 5000 6000

Pedestal Spread in e^-

Vcal Threshold Width

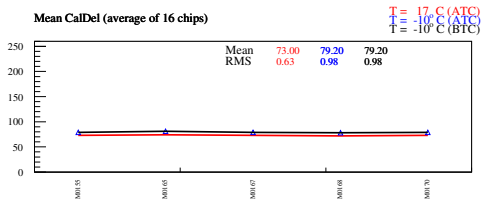
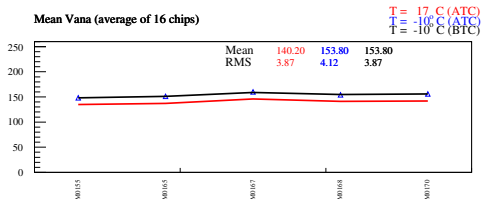
VcalThresholdWidth of chips



Vcal Thr. Width in e^-

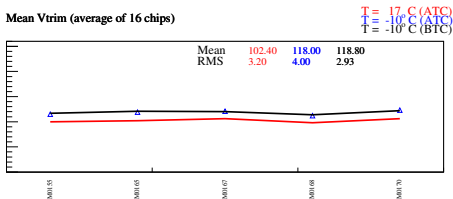
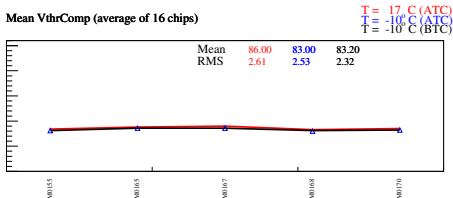
Operational parameters I

Mean DACs I



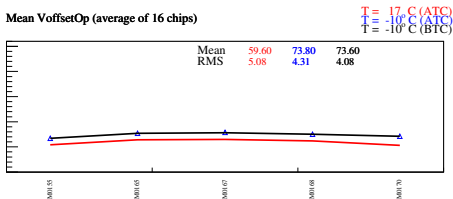
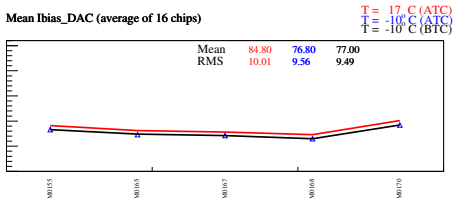
Operational parameters II

Mean DACs II



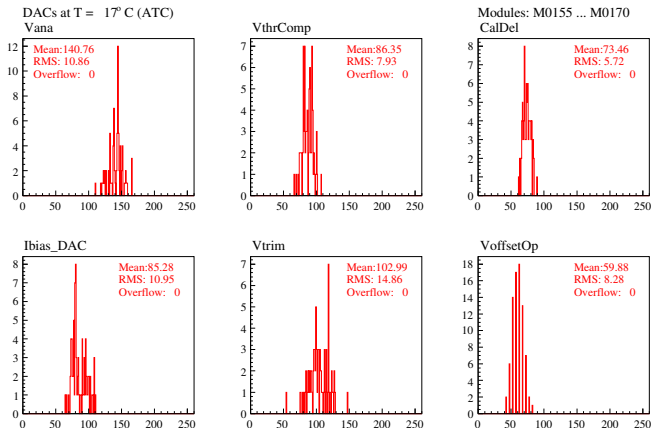
Operational parameters III

Mean DACs III



Operational parameters at $T = +17^{\circ}\text{C}$ (ATC)

DAC distribution (of chips)

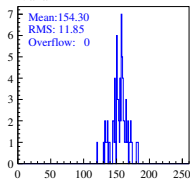


Operational parameters at $T = -10^{\circ}\text{C}$ (ATC)

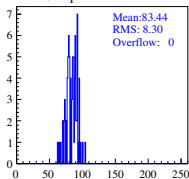
DAC distribution (of chips)

DACs at $T = -10^{\circ}\text{C}$ (ATC)

Vana

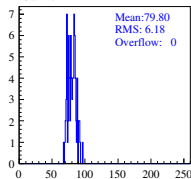


VthrComp

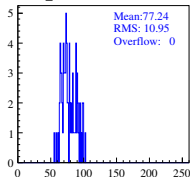


Modules: M0155 ... M0170

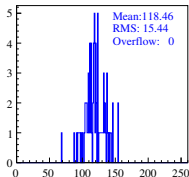
CalDel



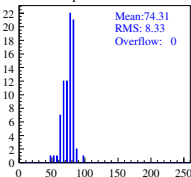
Ibias_DAC



Vtrim



VoffsetOp

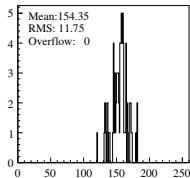


Operational parameters at $T = +17^{\circ}\text{C}$ (BTC)

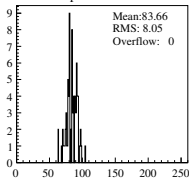
DAC distribution (of chips)

DACs at $T = -10^{\circ}\text{C}$ (BTC)

Vana

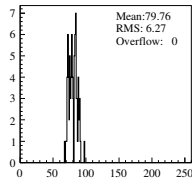


VthrComp

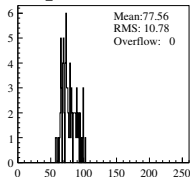


Modules: M0155 ... M0170

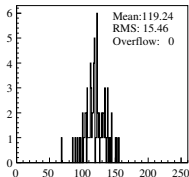
CalDel



Ibias_DAC



Vtrim



VoffsetOp

