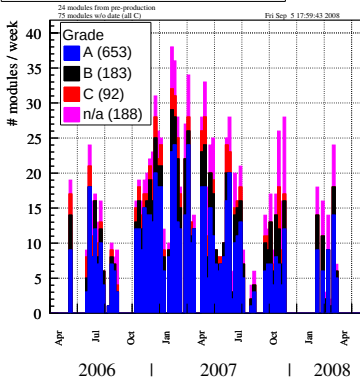
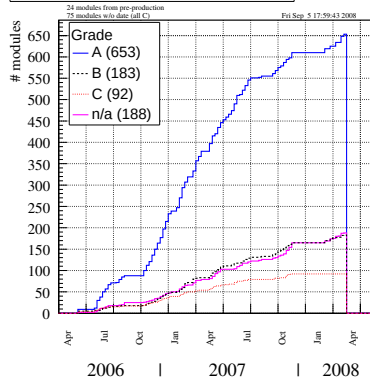


BPIX Module Testing Status - 2008

5th September 2008

Production Overview

Tested Modules 2006 - 2008 (incl. half-modules)**Tested Modules 2006 - 2008 (incl. half-modules)**

Production overview

Production Status: 929 modules produced (808 full/ 121 half)

- 566/161 graded as A/B → 90% || 87/23 → 91%
- 81 graded as C → 10% || 11 → 9%

Module Testing Report of 2008:

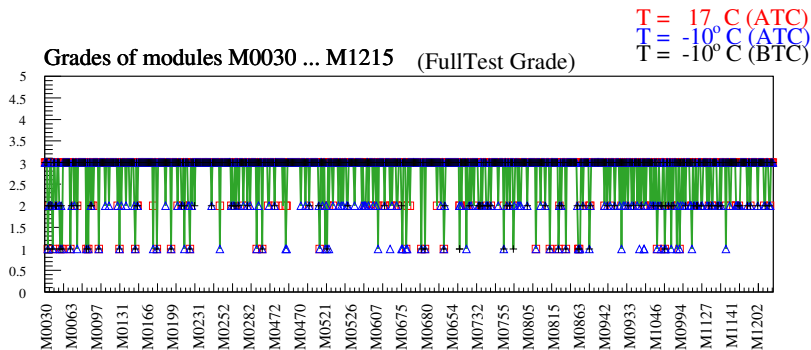
- 775 modules fully tested and therm. cycled (71 retested)

	Modules (775)			Halfmodules (119)		
Grade	A	B	C	A	B	C
T = -10° C, BTC*	674	73	28	108	5	6
T = -10° C, ATC	579	140	56	94	18	7
T = +17° C, ATC	654	92	29	98	13	8
Final Grade	565	161	49	87	23	9

- 101 were retested with new DAC settings (7 change)

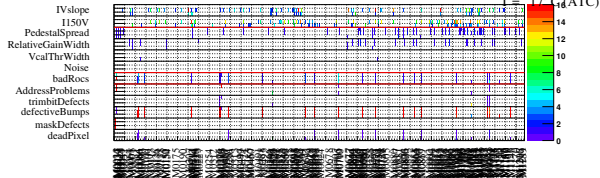
- M0037: A -> B -> overall grades - M0064: A -> B -> overall grades + M0067: B -> A -> overall grades +
M0070: C -> A -> overall grades + M0072: C -> N -> overall grades + M0143: B -> A -> overall grades +
M0145: B -> A -> overall grades

Production summary

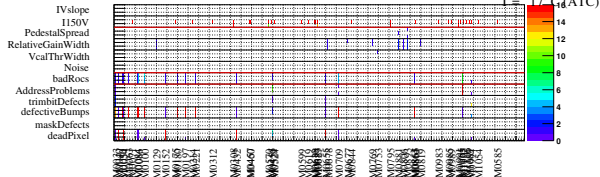


Module Failures Overview

Grade B



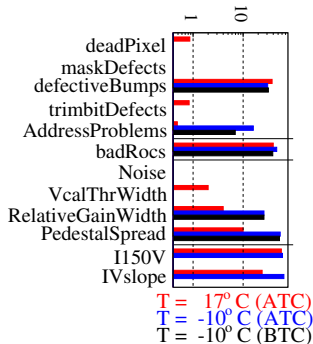
Grade C



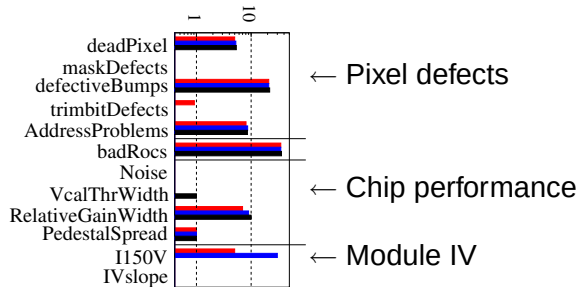
Production quality

Chip Failures

Grade B
Grade B

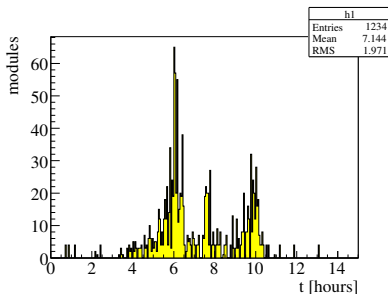


Grade C
Grade C

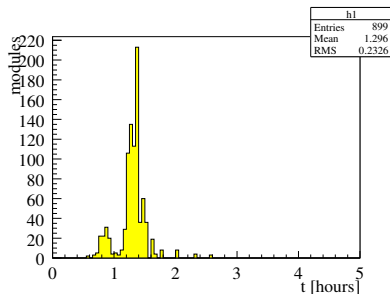


Test duration

Full tests



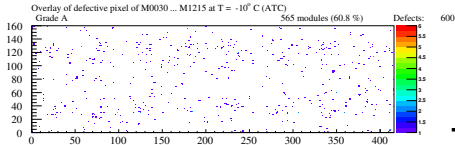
Short tests (w/o x-ray)



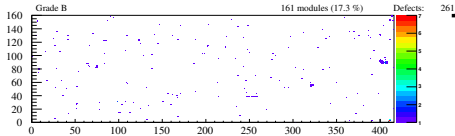
Dead pixel

Overlay of modules tested at $T = -10^{\circ}\text{C}$ (ATC)

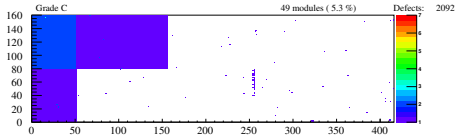
Final Grade A
(565 modules)



Final Grade B
(161 modules)



Final Grade C
(49 modules)



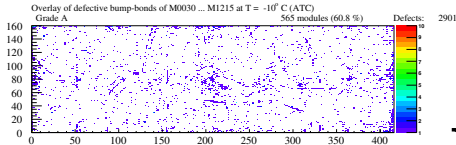
} 48.3 Mio. Pixel

3.3 Mio. Pixel

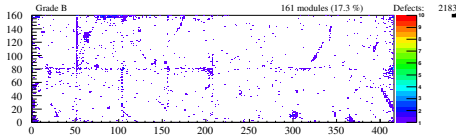
Defective bump-bonds

Overlay of modules tested at $T = -10^{\circ}\text{C}$ (ATC)

Final Grade A
(565 modules)

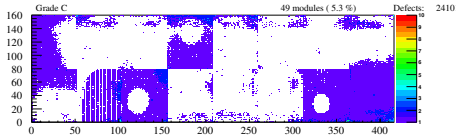


Final Grade B
(161 modules)



} 48.3 Mio. Pixel

Final Grade C
(49 modules)

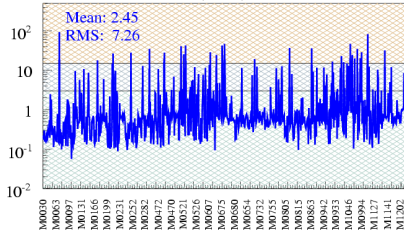


3.3 Mio. Pixel

Current at 150 V

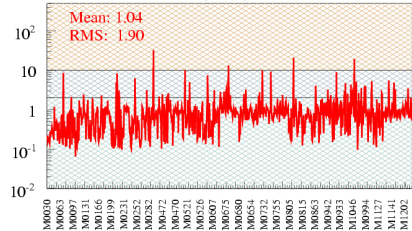
Current at 150 V (in μA) at $T = 17^\circ\text{C}$ and $T = -10^\circ\text{C}$

I150V at T = -10°C (ATC)



recalculated

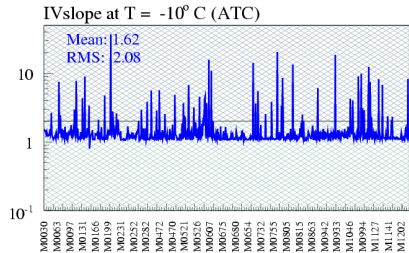
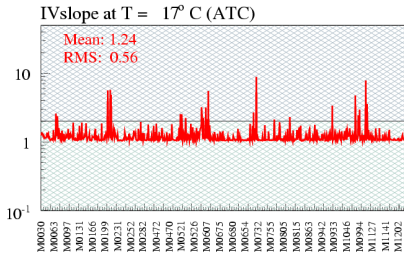
I150V at T = 17°C (ATC)



measured

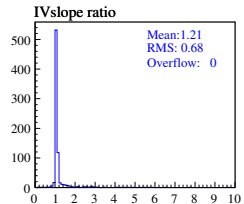
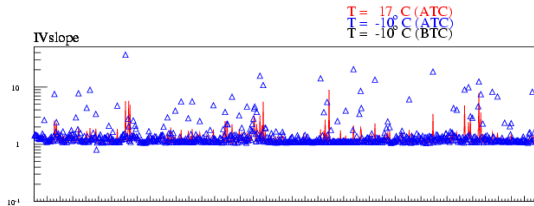
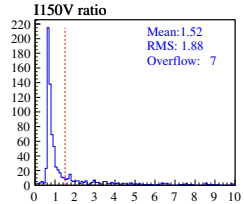
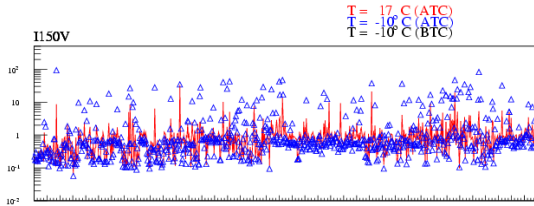
Slope of IV-Curve

Slope of IV-Curve at $T = 17^{\circ}\text{C}$ and $T = -10^{\circ}\text{C}$



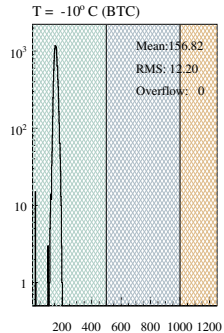
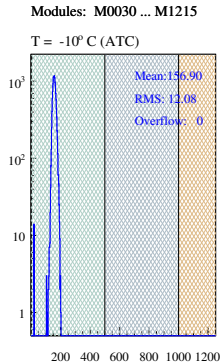
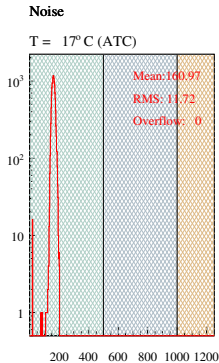
Current recalculation to $T = 17^{\circ}\text{C}$

Cross check of recalculated values with measured values



Noise

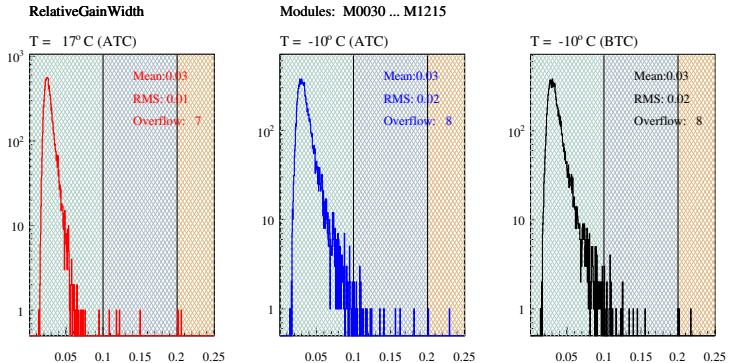
MeanNoise of chips



Noise in e^-

Relative Gain Width

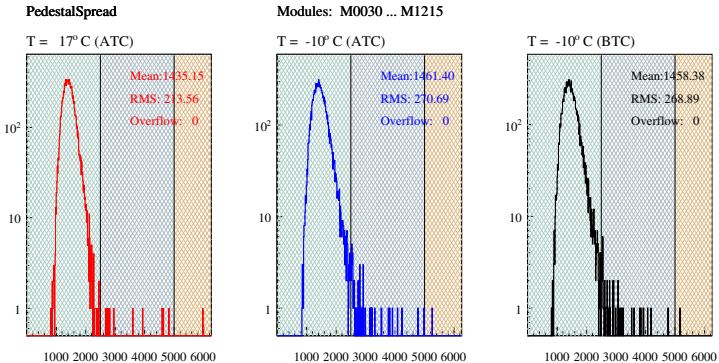
RelativeGainWidth of chips



Rel. Gain Width in %

Pedestal Spread

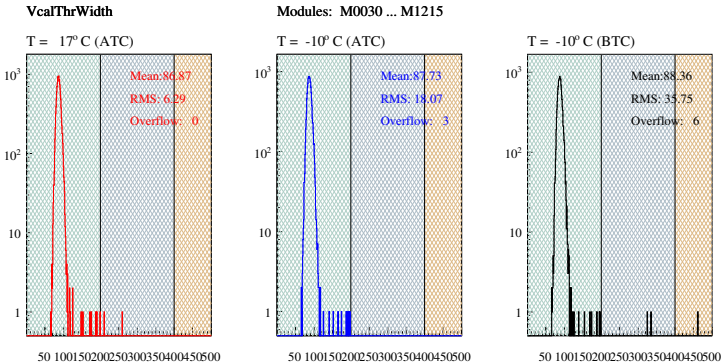
PedestalSpread of chips



Pedestal Spread in e^-

Vcal Threshold Width

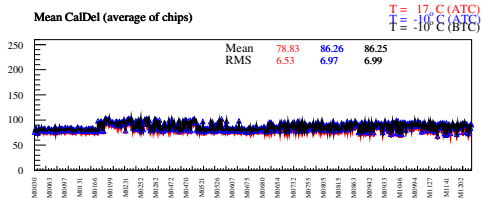
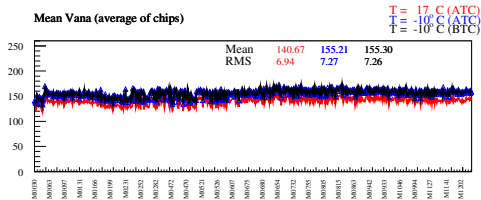
VcalThresholdWidth of chips



Vcal Thr. Width in e^-

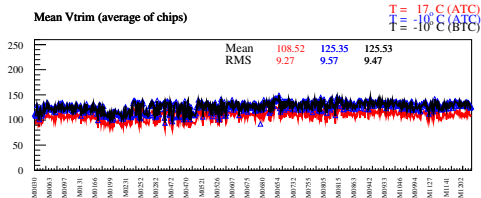
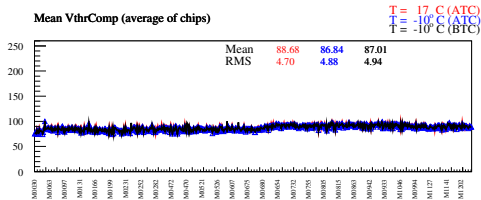
Operational parameters I

Mean DACs I



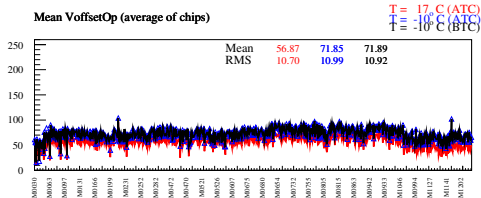
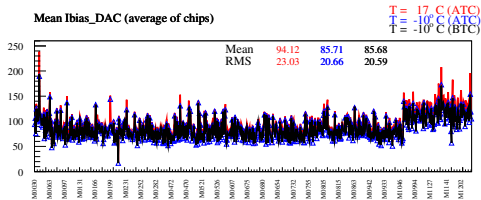
Operational parameters II

Mean DACs II



Operational parameters III

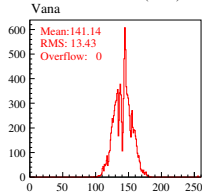
Mean DACs III



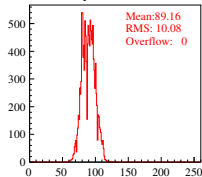
Operational parameters at $T = +17^{\circ}\text{C}$ (ATC)

DAC distribution (of chips)

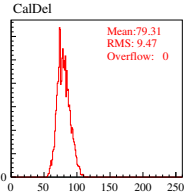
DACs at $T = 17^{\circ}\text{C}$ (ATC)



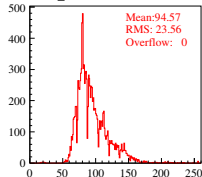
VthrComp



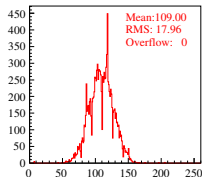
Modules: M0030 ... M1215



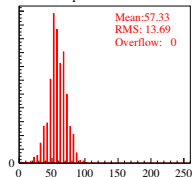
Ibias_DAC



Vtrim

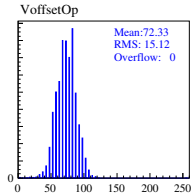
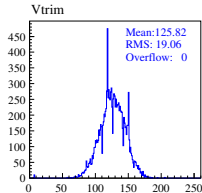
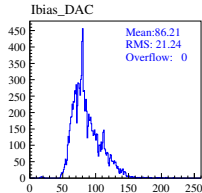
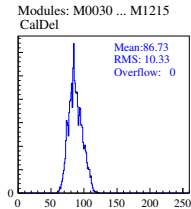
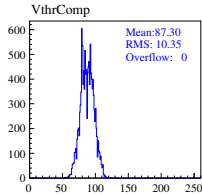
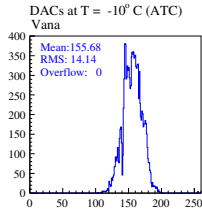


VoffsetOp



Operational parameters at $T = -10^{\circ}\text{C}$ (ATC)

DAC distribution (of chips)

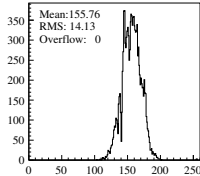


Operational parameters at $T = +17^{\circ}\text{C}$ (BTC)

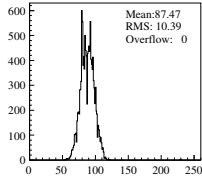
DAC distribution (of chips)

DACs at $T = -10^{\circ}\text{C}$ (BTC)

Vana

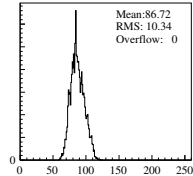


VthrComp

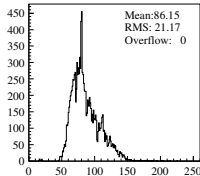


Modules: M0030 ... M1215

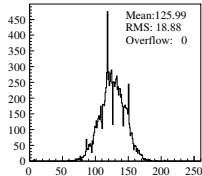
CalDel



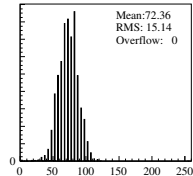
Ibias_DAC



Vtrim

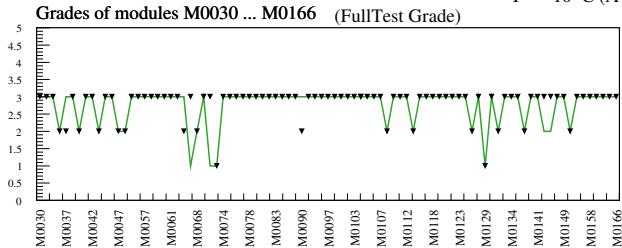


VoffsetOp



Retest Grades

T = -10° C (ATC, old DAC)
T = -10° C (ATC, new DAC)

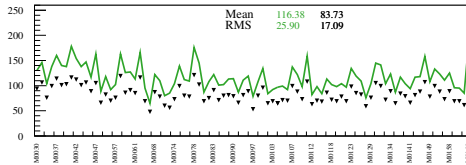


Operational parameters

Mean DACs I

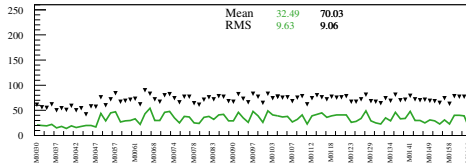
Mean Ibias_DAC (average of chips)

T = -10° C (ATC, old DACs)
T = -10° C (ATC, new DACs)



Mean VoffsetOp (average of chips)

T = -10° C (ATC, old DACs)
T = -10° C (ATC, new DACs)

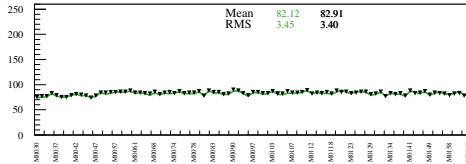


Operational parameters

Mean DACs II

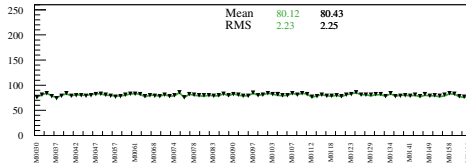
Mean VthrComp (average of chips)

T = -10° C (ATC, old DACs)
T = -10° C (ATC, new DACs)



Mean CalDel (average of chips)

T = -10° C (ATC, old DACs)
T = -10° C (ATC, new DACs)

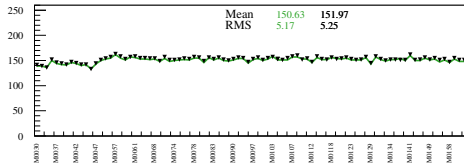


Operational parameters

Mean DACs III

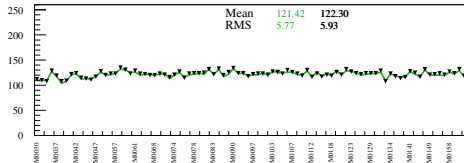
Mean Vana (average of chips)

$T = -10^{\circ}\text{C}$ (ATC, old DACs)
 $T = -10^{\circ}\text{C}$ (ATC, new DACs)



Mean Vtrim (average of chips)

$T = -10^{\circ}\text{C}$ (ATC, old DACs)
 $T = -10^{\circ}\text{C}$ (ATC, new DACs)

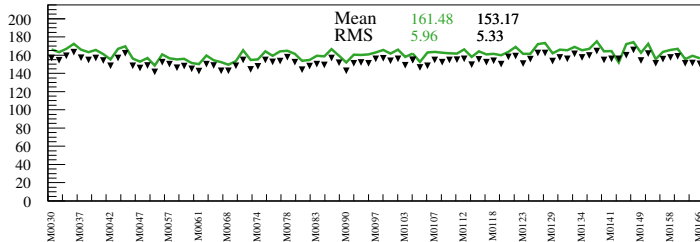


Performance parameters

Mean Noise [e^-] vs. Module Nr.

Mean Noise (average of chips)

$T = -10^\circ\text{C}$ (ATC, old DACs)
 $T = -10^\circ\text{C}$ (ATC, new DACs)

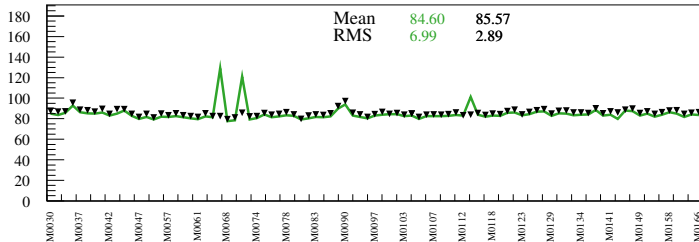


Performance parameters

Mean **VcalThresholdWidth** [e^-] vs. Module Nr.

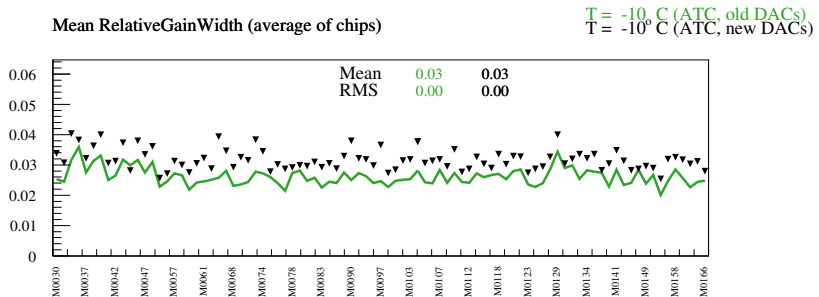
Mean VcalThrWidth (average of chips)

$T = -10^\circ\text{C}$ (ATC, old DACs)
 $T = -10^\circ\text{C}$ (ATC, new DACs)



Performance parameters

Mean **RelativeGainWidth** [%] vs. Module Nr.



Performance parameters

Mean PedestalSpread in $[e^-]$ vs. Module Nr.

