Week 12/12-18/12

12.12 - 11:00 2 modules, 1 of them dummy. No TBM trailer

13.12 - 9:00 +2 modules. No HV on modules, fixed at 11:30. No communication with TBM for all 3 modules.

- 13:00 modules work (why?). Start test module 7690-17-3
- 15:00 second test board brought from test-beam
- 17:00 (after finishing test of first module) Setup equipped with 2 test-boards. TBM trailer problem fixed for module 2.
- 18:20 start test 2 modules (7691-23-2 and 7861-23-3)
- 22:00 test finished. Lost .root file for one module, second module address level problems. Both need to Retest.

14.12 - Problems (continue) with capton cable connectors.

- 9:30 start test 2 modules (7690-02-2 and 7690-20-1)
- 13:10 start test 2 modules (7690-17-2 and 7861-23-1)
- 16:40 start Trimming
- 18:40 finish Trimming
- 19:16 start PhCalibration
- 20:02 finish PhCalibration

Week 12/12-18/12

15.12 - 9:50 start test 2 modules (7691-23-1 and 7861-01-1) + Trimming + PhCalibration
- 17:30 start test 2 modules (7861-01-2 and 7862-12-2) + Trimming + PhCalibration

16.12 - 11:00 start test 2 modules (7691-23-3 and 7861-12-3)
- 14:00 finish test
- 15:00 start test 2 modules (7691-16-1 and 7691-16-3)
- 18:00 test finished
- 18:20 start Trimming
- 20:30 finish Trimming
- 20:50 start PhCalibration
- 21:30 finish PhCalibration for 16-3
- 23:00 finish PhCalibration for 16-1 (address decoding problems for C15)

17-18.12 Retest (2 modules), Trimming and PhCalibration (4 modules)

Week 12/12-18/12

Results: 15 modules tested

Good: 7 modules (less than 1% defects per ROC)

Dead pixels: in 1 module 1 ROC has 613 defective pixels

Bump bonding problems: 4 modules (377-1913 defective pixels)

Mask defects: in 1 module 1 ROC has 31 defective pixels

TrimBit defects: 2 modules (1 and 4 defects)

Address decoding: 5 modules almost every pixel has problem, 1 module 400-1600 defective pixels per ROC, 2 modules with 1 defective ROC (800 and 1300)

ToDo: IV curves (5 modules I(150V): 2 modules < 2 muA, 3 modules >> 2 muA) and Thermal cycling

Week 12/12-18/12

Problems solved:

- Missing wire bonds (HV), removed wire bonds (missing Trailer)
- Fixed module adapters
- Fixed thermal shield in Colling Box
- Capton cable fixation
- Time stamps in log file
- Script to produce html files with test result per module

Problem to solve:

- Emergency stop for Colling Box
- Fully automatic data transfer (local copy and DB), data processing, web page creation
- Automatic dataTriggerLevel determination (at PreTest)
- T, Humidity and current (I at 150V) recording
- Module numbering scheme (to simplify)
- Handling full or individual test repetition (in local data storage, in DB, in paper record)
- Test time optimization (currently: Full test – 3hrs, Trimming – 2 hrs, PhCal – 40min, IV – 10 min)