CMS Internal Note

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Test and Qualification Procedures of the CMS Pixel Barrel Modules

U. Langenegger[1)], A. Starodumov[1)], P. Trüb[1,2)]

Abstract

The CMS pixel barrel system will consist of three layers built of about 800 modules and half modules. One full module contains 66560 readout channels and the full pixel barrel system about 48 million channels. It is mandatory to test functionality, trimming mechanism and bump-bonding quality for each channel. Different methods to determine the bump-bonding yield with electrical measurements have been developed. Measurements of key operational parameters are included in the qualification procedure. Among them are pixel noise and pulse height calibration. Test and qualification procedures of the pixel barrel modules are described and first results of prototype modules are presented.

[1)] Institute for Particle Physics, ETH Zurich, 8093 Zurich, Switzerland

[2)] Paul Scherrer Institut, 5232 Villigen PSI, Switzerland

1 Introduction

The CMS hybrid pixel system will be the detector closest to the interaction point and should provide reliable pattern recognition, efficient and precise momentum and vertex reconstruction in an extremely high track density environment. This dictates a fine granularity that correspondingly leads to a large number of readout channels. The testing of the detector building blocks—modules—of such a system poses a challenge.

The CMS pixel barrel module consists of a single sensor substrate with 16 front-end readout chips (ROC) bump-bonded to it and a hybrid circuit (HDI—high density interconnect) mounted on top of the sensor. Further details about the ROC design can be found in [1]. Two thin strips of Si_3N_4 glued to the readout chips serve as a base to attach the module to the cooling frame. The whole pixel barrel detector will contain about 48 million readout channels. It is mandatory to test each channel for functionality, trimming mechanism and bump-bonding quality. The qualification process also includes the determination of the operational parameters (like DAC and trim bit settings, measurement of noise, pulse height calibration), a check of the sensor I-V dependence and a thermal cycling test. The time scale for the barrel detector construction is about one year. This requires that four modules are tested per day. To fulfill this time-constraint it is anticipated to use only tested components and perform a failure diagnostics in parallel with the qualification tests. Further details about the assembling procedure of the pixel barrel modules can be found in [2].

In the following test and qualification procedures will be described. Some results of three tested prototype modules will be presented to illustrate the quality of ROCs and modules and to describe qualification criteria established so far.

2 Test overview

The qualification of a module implies a thorough check of its functionality and performance. Each ROC should be programmable by setting corresponding DAC registers. During the startup all 29 DACs of a ROC are initialized to their default values listed in Tab. 1. Every pixel readout circuit has to exhibit a correct behavior. Fig. 1 shows a sketch of the analog part of the pixel unit cell implemented in each pixel. The analog signal is first passed through a preamplifier and a shaper. If the signal exceeds a reference voltage, the pixel sends its address to the double column periphery. The reference voltage is mainly determined by the VthrComp DAC value. However, the threshold can be modified for each pixel by setting four trim bits, which determine the amount of the trim voltage to be subtracted from the threshold voltage.

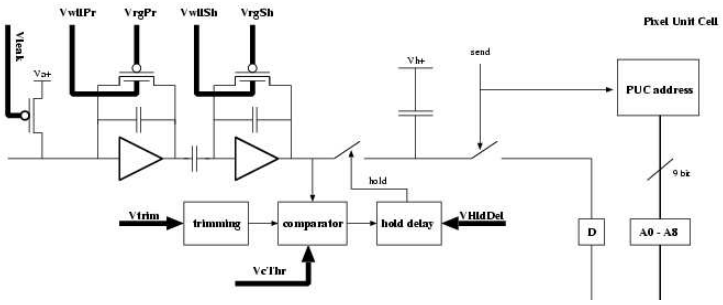

Figure 1: Sketch of the analog part of a pixel unit cell.

The test and qualification process is divided into three main steps. Before the tests can be performed, all ROCs are subject to a visual inspection and have to be set into an operational regime. This is achieved by the following procedures:

- **Analog current setting**: set the analog current to the nominal value of 24 mA.
- **Ultra-black level unification**: set the ultra-black levels of all ROCs to a common value.
- **Threshold/timing setting**: tune the signal threshold and the timing of the internal calibration signal to a stable regime.

In the second step the functionality of the pixel readout circuits and their electrical connections to the sensor pixels are checked. The following procedures are foreseen:

Table 1: The 29 DACs of a ROC and their default values.

DAC	Register	Default value
Vdig	1	8
Vana	2	150
Vsf	3	128
Vcomp	4	10
Vleak_comp	5	0
VrgPr	6	0
VwllPr	7	35
VrgSh	8	0
VwllSh	9	35
VhldDel	10	88
Vtrim	11	7
VthrComp	12	90
VIBias_Bus	13	30
Vbias_sf	14	10
VoffsetOp	15	40
VIbiasOp	16	50
VOffsetR0	17	100
VIon	18	115
VIbias_PH	19	200
Ibias_DAC	20	90
VIbias_roc	21	120
VIColOr	22	99
Vnpix	23	0
VSumCol	24	0
Vcal	25	200
CalDel	26	70
RangeTemp	27	0
CtrlReg	253	0
WBC	254	100

- **Pixel test**: check that each pixel responds to an internal calibration signal.
- **Trim bit test**: test the functionality of the four trim bits.
- **Bump-bonding test**: determine the bump-bonding quality.
- **Pixel address test**: verify that each pixel readout circuit responds with the correct pixel address.

Finally, it is necessary to determine the main characteristics for a module so that it can be set into the operational regime and be calibrated. This allows the validation of a module's proper functionality at operational voltages, working temperature and also under temperature variations. This is done by performing the following tests:

- **Noise**: determine pixel noise by measuring a threshold curve for each pixel.
- **Trimming**: set thresholds of each pixel to obtain a uniform response over the whole module.
- **Pulse height calibration**: establish the dependency of the pulse height on the injected charge.
- I**-**V **curve**: verify the absence of sensor breakdown and high leakage current.
- **Temperature sensor calibration**: relate the voltage of the temperature sensor of each ROC to an absolute temperature.
- **Thermal cycle**: ensure that the module can be operated at the working temperature of $-10°$C. Test the behavior under different temperatures and determine all relevant parameters at the working temperature.

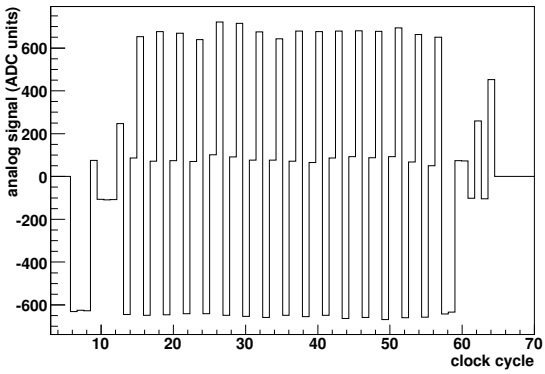

Figure 2: Analog signal after unification of the ultra-black levels.

All the tests are performed with a test board designed at ETH, which is connected to a PC via an USB interface. The module is connected to the test board with a so called module adapter board. The test board includes a field-programmable gate array (FPGA) which controls the tests as well as two analog-to-digital converters to digitize the two analog output signals of the module.

Before describing the tests in detail, we provide some general remarks about the test procedures. The first remark concerns the signal sequence sent to the module for every triggered readout. This sequence consists always of the following commands: reset, calibrate, trigger. During all tests only the pixel under examination is enabled. Therefore the analog readout sequence does not need to be decoded except for the pixel address test. It is sufficient to measure the readout length to know whether the pixel has responded or not. All tests are performed at the full speed of 40 MHz and the reverse bias voltage applied to the silicon sensor is 150 V. When setting DAC registers that control voltages of the ROCs it is important to give the hardware $20 - 100\,\mu$s to settle down at the new voltage. Otherwise no reproducible test results will be obtained. The DAC registers which need a relatively long time to recover are those controlling the trim voltage (Vtrim), the calibration voltage (Vcal) or the analog voltage (Vana).

3 Pretests

3.1 Analog current test

The voltage of the analog part is set in such a way that each ROC draws a current of 24 mA. This is achieved by adjusting the Vana DAC. Starting from its default value, this DAC is increased (decreased) as long as the analog current is below (above) 24 mA. The analog current is measured 100 ms after setting the Vana DAC.

3.2 Unification of the ultra-black levels

The decoding of the analog readout signal relies mainly on the correct detection of the so called ultra-blacks. These are clock cycles where the analog output takes a very low level. The TBM header starts with three ultra-blacks and its trailer with two ultra-blacks. One ultra-black indicates the beginning of the readout of a ROC (see Fig. 2). Without optimization the levels of the ROC ultra-blacks vary among themselves and differ from the TBM ultra-black level. With the help of the VIbias_roc DAC the ROC ultra-black levels can be adjusted to the TBM ultra-black levels. This is simply done by finding the VIbias_roc DAC value for which the ROC ultra-black level differs least from the TBM ultra-black level.

3.3 Threshold/timing test

To use the internal calibration signal for the further tests, its timing has to be brought into accordance with the trigger signal. The calibration signal of the ROC can be delayed with respect to the 40MHz clock in steps of 1 ns with the CalDel DAC. Furthermore the signal threshold, controlled by the VthrComp DAC, has to be tuned with the calibration signal. Since these two issues, the timing and the threshold, are strongly correlated, they are tuned in one step. The response of a pixel is scanned for over the whole VthrComp-CalDel parameter space. A typical result is shown in Fig. 3. Note that the VthrComp DAC is inverted: a high DAC value corresponds to a low threshold. For too high VthrComp DAC values the signal disappears abruptly. The reason for this is that the

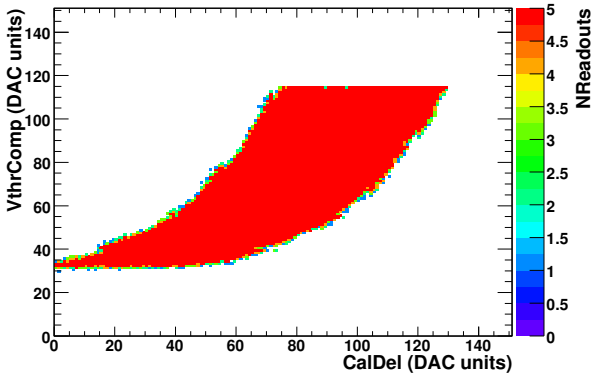

Figure 3: Signal region in the CalDel - VthrComp plane.

threshold falls below the noise and the pixel stops working properly. The VthrComp DAC value at which this happens is called the minimal threshold level. The DACs VthrComp and CalDel are now set in the following way. The VthrComp value is chosen to lie 25 DAC values below the noise level. For this VthrComp value the center of the signal window is chosen as CalDel value. This measurement is done for a few pixels and the averaged VthrComp and CalDel values are stored for further use. The method described above gives a good working point for a specific Vcal DAC value, e.g. the default value given in Tab. 1. For different calibration voltages the whole procedures would have do be redone in an analogous way.

4 Functionality tests

4.1 A comment on thresholds

The word 'threshold' can have several meanings. First one has to distinguish between Vcal and VthrComp thresholds. With a Vcal threshold we mean the following. Let the VthrComp DAC value be fixed and continuously increase the Vcal DAC value. At a certain Vcal DAC value it is found that the pixel starts to respond. To be precise, we define the threshold to be the interpolated Vcal DAC value, where the efficiency is equal to 50%. Similarly a VthrComp threshold is measured by fixing the Vcal DAC value and varying the VthrComp DAC value. Usually this measurement is done for a fixed bunch crossing. Therefore this type of threshold is called an in-time threshold. Assume that a pixel has an in-time Vcal threshold of 60. It is important to note that this does not mean that the pixel does not respond to Vcal values lower than 60. It only means that in the given bunch crossing no signals with lower Vcal values are registered. It is well possible that signals with lower Vcal DAC values can be observed in the previous bunch crossing. If a threshold independent of such timing issues should be determined, the thresholds have to be measured in different bunch crossings. The minimum of all these thresholds is called the absolute threshold. For the trim algorithm always this kind of threshold is measured. In all other tests in-time thresholds are measured.

The threshold measurements are done in two steps. In a first step the complete DAC range is scanned with only a few readouts. From this result a rough value for the threshold is determined. In the second step a window around this rough threshold value is scanned with a larger number of readouts.

4.2 Pixel test

The functionality of each pixel is checked by inducing a signal via an internal calibration capacitance. First, it is tested that the masked (disabled) pixel does not respond if a calibration signal is sent to it. Second, for the enabled pixel 10 calibration signals are sent and the number of output signals is registered. The pixel is fully working if all signals were registered, the pixel is defective, if no output signal was registered at all. As a result of this test, a list of defective pixels is produced. Three modules have been tested so far and only 6 dead pixels have been found out of almost 200000 pixels.

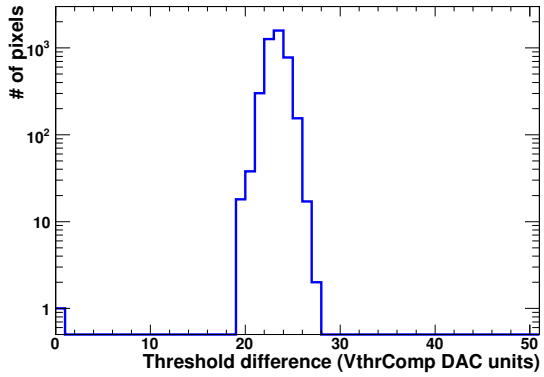

Figure 4: Threshold differences between a trimmed and an untrimmed state for all pixels on a ROC.

4.3 Trim bit test

To fine tune the thresholds of the individual pixels, in each pixel unit cell four trim bits can be set. In this test, the functionality of these four trim bits is verified. The trimming mechanism is ineffective if all trim bits are turned on (trim value = 15). By turning off the trim bits the threshold of the pixel is lowered. The strength of the modification is controlled by the trim voltage (Vtrim DAC) which can be set per ROC. The biggest modification is achieved when all trim bits are turned off (trim value = 0). In a first step the threshold of each pixel is determined in its untrimmed state. Afterwards each trim bit is turned off separately and the threshold is measured again. If no or only a very small difference in the threshold value is observed, the corresponding trim bit is defective. For a working trim bit the trimmed threshold is expected to lie below the untrimmed threshold. Fig. 4 shows the threshold difference for a ROC with one defective trim bit. The following Vtrim DAC values are used during the test:

Table 2: Vtrim DAC values used in the trim bit test.

Trim value	15	14	13	11	7
Vtrim DAC	0	250	200	150	100

4.4 Bump-bonding test

A procedure for bump-bonding the ROCs onto the sensor has been developed at PSI (for details see [3]). A first test of its quality will be performed on the bare modules. But since bonds can be damaged during the module assembly it is mandatory to repeat the bump-bonding test to identify pixels with missing or broken bumps on the fully equipped modules. To speed up and simplify the procedure four electrical methods without the usage of

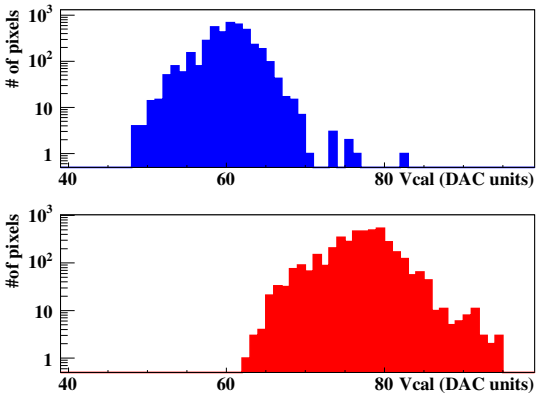

Figure 5: Pixel threshold distribution for a single ROC taken with an external calibration signal (top) and via cross-talk mechanism (bottom).

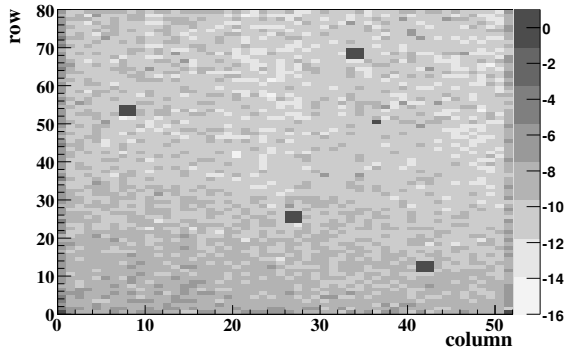

Figure 6: Threshold difference map (52×80 pixels) of the 'modified external calibration' method for a ROC with removed (black areas) bump-bonds.

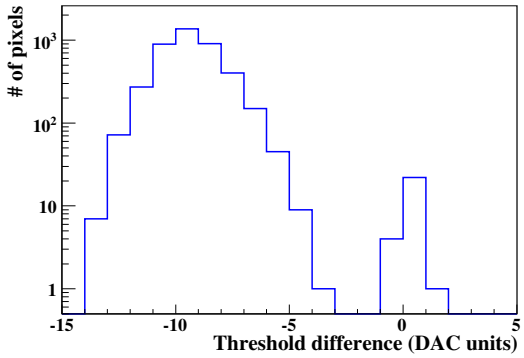

Figure 7: Threshold difference distribution. Pixels with missing bumps contribute to the region around zero.

radioactive sources have been developed.

The first method is called the 'modified external calibration' method. In the ROC the possibility to send a calibration signal through the sensor is implemented (see [1]). In principle, this functionality allows the identification of missing bumps by measuring pixel thresholds. However, due to cross-talk in the chip even for pixels with missing bumps, the threshold values are close to the values measured for pixels with bumps (see Fig. 5). This problem can be avoided by the following procedure. First the pixel for which the bonding quality is to be determined is enabled and a calibration signal through the sensor is sent to it. In this state the Vcal-threshold is measured. In a second step the pixel is kept enabled but an internal calibration signal is sent to its neighboring pixel in the same column. Again the Vcal-threshold is measured. If the bump is missing, then the same cross-talk threshold is measured in both cases. Therefore the difference between the two thresholds should be around zero. If there is a bump, the second threshold is larger than the first one. In such a way missing bumps are identified and their position is recorded for the final module qualification. An example is shown in the Figs. 6 and 7. At the moment it is not clear how well not completely connected bumps can be identified. Further tests with radioactive sources will clarify this point.

The idea of methods two and three is to put the preamplifier of a pixel into saturation. The preamplifiers get very sensitive if the VwllPr and VrgPr DACs are set to their maximal values (255 for VwllPr and 15 for VrgPr). If additionally a high leakage current is drawn through the bump, the preamplifier saturates and the pixel does not respond to internal calibration signals any more. If the bump is missing, there can be no leakage current and the pixel still works. In method two, called the 'high leakage current' method, a leakage current of about 1 mA per ROC is produced by a light source shining on the sensor. The bias voltage is kept at the default value. In method three, called the 'positive bias' voltage, the reverse bias voltage is set to a slightly negative value, e.g. -10 V. This causes a leakage current of about 0.1 mA per ROC. The disadvantage of this method is, that it does not always work for the maximum VrgPr DAC value. For different ROCs different VrgPr DAC values have to be used.

The fourth method with the name 'nominal leakage current' is not yet well understood. It was found empirically, that missing bumps can even be identified, if the preamplifiers are made sensitive (by setting VwllPr and VrgPr to their maximum values) but no high leakage current is drawn. In this case the pixels with missing bumps are not responding, those with well connected bumps are working properly.

The four procedures have been validated by applying them to six specially prepared ROCs with sensors where a few bumps had been removed manually before bump-bonding. All four methods successfully identified the missing bumps on the four chips, which were produced with new sensors. For one chip with an older sensor, only the methods one and four worked, for the second chip with an old sensor, only method one identified the missing bumps successfully. Therefore the 'modified external calibration' method was chosen to be used for the module tests. It was applied to the three available prototype modules. In one tested module no broken bumps have been found. In two other modules 4 and 7 broken bumps have been detected.

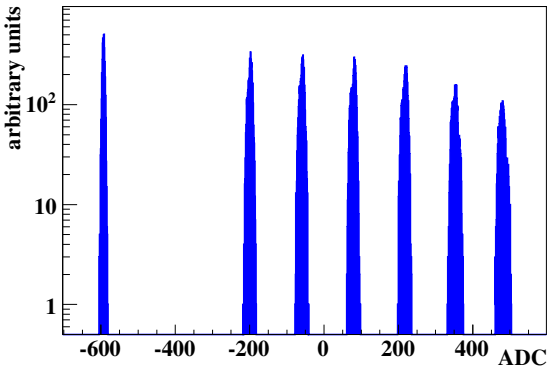

Figure 8: Ultra-black (left most) signal and the six levels of the pixel addresses.

4.5 Pixel address test

An individual pixel address consists of five analog signals: two signals encode the column index and three the row index. Each signal can take six different levels. To decode correctly the pixel address, these levels have to be well separated. The pixel address decoding test has two goals: first, to measure the separation of the six address levels, and second, to check that each pixel correctly encodes its address. Fig. 8 shows the six levels and the ultra-black level. All levels in the figure are well separated from each other and for such a ROC there is no problem to decode the pixel addresses correctly. In the three tested modules no wrong addresses have been observed.

4.6 Noise

In this test, the signal thresholds of all pixels are determined and noisy pixels are identified. Noisy pixels may flood the readout system with a high rate of fake hits and cause significant dead time and data losses. Therefore the thresholds of such pixels must be increased or these pixels should be masked completely. The noise of a pixel is determined by measuring the so called S-curve, i.e. the efficiency of the pixel as a function of the amplitude of the calibration signal. If the noise is Gaussian, the S-curve has the shape of an error function and its width is a direct measure of the noise (see Fig. 9). A difficulty arises from the fact, that the voltage of the calibration signal is not a monotonous function of the Vcal DAC. There are a few cases, where a higher Vcal DAC value corresponds to a lower voltage. For one ROC the calibration voltage was measured as a function of the Vcal DAC, see Fig. 10. This measurement is used to plot the efficiency directly as a function of the calibration voltage. These data points are then fit with an error function and the width and the position of the 50% point is extracted. The average noise and the spread of the noise distribution are part of the module qualification. For non-irradiated modules the threshold

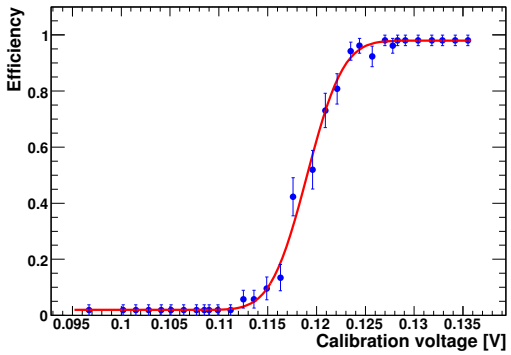

Figure 9: Fit of an error function to the S-curve, the efficiency vs. calibration signal.

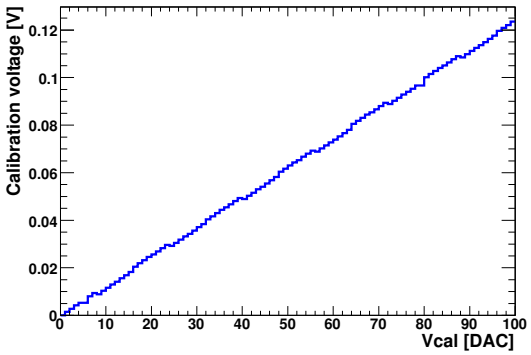

Figure 10: The calibration voltage as a function of the Vcal DAC.

will be set at 2000–2500 electrons, hence the average noise level should not exceed 400–500 electrons and the

spread should not be more than a few hundred electrons. The relation between the Vcal DAC and the ionization charge was measured during a test beam to be linear. The slope seems to vary from ROC to ROC. For the module used in the testbeam the values varied from 51 – 69 electrons per Vcal DAC. For this work a value of 65 electrons per Vcal DAC was used. Fig. 11 illustrates the noise distribution of a single ROC.

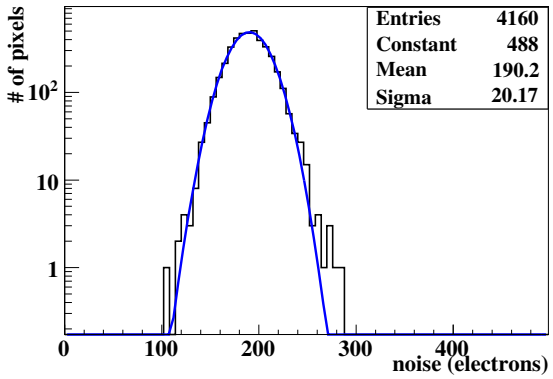

Figure 11: The noise distribution of single ROC.

5 Characterization tests

5.1 Trimming

The aim of the trim algorithm is to unify the physical thresholds of all pixels on a readout chip. To reach this goal, the following parameters can be adjusted. A global threshold can be set per ROC with the VthrComp DAC. To account for the pixel to pixel variations four trim bits can be set in each pixel unit cell. By turning off these bits the threshold of the pixel is decreased. The strength of the correction is determined by the trim voltage (Vtrim DAC), which can only be set per ROC.

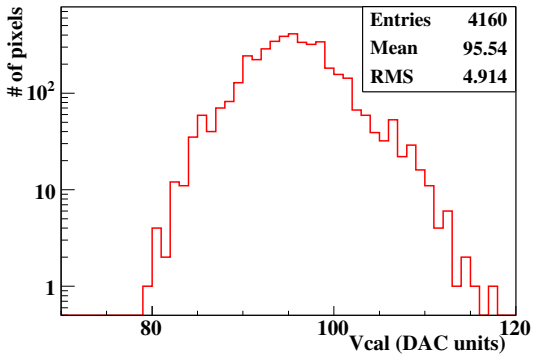

Figure 12: Pixel threshold distribution for an untrimmed readout chip.

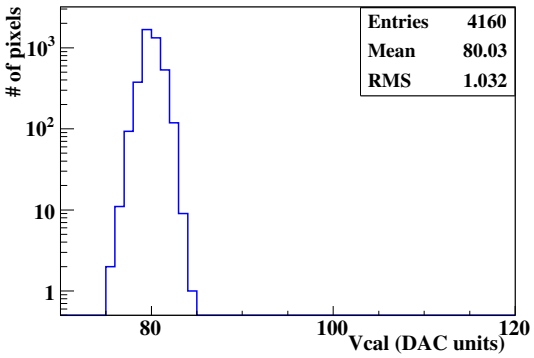

Figure 13: Pixel threshold distribution for a trimmed readout chip.

The only relevant input parameter to the algorithm described below is the absolute physical threshold at which the response is to be unified. In practice this threshold is fixed by choosing a value of the Vcal DAC, which controls the height of the internal calibration pulse.

The first step is to find a value for the global threshold which corresponds to the chosen Vcal value. This is done by measuring for each pixel the VthrComp-threshold value at which the signal with the given Vcal value appears. Since the thresholds can only be lowered afterwards, the minimum value of this distribution determines the global VthrComp value (remember that the VthrComp DAC is inverted). Threshold values from outliers with threshold deviating more than five times the root mean square from the mean, are neglected. This value is used during the

rest of the algorithm.

The second step of the trim algorithm is to find an appropriate trim voltage. To find this, the Vcal-thresholds of all pixels are measured. The pixel, which has the highest threshold is used to determine the trim voltage, again outliers are neglected. For this pixel all trim bits are turned on and the Vtrim DAC is increased, until the threshold of this pixel is at the same level as the target threshold. After this, the trim voltage is not changed any more.

The third step of the trim algorithm consists in setting the trim bits for all pixels. The straightforward way to do this, would be to enable more and more trim bits, until the thresholds of all pixels are at the same level. To speed up the algorithm, a binary search for the optimal trim bit value is performed. In the first run all thresholds are measured with the trim bits set to the mean value. Since the possible trim values range from 0 to 15, this corresponds to a trim value of 7. Depending on whether the threshold lies below or above the target value, the trim bit value is decreased or increased by 4 and all thresholds are measured again. If the difference to the target threshold became smaller, the new trim value is used for the next iteration. Otherwise the previous value of 7 is used for the next step. In exactly the same manner, three more iterations are done. In the second iteration the trim bit value is varied by 2, in the third and fourth iteration by 1. At the end all thresholds are measured once again to validate the procedure. Pixel threshold distributions for a single readout chip are shown in Fig. 12 before trimming and in Fig. 13 after trimming.

5.2 Pulse height calibration

For each hit in a pixel, the height of the generated pulse is recorded in the analog signal. This pulse height gives a measure for the ionization charge collected in the pixel. For cluster reconstruction the measured pulse height in ADC counts has to be converted into the corresponding charge. Since this conversion is not the same for all pixels, the calibration has to be done for each pixel separately.

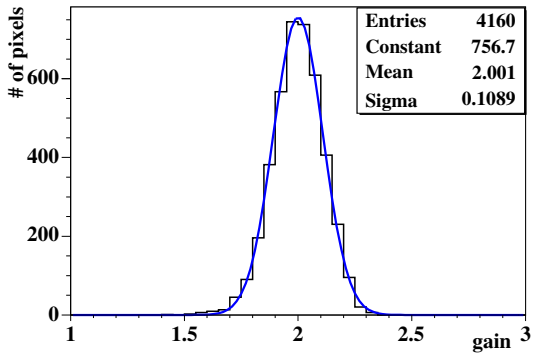

Figure 14: Gain distributions for a single ROC.

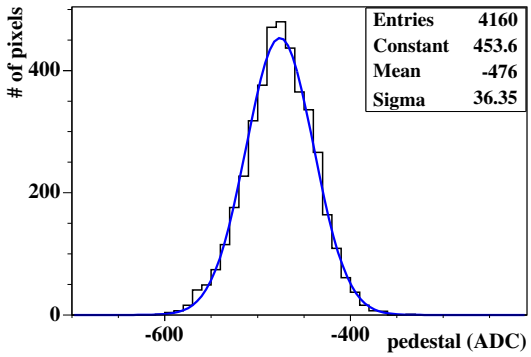

Figure 15: Pedestal distributions for a single ROC.

The calibration is performed by injecting calibration signals with various amplitudes to each pixel and measuring the corresponding pulse heights. The Vcal DAC values for which the pulse heights are measured, are 50, 100, 150, 200 and 250 in the low range, 30, 50, 70, 90 and 200 in the high range. It was found that the following function provides a very good fit to the Vcal value as a function of the pulse height p:

$$\mathrm{vcal} = \tan(c_0 p - 1.4) + c_1 p^3 + c_2 p^2 + c_3 p + c_4\,,$$

where the c_i's are five free parameters.

The pulse height is a linear function of Vcal over quite a large range. If the saturation for high values does not need to be precisely known, the curve can be described by two parameters, namely the slope and offset of a linear fit. The slope is also called gain, the offset is called pedestal. These calibration parameters are needed in off-line and on-line (at the high level trigger) analysis. It may be problematic to save the calibration data for each individual pixel because of their large number. A simplification would be the use of approximate calibration constants averaged over one double column or ROC. This will result in a degradation of the hit resolution due

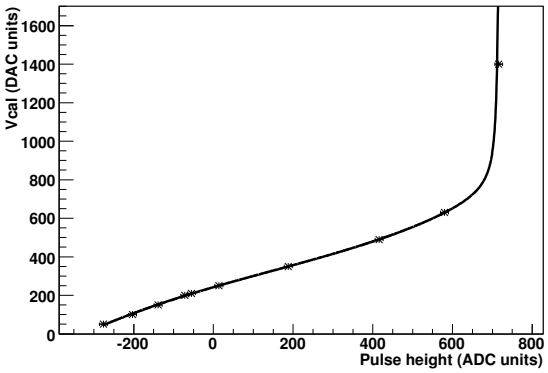

Figure 16: Fit to the Vcal vs. pulse height curve.

to less precise charge interpolation. The use of approximative values of gains and pedestals requires that the variations of these parameters among the pixels are not too large. The spread in the parameters is acceptable if the mis-calibration contribution to the track and vertex reconstruction is less than the effects of multiple scattering and misalignment. According to [4] the tolerable variation of the gains is about 20%–40% and the pedestal variation might be as large as 1000–2000 electrons.

A fit to the linear part of the calibration curve is performed and the gain and the pedestal are recorded. The distributions of these two values over a ROC provide twofold information. If any of the distributions is too broad, the module should be rejected. Additionally, if some pixels have a gain and/or a pedestal far (e.g. more than 4–5 times the RMS) from the mean value, these pixels are counted as defective ones. The distributions of gains and pedestals for a single ROC are presented in Fig. 14 and Fig. 15 respectively. The standard deviation is about 5% for the gain distribution and about 36 [ADC] $\times$ 0.5 [Vcal / ADC] $\times$ 65 [electrons / Vcal] $\sim$ 1200 electrons for the pedestal distribution.

5.3 $I - V$ curve

The measurement of the sensor leakage current versus the reverse depletion voltage (I-V curve) will be done several times during the module production. This measurement will also be performed on a fully assembled module with the aim to verify the absence of any damage which might have occurred during assembly. The leakage current is measured in steps of 5 V, starting from 0 V up to 600 V, see Fig. 17. The time between two measurements is about 5 s. The total leakage current should not exceed 2 μA at the operational voltage (V_{OP}) of 150 V. The variation of the leakage current should satisfy the following constraint

$$I(V_{OP})/I(V_{OP} - 50V) \leq 2.$$

5.4 Temperature sensor calibration

Each readout chip has a built-in temperature sensor. Its output voltage is compared to a (temperature independent) bandgap reference voltage and the difference is encoded in the third cycle of the chip readout. The first step of a temperature measurement is to convert the measured ADC value of this third clock cycle to a voltage. For this the mentioned bandgap reference is used. This reference provides eight voltages between 400 and 564 mV. By appropriately setting the RangeTemp DAC register, the difference of any of these voltages to 470 mV can be encoded in the third clock cycle. The required correspondence between an ADC value and a voltage difference is obtained by measuring the ADC value for these voltage difference.

In a second step the output voltage of the temperature sensor is related to an absolute temperature. Ideally this correspondence is the same for all readout chips. Unfortunately initial measurements showed that this is not the case and some calibration is needed. Therefore its planned to measure the sensor voltage at different temperatures between $-10°$C and $+30°$C. Figure 18 shows that the sensor voltage depends linearly on the temperature.

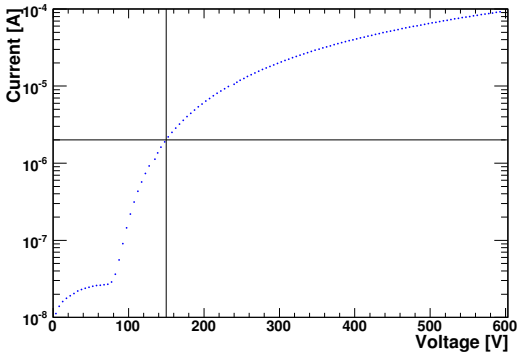

Figure 17: I-V curve of a module sensor.

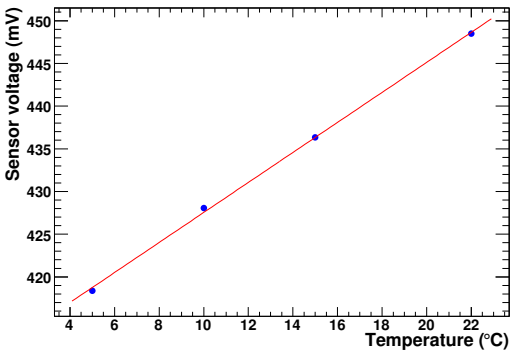

Figure 18: Temperature sensor voltage as a function of the temperature.

5.5 Thermal cycling

The CMS pixel detector will be operated at a low temperature of $-10°$C. To verify the proper performance at this temperature a thermal test is foreseen during the qualification procedure. In Fig. 19 the set-up for the thermal cycling is shown. Up to four modules can be tested concurrently. The thermal test will last about 24 hours and the temperature will be varied from $+30°$C to $-10°$C about 10 times. Operational parameters (like trim bits, gains and pedestals) will be obtained and recorded. Any failure during this procedure will eliminate the use of the module in the final construction.

5.6 Test durations

Table 3 shows the time needed by the individual tests per ROC. The three tests with the largest time consumptions are the trimming, the noise, and the pulse height measurements. At the current state the limiting factor is the data transfer between the test board and the PC via the USB connection. Implementing simple data analysis functionalities directly in the FPGA on the test board should considerably speed up all tests.

Table 3: Approximate durations and numbers of triggers for the readout chip test routines.

Test	Duration per ROC [s]	# triggers per measurement
Analog current	2	
Ultra-black level unification	2	1
Threshold / timing	20	5
Pixel test	1	10
Trim bits test	150	5
Bump-bonding test	300	10
Pixel address test	16	1
Noise (S-Curves)	210	50
Trimming	450	10
Pulse height calibration	150	2
Temperature calibration	5	10
Sum	$\sim$1300	

6 Module qualification

Based on the results of all tests the modules will be qualified for their use in the CMS pixel barrel detector. A grading scheme is currently under development. The qualification criteria can be defined completely only after having tested a reasonable amount of modules. For the time being many questions remain open, like the definition

Figure 19: A set-up for thermal test of CMS pixel barrel modules.

of the defective pixels. It is clear that pixels which do not respond or have missing bump are defective. It is not so obvious in the case of defective trim bits (one or two), highly resistive bump-bonds (which still work) or broad pedestal distribution. Generally, modules will be sorted into three or four quality classes. Those which pass the quality tests and have less than $\sim 1\%$ defective pixels will be qualified to be used in the pixel detector. If the amount of defects is between 1% and 2%, modules may be considered as spare ones. If the number of defective pixels is more than 2%, modules will be rejected. In the three modules tested so far the maximum fraction of defective pixels is less than 10^{-4}.

7 Conclusion

In the coming years about 800 barrel modules will be assembled at PSI. Each of them should pass comprehensive tests and be qualified to be used in the construction of the CMS pixel barrel detector. A qualification procedure has been established to ensure a reliable and high-quality device. One of the most crucial tests concerns the bump-bonding quality. Several procedures have been developed and validated. All of them provide consistent results. Another important procedure is the trimming of the ROCs. A sophisticated but fast algorithm has been developed to guarantee an excellent unification of the pixel thresholds down to 2%. The measurement of the pixel noise, gain and pedestal allows to set a module in the correct operational regime. I-V test and thermal cycling procedure ensure that modules can be operated under CMS conditions. The overall qualification procedure will be tuned and verified during the module pre-production period.

8 Acknowledgment

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